UP-TO-DATE

MEMORY

DATA & COMPARISON TABLES

STATIC RAM • BIPOLAR RAM • CACHE ADDRESS COMPARATORS
DYNAMIC RAM • PROM • REGISTER PROM • EPROM • EEPROM
VIDEO RAM • 1^2C-BUS RAM • SERIAL RAM • RAM MODULES • FIFO

TECH/ECA ASIA-PACIFIC EDITION

memory integrated circuits

data dictionary & comparison table

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GB PREFACE

This is the 2nd edition of the ECA Table "mem", a data and comparison table listing programmable IC memory devices.

As computer capacities grow, so too do the demands on memory devices. This data and comparison table does not include ROMs sincetheir means of comparison and equivalents are very restricted.

In this table the various types having the same pin assignment and same programming have been grouped together into families; the names of the families corresponding to the most popular type indentification in each case - although, it should be mentioned, that it is often very difficult to decide which family designation is correct. To help the user find the device he wants, the alphanumeric list of contents is not given by page number but by family. Each type identification can thus belocated immediately.

This "mem" table is intended to provide circuit designers,amateurs, computer freaks and students alike an overview and hints regarding the programming and equivalent types of memory devies.

The "mem" table is divided into two logical sections.

Section 1:

"Functional list of contents": This is of great help in finding a suitable type device since it is itemized according to type, capacity and pin No. of the memory device, i.e. it provides the user with an overview of the many memory devices listed.

"Explanations": This describes the basis properties of the various memory devices and lists general information explaining the configuration of the data table.

Section 2:

"Data table": All data important to the user such as memory organization, case styles, technology, manufacturer, logic and programming tables, standard and maximum ratings as well as the connection diagram are all grouped together here for a good overview.

To enable this wealth of data to be clearly tabulated with as much informational value as possible, special data such as response diagrams had to be eliminated since these would have overtaxed the scope of this book. The individual types have been grouped together into families which are arranged in rigid numerically ascending order.

Precise outline drawings are not included this time, since solid-state memory devices are nearly always only socket-mounted and thus thisdictates the pin-center-spacing; apart from this the PLCC, LCC, memory modules and SMD cases are shaped to hardly permit replacement by other types.

We trust that this "mem table" will become a "must" in your data documentation. Although the very latest word and data processing systems were used in compiling this data book, the publisher must reserve the right to errors excepted despite all care taken, as is usual in such high-detail data compilations.

alphanumeric list of contents

Type	Family
Am 2101	2101
Am 2111	2111
Am 2147	2147
Am 2167	2167
Am 2700	74200
Am 2701	74301
Am 2702	74189
Am 2703	74189
Am 2708	8223
Am 2709	8223
Am 2710	82126
Am 2711	82126
Am 2712	82130
Am 2713	82130
Am 2718	8223
Am 2719	8223
Am 2720	82126
Am 2721	82126
Am 2728	82147
Am 2729	82147
Am 2730	82140
Am 2731	82140
Am 2732	82136
Am 2733	82136
Am 2740	82195
Am 2741	82195
Am 2743	82321
Am 2764	2764
Am 7489	74189
Am 9016	4116
Am 9044	2147
Am 9060	2680
Am 9101	2101
Am 9102	2102

Type	Family
Am 9111	2111
Am 9112	2112
Am 9114	2114
Am 9124	2114
Am 9128	4016
Am 27128	27128
Am 27180	7680
Am 27181	7680
Am 27184	7684
Am 27185	7684
Am 27190	82190
Am 27191	82190
Am 74189	74189
Am 74289	74189
C 2118	4816
C 2147	2147
C 2164	4164
C 2732	2732
C 3636	82190
C 27128	27128
C 27256	27256
D 2128	4016
DM 7489	74189
DM 7506	74219
DM 7507	74219
DM 7725	87476
DM 7727	8727
DM 8506	74219
DM 8507	74219
DM 8577	8223
DM 8578	8223
DM 8599	74189
DM 8725	87476
DM 8727	8727

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DM 10414	10414
DM 10415	10415
DM 10422	10422
DM 10470	10470
DM 10474	10474
DM 54188	8223
DM 54189	74189
DM 54287	82126
DM 54288	8223
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DM 54471	82135
DM 54472	82147
DM 54473	82147
DM 54474	82140
DM 54475	82140
DM 54570	82130
DM 54571	82130
DM 54572	82136
DM 54573	82136
DM 74188	8223
DM 74189	74189
DM 74200	74200
DM 74206	74301
DM 74287	82126
DM 74288	8223
DM 74289	74189
DM 74387	82126
DM 74470	82135
DM 74471	82135
DM 74472	82147
DM 74473	82147
DM 74474	82140
DM 74475	82140
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DM 74572	82136
DM 74573	82136
DM 77180	7680
DM 77181	7680
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DM 77184	7684
DM 77185	7684
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DM 77191	82190
DM 77193	87191
DM 77195	82195
DM 77280	7680
DM 77281	7680
DM 77290	82190
DM 77291	82190
DM 77321	82321
DM 77421	82321
DM 77474	87474
DM 77476	87476
DM 87180	7680
DM 87181	7680
DM 87183	87183
DM 87184	7684
DM 87185	7684
DM 87188	8223
DM 87190	82190
DM 87191	82190
DM 87193	87191
DM 87195	82195
DM 87228	7680
DM 87229	7680
DM 87280	7680
DM 87281	7680

Type	Family
DM 87288	8223
DM 87290	82190
DM 87291	82190
DM 87295	82140
DM 87296	82140
DM 87321	82321
DM 87421	82321
DM 87474	87474
DM 87476	87476
DM 100422	100422
DM 100470	100470
DM 100474	100474
DM 742387	87288
ET 2128	4016
ET 2147	2147
ET 2716	2716
ETC 2716	2716
ETC 2732	2732
ETL 2128	4016
ETL 2147	2147
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F 1601	1601
F 1620	1620
F 1621	1621
F 1622	1622
F 1623	1623
F 2114	2114
F 2708	2708
F 2732	2732
F 2764	2764
F 3528	4016
F 3567	2167
F 4116	4116
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F 10405	10147
F 10410	10414
F 10411	10414
F 10414	10414
F 10415	10415
F 10416	10149
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F 10470	10470
F 10474	10474
F 100145	100145
F 100402	10145
F 100414	100414
F 100415	100415
F 100416	100416
F 100422	100422
F 100470	100470
F 100474	100474
FCB 6165	6164
FCB 61251	1800
FCB 61252	44252
FCB 61253	61253
FCB 61257	44256
FCB 611025	48128
HEF 4505	4505
HEF 4720	4720
HM 2105	10414
HM 2106	10414
HM 2110	10415
HM 2112	10415
HM 2142	2142
HM 2504	2504
HM 2510	8210

Type	Family
HM 2511	8211
HM 4315	4315
HM 4334	4334
HM 4704	2660
HM 4710	2680
HM 4711	2680
HM 4716	4116
HM 4816	4816
HM 4847	2147
HM 4864	4164
HM 4865	4164
HM 6116	6116
HM 6117	6117
HM 6147	2147
HM 6148	2148
HM 6167	2167
HM 6168	2169
HM 6264	6164
HM 6267	2167
HM 6268	2169
HM 6287	1600
HM 6288	1620
HM 6787	1600
HM 6788	1620
HM 10414	10414
HM 10422	10422
HM 10470	10470
HM 10474	10474
HM 10480	10480
HM 46810	6810
HM 50256	41256
HM 50257	41257
HM 50464	4464
HM 50465	4464

Type	Family
HM 51256	41256
HM 51258	41258
HM 62256	61256
HM 65256	61256
HM 100415	100415
HM 100422	100422
HM 100470	100470
HM 100474	100474
HM 100480	100480
HM 435101	2101
HM 472114	2114
HM 511000	411000
HM 511001	411001
HM 511002	411002
HM1 6116	6116
HM1 65161	6116
HM1 65162	6116
HM1 65262	2167
HM1 65641	6164
HM1 65664	6164
HM1 65687	1600
HM1 65688	1620
HM1 65728	6116
HM1 65764	6164
HM1 65767	2167
HM1 65768	2169
HM1 65770	65770
HM1 65772	65772
HM1 65787	1600
HM1 65788	1620
HM1 65789	1622
HM1 65790	1626
HM1 65791	1626
HM3 6116	6116

Type	Family
HM3 65161	6116
HM3 65162	6116
HM3 65262	2167
HM3 65641	6164
HM3 65664	6164
HM3 65687	1600
HM3 65688	1620
HM3 65728	6116
HM3 65764	6164
HM3 65767	2167
HM3 65768	2169
HM3 65770	65770
HM3 65772	65772
HM3 65779	1695
HM3 65787	1600
HM3 65788	1620
HM3 65789	1622
HM3 65790	1626
HM3 65791	1626
HM3E 65664	6164
HM3E 65728	6116
HM3E 65764	6164
HM4 6116	6116
HM4 65161	6116
HM4 65162	6116
HM4 65262	2167
HM4 65641	6164
HM4 65664	6164
HM4 65687	1600
HM4 65688	1620
HM4 65728	6116
HM4 65764	6164
HM4 65767	2167
HM4 65768	2169

Type	Family
HM4 65787	1600
HM4 65788	1620
HM4 65789	1622
HM4 65790	1626
HM4 65791	1626
HMT 65664	6164
HMT 65687	1600
HMT 65688	1620
HMT 65728	6116
HMT 65764	6164
HMT 65767	2167
HMT 65768	2169
HMT 65779	1695
HMT 65787	1600
HMT 65788	1620
HMT 65789	1622
HMT 65790	1626
HMT 65791	1626
HN 2764	2764
HN 5865	2864
HN 25044	82136
HN 25045	82136
HN 25084	7684
HN 25085	7684
HN 25088	7680
HN 25089	7680
HN 25168	82190
HN 25169	82190
HN 27101	271023
HN 27128	27128
HN 27256	27256
HN 27301	271023
HN 27512	27512
HN 48016	2716

Type	Family
HN 58064	2864
HN 271024	271024
HN 462532	2532
HN 462708	2708
HN 462716	2716
HN 462732	2732
HN 482732	2732
HN 482764	2764
HN 4827128	27128
HYB 4116	4116
HYB 41256	41256
HYB 511000	41024
HYB 514100	44100
HYB 514256	424256
HYB 514400	44400
HYM 39500	4256
HYM 91000	1000
HYM 94000	94000
HYM 361020	361020
HYM 362020	362020
HYM 362500	362500
HYM 365120	365120
IM 2114	2114
IM 2147	2147
IM 2148	2148
IM 4116	4116
IM 5501	74189
IM 5503	74301
IM 5508	8210
IM 5518	8211
IM 5523	74200
IM 5533	74301
IM 5600	8223
IM 5603	82126

Type	Family
IM 5604	82130
IM 5605	82140
IM 5606	82136
IM 5610	8223
IM 5623	82126
IM 5624	82130
IM 5625	82140
IM 5626	82136
IM 6508	6508
IM 6518	6518
IM 7005	2660
IM 7027	2660
IM 7114	2114
IM 7141	2147
IM 7280	2680
IM 7410	410
IM 7708	2708
IMS 1203	2147
IMS 1223	2148
IMS 1400	2167
IMS 1403	2167
IMS 1420	2168
IMS 1423	2168
IMS 1600	1600
IMS 1601	1601
IMS 1605	1605
IMS 1620	1620
IMS 1624	1623
IMS 1625	1625
IMS 1626	1626
IMS 1629	1629
IMS 1630	6164
IMS 1635	1635
IMS 1695	1695

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IMS 1800	1800
IMS 1820	1820
IMS 2600	2600
ITT 4027	2660
KM 2816	2816
KM 2817	2817
KM 2864	2864
KM 2865	2865
KM 4164	4164
KM 6264	6164
KM 6816	6116
KM 41256	41256
KM 41257	41257
KM 41464	4464
KM 44256	424256
KM 44258	424258
KM 62256	61256
KM 411001	41025
KM 411002	411002
KM 4110000	41024
KMM 44256	4256
KMM 44257	4257
KMM 48256	4256
KMM 48257	4257
KMM 49256	4256
KMM 49257	4257
KMM 54256	4256
KMM 54257	4257
KMM 58256	4256
KMM 58257	4257
KMM 59256	4256
KMM 59257	4257
KMM 481000	1000
KMM 481001	1001

Type	Family
KMM 491000	1000
KMM 491001	1001
KMM 581000	1000
KMM 581001	1001
KMM 591000	1000
KMM 591001	1001
L 6530	74301
L 6531	74200
L 6560	74189
L 6561	74189
LH 2111	2111
LH 2114	2114
LH 4027	2660
LH 5101	2101
LH 5114	2114
LH 5606	82136
LH 5626	82136
LH 6116	4116
M 2716	2716
M 2732	2732
M 2764	2764
M 8571	8571
M 9306	9306
M 9346	9346
M 27128	27128
M 27256	27256
M 27512	27512
M 54700	82126
M 54730	8223
M 54740	82136
M 54741	82136
M 58721	2101
M 58722	2111
M 58723	2112

Type	Family
M 58725	4016
M 58751	2102
M 58755	2680
M 58756	2660
M 58759	4116
M 58981	2114
M 271024	271024
M5 2708	2708
M5K 4116	4116
M5K 4164	4164
M5L 2101	2101
M5L 2102	2102
M5L 2107	2680
M5L 2111	2111
M5L 2112	2112
M5L 2114	2114
M5L 2716	2716
M5L 2732	2732
M5L 2764	2764
M5L 5101	2101
M5L 27128	27128
M5M 2167	2167
M5M 2168	2168
M5M 4164	4164
M5M 4256	41256
M5M 4257	41257
M5M 4464	4464
M5M 5116	6116
M5M 5117	6117
M5M 5165	6164
M5M 5178	6164
M5M 5179	1695
M5M 5187	1600
M5M 5188	1620

Type	Family
M5M 5189	1622
M5M 5255	5255
M5M 5256	5256
M5M 5257	5257
M5M 5258	1820
M5M 41000	411000
M5M 41001	411001
M5M 41002	411002
M5M 44100	44100
M5M 44101	44101
M5M 44102	44102
M5M 44256	424256
M5M 44258	424258
M5M 44266	424256
M5M 44268	424258
M5M 44400	44400
M5M 44402	44402
M5M 51001	51001
M5M 51004	51004
M5M 51008	51008
M5T 4044	2147
MB 461	74189
MB 7051	8223
MB 7052	82126
MB 7053	82130
MB 7054	82136
MB 7057	82126
MB 7058	82130
MB 7059	82136
MB 7121	82136
MB 7122	82136
MB 7123	82147
MB 7124	82147
MB 7141	82321

Type	Family
MB 7142	82321
MB 8101	2101
MB 8102	2102
MB 8107	2680
MB 8111	2111
MB 8112	2112
MB 8114	2114
MB 8115	2115
MB 8116	4116
MB 8118	4816
MB 8125	2125
MB 8128	4016
MB 8144	2147
MB 8147	2147
MB 8148	2148
MB 8149	2148
MB 8167	2167
MB 8168	4016
MB 8216	4116
MB 8224	2660
MB 8227	2660
MB 8264	4164
MB 8265	4164
MB 8266	4164
MB 8401	6508
MB 8411	6518
MB 8516	2716
MB 8532	2732
MBM 2114	2114
MBM 2732	2732
MBM 2764	2764
MC 10145	10145
MC 41256	4256
MC 411000	411000

Type	Family
MCM 1423	2168
MCM 2016	4016
MCM 2018	4016
MCM 2102	2102
MCM 2111	2111
MCM 2112	2112
MCM 2114	2114
MCM 2115	2115
MCM 2125	2125
MCM 2147	2147
MCM 2148	2148
MCM 2149	2148
MCM 2167	2167
MCM 2532	2532
MCM 2708	2708
MCM 2716	2716
MCM 2801	2801
MCM 2802	2802
MCM 2814	2814
MCM 2816	2816
MCM 4016	4016
MCM 4027	2660
MCM 4096	2660
MCM 4116	4116
MCM 4180	4180
MCM 4517	4816
MCM 5101	2101
MCM 6064	6164
MCM 6164	6164
MCM 6168	2168
MCM 6206	61256
MCM 6207	1800
MCM 6208	1820
MCM 6256	41256

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MCM 6264	6164
MCM 6268	2168
MCM 6269	2169
MCM 6287	1600
MCM 6288	1620
MCM 6290	1622
MCM 6292	6292
MCM 6293	6293
MCM 6294	6294
MCM 6295	6295
MCM 6508	6508
MCM 6518	6518
MCM 6604	2660
MCM 6605	6605
MCM 6616	4116
MCM 6632	6632
MCM 6633	6633
MCM 6641	2147
MCM 6664	4164
MCM 6665	4164
MCM 6810	6810
MCM 6815	6605
MCM 7620	82130
MCM 7621	82130
MCM 7640	82140
MCM 7641	82140
MCM 7642	82136
MCM 7643	82136
MCM 7680	7680
MCM 7681	7680
MCM 7684	7684
MCM 7685	7684
MCM 10139	10139

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MCM 10144	10414
MCM 10145	10145
MCM 10146	10415
MCM 10147	10147
MCM 10148	10148
MCM 10149	10149
MCM 10152	10414
MCM 10415	10415
MCM 10539	10139
MCM 10544	10414
MCM 10545	10145
MCM 10546	10415
MCM 10547	10147
MCM 10548	10148
MCM 10549	10149
MCM 10552	10414
MCM 14505	4505
MCM 14537	4537
MCM 14552	4552
MCM 41464	4464
MCM 60256	61256
MCM 62350	62350
MCM 62351	62351
MCM 65116	6116
MCM 65147	2147
MCM 65148	2148
MCM 68111	2111
MCM 68112	2112
MCM 68708	2708
MCM 68732	2732
MCM 68764	2764
MCM 68766	2764
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MCM 93415	8210
MCM 93422	93412
MCM 93425	2125
MCM 145101	2101
MCM 146508	6508
MCM 146518	6518
MCM 511000	41024
MCM 511001	41025
MCM 511002	411002
MCM 514256	424256
MCM 514258	424258
MH 25608	4256
MH 25609	4256
MK 2147	2147
MK 2148	2148
MK 2716	2716
MK 4027	2660
MK 4096	2660
MK 4104	2147
MK 4116	4116
MK 4118	4118
MK 4164	4164
MK 4166	2167
MK 4167	2167
MK 4168	2168
MK 4169	2169
MK 4178	4178
MK 4179	4179
MK 4180	4180
MK 4187	1600
MK 4200	2660
MK 4202	4202
MK 4332	4332
MK 4480	4480
MK 4501	4501
MK 4502	4502
MK 4503	4503
MK 4504	4504
MK 4505	4505
MK 4508	4508
MK 4511	4511
MK 4513	4503
MK 4516	4516
MK 4801	4118
MK 4802	6116
MK 4808	4808
MK 4809	4809
MK 4812	6116
MK 4818	4808
MK 4819	4809
MK 4830	4830
MK 4832	61256
MK 4864	6164
MK 4865	6164
MK 4874	4874
MK 4875	4874
MK 4880	4880
MK 4889	4889
MK 4898	4898
MK 4899	4899
MK 6116	6116
MK 45264	45264
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MK 48127	48127
MK 48128	48128
MKB 2716	2716
MKB 4027	2660
MKB 4104	2147
MKB 4116	4116
MKB 4118	4118
MKB 4168	2168
MKB 4332	4332
MKB 4501	4501
MKB 4556	41256
MKB 4564	4164
MKB 4801	4801
MKB 6116	6116
MKI 4802	6116
MKI 4812	6116
MKI 6116	6116
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MM 2102	2102
MM 2111	2111
MM 2112	2112
MM 2114	2114
MM 2147	2147
MM 2704	2704
MM 2708	2708
MM 2716	2716
MM 2758	2758
MM 4280	2680
MM 5247	2147
MM 5257	2147
MM 5280	2680
MM 5290	4116
MM 7489	74189
MM 74929	6508
MM 74930	6518
MM 74989	74189
MN 1001	2680
MN 1002	2680
MN 2147	2147
MN 2148	2148
MN 2764	2764
MN 4164	4164
MN 4216	4016
MN 4264	4416
MN 4364	4168
MN 4416	6116
MN 4464	6164
MN 4700	521000
MN 4701	4701
MN 4760	4760
MN 4780	4780
MN 41256	41256
MN 41257	41257
MN 41464	4464
MN 44251	44256
MN 44252	44252
MN 44253	44253
MN 44256	44256
MN 47464	47464
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MN 411002	411002
MN 414000	44100
MN 414002	44102
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MN 414258	424258
MN 424256	424256
MN 4141000	44400
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MSL 8515	8223
MSL 8516	8223
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Type	Family
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MSM 3741	2680
MSM 3743	2680
MSM 3764	4164
MSM 5114	2114
MSM 5128	6116
MW 4060	2680
MW 4104	2660
MWS 5114	2114
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N 2101	2101
N 2102	2102
N 2111	2111
N 2112	2112
N 2115	2115
N 2125	2125
N 2501	2501
N 2606	2606
N 2660	2660
N 2680	2680
N 2690	4116
N 2704	2704
N 2708	2708
N 3101	74189
N 4027	2660
N 7489	74189
N 8209	8209
N 8210	8210
N 8211	8211
N 8216	8216
N 8217	8216
N 8219	8219
N 8223	8223

Type	Family
N 8225	74189
N 8227	82126
N 8350	8X350
N 10139	10139
N 74189	74189
N 74200	74200
N 74201	74200
N 74219	74219
N 74301	74301
N 74410	74410
N 82110	8210
N 82111	8211
N 82114	82114
N 82115	82115
N 82116	8216
N 82117	8216
N 82123	8223
N 82126	82126
N 82129	82126
N 82130	82130
N 82131	82130
N 82135	82135
N 82136	82136
N 82137	82136
N 82140	82140
N 82141	82140
N 82147	82147
N 82180	7680
N 82181	7680
N 82183	82183
N 82184	7684
N 82185	7684
N 82187	82187
N 82189	82189

Type	Family
N 82190	82190
N 82191	82190
N 82195	82195
N 82208	82208
N 82210	82210
N 82212	82212
N 82321	82321
N 82400	82400
N 82401	82400
N 82641	82641
N 93415	8210
N 93425	2125
N 821281	821281
N 822708	822708
NMC 2114	2114
NMC 2141	2147
NMC 2147	2147
NMC 2148	2148
NMC 2532	2532
NMC 2716	2716
NMC 2732	2732
NMC 2749	2749
NMC 2751	2751
NMC 2764	2764
NMC 2816	2816
NMC 3764	4164
NMC 5257	2147
NMC 5295	4816
NMC 6164	6164
NMC 6508	6508
NMC 6518	6518
NMC 9306	9306
NMC 9307	9307
NMC 9326	9326

Type	Family
NMC 9346	9346
NMC 9356	9356
NMC 9366	9366
NMC 9716	2816
NMC 9810	9810
NMC 9817	2817
NMC 9840	9840
NMC 9864	2864
NMC 27128	27128
NMC 27256	27256
NMC 27512	27512
NMC 41257	41257
NMC 61256	61256
NMC 271023	271023
NMC 271024	271024
NSC 4164	4164
P 2128	4016
PCD 5101	2101
PCD 5114	2114
PCD 8571	8571
PCF 8570	8570
PCF 8571	8571
PCF 8581	8581
PCF 8582	8582
PCF 8583	8583
PL 77288	87288
PL 87288	87288
S 8209	8209
S 8210	8210
S 8211	8211
S 8216	8216
S 8217	8216
S 8223	8223
S 54200	74200
S 54201	74200
S 54301	74301

Type	Family
S 82114	82114
S 82115	82115
S 82123	8223
S 82130	82130
S 82131	82130
S 82136	82136
S 82137	82136
S 82140	82140
S 82141	82140
S 82180	7680
S 82181	7680
S 82184	7684
S 82185	7684
S 82190	82190
S 82191	82190
S 822708	822708
SBB 6116	6116
SMJ 4161	4161
SMJ 4164	4164
SMJ 4256	41256
SMJ 4416	4416
SMJ 4461	4461
SMJ 4464	4464
SMJ 27010	271023
SMJ 27128	27128
SMJ 27210	271024
SMJ 27256	27256
SMJ 27512	27512
SMJ 41024	41024
SMJ 44256	44256
SN 7489	74189
SN 54189	74189
SN 54219	74219
SN 54222	74222

Type	Family
SN 54224	74224
SN 54227	74222
SN 54228	74224
SN 54229	74229
SN 54232	74232
SN 54233	74233
SN 54234	74234
SN 54235	74235
SN 54236	74236
SN 54289	74189
SN 54319	74219
SN 74188	8223
SN 74189	74189
SN 74201	74200
SN 74209	8211
SN 74219	74219
SN 74222	74222
SN 74224	74224
SN 74225	74225
SN 74227	74222
SN 74228	74224
SN 74229	74229
SN 74232	74232
SN 74233	74233
SN 74234	74234
SN 74235	74235
SN 74236	74236
SN 74287	82126
SN 74288	8223
SN 74289	74189
SN 74301	74301
SN 74309	8210
SN 74319	74219
SN 74387	82126

Type	Family
SN 74400	82400
SN 74401	82400
SN 74454	7684
SN 74455	7684
SN 74470	82135
SN 74471	82135
SN 74472	82147
SN 74473	82147
SN 74474	82140
SN 74475	82140
SN 74476	82136
SN 74477	82136
SN 74478	7680
SN 74479	7680
SN 742151	742151
SN 742152	742152
SN 742153	742153
SN 742154	742154
SN 742232	742232
SN 742233	742233
SN 742708	822708
SN 747201	747201
SN 747202	747202
ST 2402	2402
ST 9356	9356
ST 271001	271023
TACT 2150	2150
TBP 1410	82126
TBP 1822	82135
TBP 1842	82147
TBP 1846	82140
TBP 2410	82126
TBP 2441	82136
TBP 2481	7684

Type	Family
TBP 2822	82135
TBP 2842	82147
TBP 2845	82140
TBP 2846	82140
TBP 2885	7680
TBP 2886	7680
TBP 18030	8223
TBP 28165	87191
TBP 28166	82190
TBP 282708	822708
TC 5017	2101
TC 5114	2114
TC 5501	2101
TC 5508	6508
TC 5514	2114
TC 5516	6117
TC 5517	6116
TC 5518	6117
TC 5561	1600
TC 5562	1600
TC 5563	6164
TC 5564	6164
TC 5565	6164
TC 5588	1635
TC 5589	1695
TC 51832	51832
TC 55257	61256
TC 55416	1620
TC 55417	1622
TC 57256	27256
TC 511000	411000
TC 511001	411001
TC 511002	411002
TC 514256	424256

Type	Family
TC 514258	424258
TC 518128	518128
TC 521000	521000
TC 524256	524256
TC 524257	524257
TC 551001	48128
TC 571000	271023
TC 571001	271023
TC 571024	271024
THM 8512	8512
THM 8514	8514
THM 41000	41000
THM 41001	41001
THM 41002	41002
THM 81000	1000
THM 81001	1001
THM 81002	1002
THM 91000	1000
THM 91001	1001
THM 91002	1002
THM 91010	1000
THM 91020	1000
THM 91021	1001
THM 91022	1002
TM 4161	4161
TM 4164	4164
TM 4256	4256
TM 4257	4257
TM 4416	4416
TM 4464	4464
TMM 311	2111
TMM 312	2112
TMM 313	2102
TMM 314	2114
TMM 315	2147
TMM 321	2704
TMM 322	2708
TMM 323	2716
TMM 415	2660
TMM 416	4116
TMM 2015	6116
TMM 2016	4016
TMM 2018	4016
TMM 2063	6164
TMM 2064	6164
TMM 2068	2169
TMM 2088	6164
TMM 2089	1695
TMM 2732	2732
TMM 2764	2764
TMM 4164	4164
TMM 27128	27128
TMM 27256	27256
TMM 27512	27512
TMM 41256	41256
TMM 41257	41257
TMM 41464	4464
TMS 2114	2114
TMS 2147	2147
TMS 2149	2148
TMS 2167	2167
TMS 2168	2168
TMS 2169	2169
TMS 2508	2758
TMS 2516	2716
TMS 2532	2532
TMS 2564	2564
TMS 2708	2708
TMS 2716	2716
TMS 2732	2732
TMS 2749	2749
TMS 2764	2764
TMS 2864	2864
TMS 4016	4016
TMS 4027	2660
TMS 4030	2680
TMS 4033	2102
TMS 4034	2102
TMS 4035	2102
TMS 4039	2101
TMS 4042	2111
TMS 4043	2112
TMS 4044	2147
TMS 4045	2114
TMS 4060	2680
TMS 4070	4116
TMS 4116	4116
TMS 4161	4161
TMS 4164	4164
TMS 4256	41256
TMS 4257	41257
TMS 4416	4416
TMS 4461	4461
TMS 4464	4464
TMS 27010	271023
TMS 27128	27128
TMS 27210	271024
TMS 27256	27256
TMS 27291	27291
TMS 27292	27291
TMS 27512	27512
TMS 41024	41024
TMS 41025	41025
TMS 41027	41027
TMS 41050	41050
TMS 41128	41128
TMS 44251	44251
TMS 44256	44256
TMS 44257	44257
TMX 4461	4461
TMX 27010	271023
TMX 27128	27128
TMX 27210	271024
TMX 27256	27256
TMX 27512	27512
TMX 41024	41024
TMX 41025	41025
TMX 41026	41026
TMX 41027	41027
TMX 41029	41029
TMX 44256	44256
TMX 44257	44257
TMX 44259	44259
TS 2764	2764
TS 2817	2817
TS 5911	5911
TS 6167	2167
TS 6168	2168
TS 9346	9346
TS 27256	27256
TS 71180	7680
TS 71181	7680
TS 71190	82190
TS 71191	82190
TS 71280	7680
TS 71281	7680

Type	Family
TS 71290	82190
TS 71291	82190
TS 71321	82321
TS 71640	82641
TS 71641	82641
TS 271001	271023
TS 271024	271024
XLE 2864	2864
XLE 2865	2865
XLE 4664	4664
XLE 9346	9346
XLM 2816	2816
XLM 2817	2817
XLM 2864	2864
XLM 2865	2864
XLM 4615	4615
XLM 4664	4664
XLS 2804	2804
XLS 2816	2816
XLS 2817	2817
XLS 2864	2864
XLS 2865	2864
XLS 4615	4615
XLS 4664	4664
XLS 9346	9346
2101	2101
2102	2102
2104	2660
2107	2680
2111	2111
2112	2112
2114	2114
2115	2115
2117	4116

Type	Family
2125	2125
2141	2147
2147	2147
2148	2148
2149	2148
2164	4164
2167	2167
2704	2704
2708	2708
2716	2716
2758	2758
2764	2764
3101	74189
3106	74200
3107	74301
3601	82126
3602	82130
3604	82140
3605	82136
3608	7680
3621	82126
3622	82130
3624	82140
3625	82136
3628	7680
3632	82321
3636	82190
5101	2101
6164	6164
6168	2168
6268	2168
6287	1600
6288	1620
6300	82126

Type	Family
6301	82126
6305	82130
6306	82130
6308	82135
6309	82135
6330	8223
6331	8223
6340	82140
6341	82140
6348	82147
6349	82147
6352	82136
6353	82136
6380	7680
6381	7680
6384	822708
6385	822708
6530	74301
6531	74200
6560	74189
6561	74189
7489	74189
8225	74189
8764	2764
9403	9403
9423	9423
10149	10149
10415	10415
10422	10422
10470	10470
10474	10474
27210	271024
27256	27256
27512	27512

Type	Family
27641	27641
34725	74189
63080	8223
63081	8223
63140	82126
63141	82126
63240	82130
63241	82130
63280	82135
63281	82135
63440	82136
63441	82136
63480	82147
63481	82147
63482	82140
63483	82140
63880	7680
63881	7680
82191	82190
82321	82321
87256	27256
93403	74189
93410	93410
93411	74301
93412	93412
93415	8210
93417	82126
93419	8209
93420	8216
93421	8216
93422	93412
93425	8211
93427	82126
93436	82130

Type	Family
93438	82140
93446	82130
93448	82140
93450	7680
93451	7680
93452	82136
93453	82136
93470	93470
93471	93470
93475	2114
93479	82212
93510	82190
93511	82190
93564	82641
93565	82641
93611	82190
93667	82641
100470	100470
100149	100149
100415	100415
100422	100422
100474	100474
631640	82195
631641	82195
631680	82190
631681	82190
633281	82321
µPB 22	74189
µPB 400	82136
µPB 403	82126
µPB 405	82140
µPB 406	82136
µPB 408	7680

Type	Family
µPB 409	82190
µPB 410	8223
µPB 412	82130
µPB 417	822708
µPB 419	419
µPB 421	82135
µPB 423	82126
µPB 424	82147
µPB 425	82140
µPB 426	82136
µPB 427	7684
µPB 428	7680
µPB 429	82190
µPB 2089	74189
µPB 2200	74200
µPB 2202	74200
µPB 2205	8210
µPB 2206	74301
µPB 2289	74189
µPB 10142	10148
µPB 10144	10414
µPB 10148	10148
µPB 10422	10422
µPB 10470	10470
µPB 10474	10474
µPB 100422	100422
µPB 100470	100470
µPB 100474	100474
µPD 402	402
µPD 404	404
µPD 405	405
µPD 410	410
µPD 411	2680
µPD 412	412

Type	Family
µPD 414	2660
µPD 416	4116
µPD 443	6508
µPD 444	2114
µPD 445	445
µPD 446	6116
µPD 449	6117
µPD 454	454
µPD 458	458
µPD 2101	2101
µPD 2102	2102
µPD 2111	2111
µPD 2114	2114
µPD 2147	2147
µPD 2149	2148
µPD 2167	2167
µPD 2716	2716
µPD 2732	2732
µPD 2764	2764
µPD 4016	4016
µPD 4164	4164
µPD 4168	4168
µPD 5101	2101
µPD 27128	27128
µPD 41101	41100
µPD 41102	41100
µPD 41221	41200
µPD 41256	41256
µPD 41257	41257
µPD 41264	41264
µPD 41416	4416
µPD 41464	4464
µPD 42505	41100
µPD 42832	61256

Type	Family
µPD 411000	411000
µPD 411001	411001
µPD 421000	411000
µPD 421001	411001
µPD 421002	411002
µPD 424256	424256
µPD 424258	424258

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Short Description	Family	Pins	Techn.	Output
1MB				
1048576x1-Bit dynamic RAM	41026	18	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	41024	20	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (static column)	41027	18	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (nibble mode)	41025	20	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (static column)	41027	18	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	41029	18	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	41024	26	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	41025	26	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	41026	26	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (static column)	41027	26	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	41029	26	CMOS	TTL-TS
262144x4-Bit dyn. RAM (page mode)	44256	20	CMOS	TTL-TS
262144x4-Bit dyn. RAM (static column)	44257	20	CMOS	TTL-TS
262144x4-Bit dynamic RAM	44259	20	CMOS	TTL-TS
262144x4-Bit dynam. RAM (page mode)	44256	26	CMOS	TTL-TS
262144x4-Bit dyn. RAM (static column)	44257	26	CMOS	TTL-TS
262144x4-Bit dynamic RAM	44259	26	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	18	NMOS	TTL-TS
1048576x1-Bit dynamic RAM	411000	18	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	411000	18	NMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	18	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (nibble mode)	411001	18	NMOS	TTL-TS
1048576x1-Bit dynamic RAM	411001	18	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	411002	18	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	20	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (static c.)	411002	18	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	20	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	411000	20	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	411000	20	NMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	20	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (nibble w.)	411001	20	CMOS	TTL-TS
1048576x1-Bit dynam. RAM-Modul	411000	22	NMOS	TTL-TS
1048576x1-Bit dyn. RAM (static c.)	411002	20	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	24	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	26	NMOS	TTL-TS
1048576x1-Bit dynamic RAM	411000	26	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	411000	26	NMOS	TTL-TS
1048576x1-Bit dyn. RAM (page mode)	411000	26	CMOS	TTL-TS
1048576x1-Bit dyn. RAM (nibble mode)	411001	26	NMOS	TTL-TS
1048576x1-Bit dyn. RAM (nibble mode)	411001	26	CMOS	TTL-TS
1048576x1-Bit dynamic RAM	411002	26	CMOS	TTL-TS
262144x4-Bit dynamic RAM	424256	20	CMOS	TTL-TS
262144x4-Bit dyn. RAM (page mode)	424256	20	NMOS	TTL-TS
262144x4-Bit dyn. RAM (page mode)	424256	20	CMOS	TTL-TS
262144x4-Bit dyn. RAM (static column)	424258	20	CMOS	TTL-TS
262144x4-Bit dyn. RAM (page mode)	424256	24	CMOS	TTL-TS
262144x4-Bit dynamic RAM	424256	26	CMOS	TTL-TS
1MB				
262144x4-Bit dyn. RAM (page mode)	424256	26	NMOS	TTL-TS
262144x4-Bit dyn. RAM (page mode)	424256	26	CMOS	TTL-TS
262144x4-Bit dynamic RAM	424258	26	CMOS	TTL-TS
262144x4-Bit Multiport Video-RAM	524256	32	CMOS	TTL-TS
262144x4-Bit Multiport Video RAM	524257	32	CMOS	TTL-TS
2MB				
262144x8-Bit dynamic RAM-Modul	4256	30	CMOS	TTL-TS

Short Description	Family	Pins	Techn.	Output
262144x8-Bit dynamic RAM-Modul	4256	30	NMOS	TTL-TS
262144x8-Bit dynamic RAM-Modul	4257	30	CMOS	TTL-TS
262144x8-Bit dynamic RAM	4257	30	NMOS	TTL-TS
2,3MB				
262144x9-Bit dynamic RAM-Modul	4256	30	CMOS	TTL-TS
262144x9-Bit dynamic RAM-Modul	4256	30	NMOS	TTL-TS
262144x9-Bit dynamic RAM-Modul	4257	30	CMOS	TTL-TS
262144x9-Bit dynamic RAM	4257	30	NMOS	TTL-TS
262144x9-Bit dynamic RAM-Modul	4256	32	CMOS	TTL-TS
4MB				
524288x8-Bit dyn. RAM-Modul (page m.)	8512	30	CMOS	TTL-TS
524288x8-Bit dyn. RAM-Modul (static col)	8514	30	CMOS	TTL-TS
1048576x4-Bit dyn. RAM-Modul (page m.)	41000	25	CMOS	TTL-TS
1048576x4-Bit dyn. RAM-Modul (nibble m.)	41001	25	CMOS	TTL-TS
1048576x4-Bit dyn. RAM-Modul (static c.)	41002	25	CMOS	TTL-TS
4194304x1-Bit dyn. RAM (page mode)	44100	18	CMOS	TTL-TS
4194304x1-Bit dyn. RAM (page mode)	44100	20	CMOS	TTL-TS
4194304x1-Bit dyn. RAM (static column)	44102	18	CMOS	TTL-TS
4194304x1-Bit dyn. RAM (nibble mode)	44101	20	CMOS	TTL-TS
4194304x1-Bit dyn. RAM (static column)	44102	20	CMOS	TTL-TS
4194304x1-Bit dynamic RAM	44100	26	CMOS	TTL-TS
4194304x1-Bit dyn. RAM (nibble mode)	44101	26	CMOS	TTL-TS
4194304x1-Bit dyn. RAM (static column)	44102	26	CMOS	TTL-TS
1048576x4-Bit dyn. RAM (page mode)	44400	20	CMOS	TTL-TS
1048576x4-Bit dyn. RAM (static column)	44402	20	CMOS	TTL-TS
1048576x4-Bit dynamic RAM	44400	26	CMOS	TTL-TS
1048576x4-Bit dyn. RAM (static column)	44402	26	CMOS	TTL-TS

Shortdescription	Family	Pins	Techn.	Output
8MB				
1048576x8-Bit dynamic RAM-Modul	1000	30	NMOS	TTL-TS
1048576x8-Bit dyn. RAM-Modul (page w.)	1000	30	CMOS	TTL-TS
1048576x8-Bit dyn. RAM-Modul (nibble w.)	1001	30	NMOS	TTL-TS
1048576x8-Bit dyn. RAM-Modul (nibble w.)	1001	30	CMOS	TTL-TS
1048576x8-Bit dyn. RAM-Modul (static c.)	1002	30	CMOS	TTL-TS
9MB				
1048576x9-Bit dynamic RAM-Modul	1000	30	NMOS	TTL-TS
1048576x9-Bit dynamic RAM-Modul	1000	30	CMOS	TTL-TS
1048576x9-Bit dyn. RAM-Mod. (nibble w.)	1001	30	NMOS	TTL-TS
1048576x9-Bit dyn. RAM-Mod. (nibble w.)	1001	30	CMOS	TTL-TS
1048576x9-Bit dyn. RAM-Modul (static c.)	1002	30	CMOS	TTL-TS
262144x36-Bit dyn. RAM-Modul	362500	72	CMOS	TTL-TS
18MB				
524288x36-Bit dynam. RAM-Modul	365120	72	CMOS	TTL-TS
36MB				
4194304x9-Bit dynam. RAM-Modul	94000	30	NMOS	TTL-TS
1048576x36-Bit dynam. RAM-Modul	361020	72	CMOS	TTL-TS
72MB				
2097152x36-Bit dynam. RAM-Modul	362020	72	CMOS	TTL-TS

2.EEPROM

Short Description	Family	Pins	Techn.	Output
256 Bit				
16x16-Bit EEPROM	2801	14	NMOS	
256x1-Bit serial EEPROM	9306	14	NMOS	TTL-TS
256x1-Bit serial EEPROM	9306	14	CMOS	TTL-TS
256x1-Bit serial EEPROM	9306	8	NMOS	TTL-TS
256x1-Bit serial EEPROM	9306	8	CMOS	TTL-TS
256x1-Bit serial EEPROM	9306	8	NMOS	TTL-TS
256x1-Bit serial EEPROM	9307	14	NMOS	TTL-TS
256x1-Bit serial EEPROM	9307	8	NMOS	TTL-TS
512 Bit				
512x1-Bit serial EEPROM	9326	14	CMOS	TTL-TS
512x1-Bit serial EEPROM	9326	8	CMOS	TTL-TS
1kB				
32x32-Bit EEPROM	2802	14	NMOS	
128x8-Bit serial EEPROM	5911	8	CMOS	
128x8-Bit serial EEPROM for I²C-BUS	8571	8	NMOS	I²C-BUS
128x8-Bit EEPROM for I²C-BUS	8581	8	CMOS	I²C-BUS
1024x1-Bit serial EEPROM	9346	14	NMOS	TTL-TS
1024x1-Bit serial EEPROM	9346	14	CMOS	TTL-TS
1024x1-Bit serial EEPROM	9346	14	NMOS	TTL-TS
1024x1-Bit serial EEPROM	9346	8	NMOS	TTL-TS
1024x1-Bit serial EEPROM	9346	8	CMOS	TTL-TS
128x8-Bit EEPROM	9810	18	CMOS	TTL-TS
2kB				
256x8-Bit EEPROM	454	24	NMOS	TTL-TS
256x8-Bit serial EEPROM with IC-BUS	2402	8	CMOS	IC-BUS
256x8-Bit Serial EEPROM	2814	8	CMOS	
256x8-Bit EEPROM for I²C-BUS	8582	16	CMOS	I²C-BUS
-8582	8	CMOS	I²C-BUS	
2048x1-Bit serial EEPROM	9356	14	CMOS	TTL-TS
2048x1-Bit serial EEPROM	9356	8	CMOS	TTL-TS
4kB				
512x8-Bit EEPROM	2804	24	NMOS	TTL
4096x1-Bit serial EEPROM	9366	14	CMOS	TTL-TS
4096x1-Bit serial EEPROM	9366	8	CMOS	TTL-TS
512x8-Bit EEPROM	9840	18	CMOS	TTL-TS
8kB				
1024x8-Bit EEPROM	458	28	NMOS	TTL-TS
16kB				
2048x8-Bit EEPROM	2716	24	NMOS	TTL-TS
2048x8-Bit EEPROM	2816	24	NMOS	TTL-TS
2048x8-Bit EEPROM	2817	28	NMOS	TTL-TS
2048x8-Bit EEPROM	2817	28	CMOS	TTL-TS
2048x8-Bit EEPROM	4615	24	CMOS	TTL-TS
64kB				
8192x8-Bit EEPROM	2864	28	CMOS	TTL-TS
8192x8-Bit EEPROM	2864	28	NMOS	TTL-TS
8192x8-Bit EEPROM	2864	32	CMOS	TTL-TS
8192x8-Bit EEPROM	2865	28	CMOS	TTL-TS
8192x8-Bit EEPROM	2865	32	CMOS	TTL-TS
8192x8-Bit EEPROM	4664	24	CMOS	TTL-TS
8192x8-Bit EEPROM	4664	28	CMOS	TTL-TS
8192x8-Bit EEPROM	2864	28	CMOS	TTL-TS
8192x8-Bit EEPROM	2864	32	CMOS	TTL-TS

Short Description	Family	Pins	Techn.	Output
8192x8-Bit EEPROM	2865	28	CMOS	TTL-TS
8192x8-Bit EEPROM	2865	28	NMOS	TTL
8192x8-Bit EEPROM	2865	32	CMOS	TTL-TS
3.EPROM				
2kB				
256x8-Bit EPROM	1702	24	NMOS	TTL-TS
4kB				
512x8-Bit EPROM	2704	24	NMOS	TTL-TS
8kB				
1024x8-Bit EPROM	2708	24	NMOS	TTL-TS
1024x8-Bit EPROM	2758	24	NMOS	TTL-TS
16kB				
2048x8-Bit EPROM	2716	24	CMOS	TTL-TS
2048x8-Bit EPROM	2716	24	NMOS	TTL-TS
2048x8-Bit EPROM	27291	24	CMOS	TTL-TS
32kB				
4096x8-Bit EPROM	2532	24	NMOS	TTL-TS
4096x8-Bit EPROM	2732	24	NMOS	TTL-TS
4096x8-Bit EPROM	2732	24	CMOS	TTL-TS
64kB				
8192x8-Bit EPROM	2564	28	NMOS	TTL-TS
8192x8-Bit EPROM	2749	24	CMOS	TTL-TS
8192x8-Bit EPROM	2764	24	NMOS	TTL-TS
8192x8-Bit EPROM	2764	28	NMOS	TTL-TS
8192x8-Bit EPROM	2764	28	CMOS	TTL-TS
8192x8-Bit EPROM	2764	32	CMOS	TTL-TS
8192x8-Bit EPROM	27128	28	NMOS	TTL-TS

Shortdescription	Family	Pins	Techn.	Output
8192x8-Bit EPROM	27256	28	NMOS	TTL-TS
8192x8-Bit EPROM	27641	24	CMOS	TTL-TS
128kB				
16384x8-Bit EPROM	2751	28	CMOS	TTL-TS
16384x8-Bit EPROM	27128	28	NMOS	TTL-TS
16384x8-Bit EPROM	27128	28	CMOS	TTL-TS
256kB				
32768x8-Bit EPROM	27256	28	CMOS	TTL-TS
32768x8-Bit EPROM	27256	28	NMOS	TTL-TS
32768x8-Bit EPROM	27256	32	CMOS	TTL-TS
512kB				
65536x8-Bit EPROM	27512	28	CMOS	TTL-TS
65536x8-Bit EPROM	27512	28	NMOS	TTL-TS
1MB				
131072x8-Bit EPROM	271023	32	CMOS	TTL-TS
65536x16-Bit EPROM	271024	40	CMOS	TTL-TS
4.FIFO				
64 Bit				
16 words x 4-Bit FIFO	9403	24	TTL	TTL-TS
16 words x 4-Bit asynchronous FIFO	74222	20	TTL	TTL-OC
16 words x 4-Bit asynchronous FIFO	74222	20	TTL	TTL-TS
16 words x 4-Bit FIFO	74224	16	TTL	TTL-OC
16 words x 4-Bit FIFO	74224	16	TTL	TTL-TS
16 words x 4-Bit asynchronous FIFO	74232	16	TTL	TTL-TS
16 words x 4-Bit asynchronous FIFO	74232	20	TTL	TTL-TS
80 Bit				
16 words x 5-Bit asynchronous FIFO	74225	20	TTL	TTL-TS

Short Description	Family	Pins	Techn.	Output
16 words x 5-Bit asynchronous FIFO	74229	20	TTL	TTL-TS
16 words x 5-Bit asynchronous FIFO	74233	20	TTL	TTL-TS
256 Bit				
64 words x 4-Bit FIFO	9423	24	TTL	TTL-TS
64 words x 4-Bit asynchronous FIFO	74234	16	TTL	TTL-TS
64 words x 4-Bit asynchronous FIFO	74234	20	TTL	TTL-TS
64 words x 4-Bit asynchronous FIFO	74236	16	TTL	TTL-TS
64 words x 4-Bit asynchronous FIFO	74236	20	TTL	TTL-TS
320 Bit				
64 words x 5-Bit asynchronous FIFO	74235	20	TTL	TTL-TS
512 Bit				
64 words x 8-Bit asynchronous FIFO	742232	24	TTL	TTL-TS
64 words x 8-Bit asynchronous FIFO	742232	28	TTL	TTL-TS
576 Bit				
64 words x 9-Bit asynchronous FIFO	742233	28	TTL	TTL-TS
640 Bit				
(64x5)x2-Bit bidirectional Biport FIFO	45264	24	CMOS	
(64x5)x2-BIT bidirectional Biport FIFO	45265	24	CMOS	
4608 Bit				
512x9-Bit FIFO	4501	28	CMOS	TTL-TS
512 words x 9-Bit FIFO	4501	32	CMOS	TTL-TS
512 words x 9-Bit asynchronous FIFO	747201	28	CMOS	TTL-TS
5kB				
1024x5-Bit FIFO	4505	20	CMOS	TTL-TS
1024x5-Bit FIFO	4505	24	CMOS	TTL-TS
7kB				
910 words x8 Bit FIFO	41100	24	NMOS	TTL-TS

Short Description	Family	Pins	Techn.	Output
9kB				
1024x9-Bit FIFO	4502	28	CMOS	TTL-TS
1024x9-Bit FIFO	4502	32	CMOS	TTL-TS
1024 words x 9-Bit asynchronous FIFO	747202	28	CMOS	TTL-TS
18kB				
2048x9-Bit FIFO	4503	28	CMOS	TTL-TS
2048x9-Bit FIFO	4503	32	CMOS	TTL-TS
36kB				
4096x9-Bit FIFO	4504	28	CMOS	TTL-TS
40kB				
5048x8-Bit FIFO	41100	24	CMOS	TTL-TS
72kB				
8192x9-Bit FIFO	4508	28	CMOS	TTL-TS
1MB				
262144x4-Bit FIFO (pseudo static)	41050	16	CMOS	TTL
262144x4-Bit FIFO (pseudo static)	41050	20	CMOS	TTL
262144x4-Bit FIFO (pseudo static)	41050	26	CMOS	TTL

5.PROM

Short Description	Family	Pins	Techn.	Output
256 Bit				
32x8-Bit PROM	8223	16	TTL	TTL-OC
32x8-Bit PROM	8223	16	TTL	TTL-TS
32x8-Bit PROM	8223	20	TTL	TTL-OC
32x8-Bit PROM	8223	20	TTL	TTL-TS
32x8-Bit PROM	10139	16	ECL	ECL
32x8-Bit PROM	87288	16	TTL	TTL-TS
32x8-Bit PROM	87288	20	TTL	TTL-TS
1kB				
256x4-Bit PROM	10149	16	ECL	ECL
256x4-Bit PROM	82126	16	TTL	TTL-OC
256x4-Bit PROM	82126	16	TTL	TTL-TS
256x4-Bit PROM	82126	20	TTL	TTL-OC
256x4-Bit PROM	82126	20	TTL	TTL-TS
256x4-Bit PROM	100149	16	ECL	ECL
256x4-Bit PROM	100416	16	ECL	ECL
2kB				
256x8-Bit PROM	82114	24	TTL	TTL-TS
256x8-Bit PROM	82115	24	TTL	TTL-TS
514x4-Bit PROM	82130	16	TTL	TTL-OC
514x4-Bit PROM	82130	16	TTL	TTL-TS
512x4-Bit PROM	82130	20	TTL	TTL-OC
512x4-Bit PROM	82130	20	TTL	TTL-TS
256x8-Bit PROM	82135	16	TTL	TTL-TS
256x8-Bit PROM	82135	20	TTL	TTL-OC
256x8-Bit PROM	82135	20	TTL	TTL-TS

Shortdescription	Family	Pins	Techn.	Output
4kB				
512x8-Bit Register PROM	2845	24	TTL	TTL-TS
512x8-Bit Register PROM	8727	22	TTL	TTL-TS
512x8-Bit PROM	82115	24	TTL	TTL-TS
1024x4-Bit PROM	82136	18	TTL	TTL-OC
1024x4-Bit PROM	82136	18	TTL	TTL-TS
1024x4-Bit PROM	82136	20	TTL	TTL-OC
1024x4-Bit PROM	82136	20	TTL	TTL-TS
512x8-Bit PROM	82140	24	TTL	TTL-OC
512x8-Bit PROM	82140	24	TTL	TTL-TS
512x8-Bit PROM	82140	28	TTL	TTL-OC
512x8-Bit PROM	82140	28	TTL	TTL-TS
512x8-Bit PROM	82147	20	TTL	TTL-OC
512x8-Bit PROM	82147	20	TTL	TTL-TS
512x8-Bit Register PROM	87474	24	TTL	TTL-TS
512x8-Bit Register PROM	87474	28	TTL	TTL-TS
512x8-Bit Register PROM	87476	24	TTL	TTL-TS
512x8-Bit Register PROM	87476	28	TTL	TTL-TS
8kB				
1024x8-Bit Register PROM	2885	24	TTL	TTL-TS
1024x8-Bit PROM	7680	24	TTL	TTL-OC
1024x8-Bit PROM	7680	24	NMOS	TTL-OC
1024x8-Bit PROM	7680	24	TTL	TTL-TS
1024x8-Bit PROM	7680	24	NMOS	TTL-TS
1024x8-Bit PROM	7680	28	TTL	TTL-OC
1024x8-Bit PROM	7680	28	TTL	TTL-TS
2048x4-Bit PROM	7684	18	TTL	TTL-OC
2048x4-Bit PROM	7684	18	TTL	TTL-TS

Short Description	Family	Pins	Techn.	Output
2048x4-Bit PROM	7684	20	TTL	TTL-OC
2048x4-Bit PROM	7684	20	TTL	TTL-TS
1024x8-Bit PROM	82183	24	TTL	TTL-TS
1024x8-Bit PROM	82183	28	TTL	TTL-TS
2048x4-Bit PROM	82185	20	TTL	TTL-TS
1024x8-Bit Register PROM	82187	24	TTL	TTL-TS
1024x8-Bit PROM	82187	28	TTL	TTL-TS
1024x8-Bit Register PROM	82189	24	TTL	TTL-TS
1024x8-Bit Register PROM	82189	28	TTL	TTL-TS
1024x8-Bit Register PROM	87183	24	TTL	TTL-TS
1024x8-Bit Register PROM	87183	28	TTL	TTL-TS
1024x8-Bit PROM	822708	24	TTL	TTL-OC
1024x8-Bit PROM	822708	24	TTL	TTL-TS
16kB				
2048x8-Bit PROM	419	24	TTL	TTL-TS
2048x8-Bit PROM	27291	24	CMOS	TTL-TS
2048x8-Bit PROM	27291	28	CMOS	TTL-TS
2048x8-Bit Register PROM	28166	24	TTL	TTL-TS
2048x8-Bit PROM	82190	24	TTL	TTL-OC
2048x8-Bit PROM	82190	24	NMOS	TTL-OC
2048x8-Bit PROM	82190	24	TTL	TTL-TS
2048x8-Bit PROM	82190	24	NMOS	TTL-TS
2048x8-Bit PROM	82190	28	TTL	TTL-OC
2048x8-Bit PROM	82190	28	TTL	TTL-TS
2048x8-Bit PROM	82190	28	NMOS	TTL-TS
4096x4-Bit PROM	82195	20	TTL	TTL-OC
4096x4-Bit PROM	82195	20	TTL	TTL-TS
2048x8-Bit Register PROM	87191	24	TTL	TTL-TS

Short Description	Family	Pins	Techn.	Output
2048x8-Bit Register PROM	87191	28	TTL	TTL-TS
32kB				
4096x8-Bit PROM	2732	24	NMOS	TTL-TS
4096x8-Bit PROM	2732	24	CMOS	TTL-TS
4096x8-Bit PROM	82321	24	TTL	TTL-OC
4096x8-Bit PROM	82321	24	TTL	TTL-TS
4096x8-Bit PROM	82321	24	NMOS	TTL-TS
4096x8-Bit PROM	82321	28	TTL	TTL-TS
64kB				
8192x8-Bit PROM	2749	24	CMOS	TTL-TS
8192x8-Bit PROM	2749	28	CMOS	TTL-TS
8192x8-Bit PROM	2764	28	NMOS	TTL-TS
8192x8-Bit PROM (one-time programm.)	2764	28	CMOS	TTL-TS
8192x8-Bit PROM	82641	24	TTL	TTL-OC
8192x8-Bit PROM	82641	24	NMOS	TTL-OC
8192x8-Bit PROM	82641	24	TTL	TTL-TS
8192x8-Bit PROM	82641	24	NMOS	TTL-TS
8192x8-Bit PROM	82641	28	TTL	TTL-OC
8192x8-Bit PROM	82641	28	TTL	TTL-TS
128kB				
16384x8-Bit PROM	27128	28	CMOS	TTL-TS
16384x8-Bit PROM	27128	28	NMOS	TTL-TS
16384x8-Bit PROM (one-time program.)	27128	28	CMOS	TTL-TS
16384x8-Bit PROM (one-time program.)	27128	32	CMOS	TTL-TS
16384x8-Bit PROM	821281	28	TTL	TTL-TS
256kB				
32768x8-Bit PROM	27256	28	CMOS	TTL-TS
32768x8-Bit PROM	27256	28	NMOS	TTL-TS

Short Description	Family	Pins	Techn.	Output
32768x8-Bit PROM (one-time program.)	27256	28	CMOS	TTL-TS
32768x8-Bit PROM (one-time program.)	27256	32	CMOS	TTL-TS
512kB				
65536x8-Bit PROM (one-time program.)	27512	28	CMOS	TTL-TS
65536x8-Bit PROM (one-time program.)	27512	32	CMOS	TTL-TS
1MB				
131072x8-Bit PROM (one-t. program.)	271023	32	CMOS	TTL-TS
65536x16-Bit PROM (one-t. program.)	271024	40	CMOS	TTL-TS

6. Static RAM

16 Bit				
8x2-Bit Multiport Register RAM	10143	24	ECL	ECL
64 Bit				
64x1-Bit static RAM	4505	14	CMOS	TTL-TS
16x4-Bit RAM (bipolar)	10145	16	ECL	ECL
64x1-Bit RAM (bipolar)	10148	16	ECL	ECL
16x4-Bit Register RAM	10402	16	ECL	ECL
16x4-Bit RAM (bipolar)	74189	16	TTL	TTL-OC
16x4-Bit RAM (bipolar)	74189	16	CMOS	TTL-OC
16x4-Bit RAM (bipolar)	74189	16	TTL	TTL-TS
16x4-Bit RAM (bipolar)	74189	16	CMOS	TTL-TS
16x4-Bit static RAM	74189	20	CMOS	TTL-TS
16x4-Bit RAM (bipolar)	74219	16	TTL	TTL-OC
16x4-Bit static RAM	74219	16	CMOS	TTL-TS
16x4-Bit RAM (bipolar)	74219	16	TTL	TTL-TS
16x4-Bit static RAM	74219	20	CMOS	TTL-TS
16x4-Bit RAM (bipolar)	74410	18	TTL	TTL-TS
16x4-Bit Register RAM	100145	24	ECL	ECL

Shortdescription	Family	Pins	Techn.	Output
128 Bit				
128x1-Bit RAM (bipolar)	10147	16	ECL	ECL
256 Bit				
256x1-Bit static RAM	402	18	NMOS	TTL-TS
256x1-Bit static RAM	2501	16	PMOS	TTL-OC
256x1-Bit RAM (bipolar)	2504	16	TTL	TTL-OC
256x1-Bit static RAM	4537	16	CMOS	TTL-TS
64x4-Bit static RAM	4552	24	CMOS	TTL-TS
256x1-Bit static RAM	4720	16	CMOS	TTL-TS
256x1-Bit RAM (bipolar)	8216	16	TTL	TTL-OC
256x1-Bit RAM (bipolar)	8216	16	TTL	TTL-TS
256x1-Bit RAM (bipolar)	10414	16	ECL	ECL
256x1-Bit RAM (bipolar)	74200	16	TTL	TTL-OC
256x1-Bit RAM (bipolar)	74200	16	TTL	TTL-TS
256x1-Bit RAM (bipolar)	74301	16	TTL	TTL-OC
256x1-Bit RAM (bipolar)	93410	16	TTL	TTL-OC
256x1-Bit RAM (bipolar)	100414	16	ECL	ECL
256x1-Bit RAM (bipolar)	100414	24	ECL	ECL
576 Bit				
64x9-Bit RAM (bipolar)	8209	28	TTL	TTL-OC
64x9-Bit RAM (bipolar)	8219	28	TTL	TTL-OC
1kB				
1024x1-Bit static RAM	405	18	NMOS	TTL-TS
256x4-Bit static RAM	412	24	NMOS	TTL-TS
256x4-Bit static RAM	2101	22	CMOS	TTL-TS
256x4-Bit static RAM	2101	22	NMOS	TTL-TS
256x4-Bit static RAM	2101	24	CMOS	TTL-TS
1024x1-Bit static RAM	2102	16	NMOS	TTL-TS

Short Description	Family	Pins	Techn.	Output
256x4-Bit static RAM	2111	18	NMOS	TTL-TS
256x4-Bit static RAM	2112	16	NMOS	TTL-TS
1024x1-Bit static RAM	2115	16	NMOS	TTL-OC
1024x1-Bit static RAM	2125	16	NMOS	TTL-TS
1024x1-Bit static RAM	2125	16	TTL	TTL-TS
256x4-Bit static RAM	2606	16	NMOS	TTL-TS
1024x1-Bit static RAM	6508	16	CMOS	TTL-TS
1024x1-Bit static RAM	6518	18	CMOS	CMOS
1024x1-Bit static RAM	6518	18	CMOS	TTL-TS
128x8-Bit static RAM	6810	24	NMOS	TTL-TS
1024x1-Bit RAM (bipolar)	8210	16	TTL	TTL-OC
1024x1-Bit RAM (bipolar)	8211	16	TTL	TTL-TS
128x8-Bit static RAM for I²C-BUS	8571	8	CMOS	I²C-BUS
1024x1-Bit RAM (bipolar)	10415	16	ECL	ECL
256x4-Bit RAM (bipolar)	10422	24	ECL	ECL
256x4-Bit RAM (bipolar)	93412	22	TTL	TTL-OC
256x4-Bit RAM (bipolar)	93412	22	TTL	TTL-TS
256x4-Bit RAM (bipolar)	93412	24	TTL	TTL-OC
256x4-Bit RAM (bipolar)	93412	24	TTL	TTL-TS
1024x1-Bit RAM (bipolar)	93425	16	TTL	TTL-TS
1024x1-Bit RAM (bipolar)	100415	16	ECL	ECL
1024x1-Bit RAM (bipolar)	100415	24	ECL	ECL
256x4-Bit RAM (bipolar)	100422	24	ECL	ECL
2kB				
256x8-Bit RAM (bipolar)	8X350	22	TTL	TTL-TS
256x8-Bit RAM (bipolar)	8X350	28	TTL	TTL-TS
256x8-Bit static RAM for I²C-BUS	8570	8	CMOS	I²C-BUS
256x8-Bit static RAM for I²C-BUS	8583	8	CMOS	I²C-BUS

Short Description	Family	Pins	Techn.	Output
258x8-Bit RAM (bipolar)	82208	22	TTL	TTL-TS
258x9-Bit RAM (bipolar)	82210	24	TTL	TTL-TS
256x9-Bit RAM (bipolar)	82212	22	TTL	TTL-TS
256x9-Bit RAM (bipolar)	82212	28	TTL	TTL-TS
4kB				
4096x1-Bit static RAM	410	22	NMOS	TTL-TS
1024x4-Bit static RAM	445	20	CMOS	TTL-TS
1024x4-Bit static RAM	2114	18	NMOS	TTL-TS
1024x4-Bit static RAM	2114	18	CMOS	TTL-TS
1024x4-Bit static RAM	2114	18	TTL	TTL-TS
1024x4-Bit static RAM	2114	20	CMOS	TTL-TS
4096x1-Bit ECL RAM (bipolar)	2142	20	ECL	ECL
4096x1-Bit static RAM	2147	18	CMOS	TTL-TS
4096x1-Bit static RAM	2147	18	NMOS	TTL-TS
1024x4-Bit static RAM	2148	18	CMOS	TTL-TS
1024x4-Bit static RAM	2148	18	NMOS	TTL-TS
4096x1-Bit static RAM	4178	22	CMOS	TTL-TS
4096x1-Bit static RAM	4315	18	CMOS	CMOS
1024x4-Bit static RAM	4334	18	CMOS	TTL-TS
4096x1-Bit RAM (bipolar)	10470	18	ECL	ECL
1024x4-Bit RAM (bipolar)	10474	24	ECL	ECL
4096x1-Bit RAM (bipolar)	82400	18	TTL	TTL-OC
4096x1-Bit RAM (bipolar)	82400	18	TTL	TTL-TS
4096x1-Bit RAM (bipolar)	93470	18	TTL	TTL-OC
4096x1-Bit RAM (bipolar)	93470	18	TTL	TTL-TS
4096x1-Bit RAM (bipolar)	100470	18	ECL	ECL
1024x4-Bit RAM (bipolar)	100474	24	ECL	ECL

Short Description	Family	Pins	Techn.	Output
2,5kB				
512x9-Bit BIPORT-RAM	4511	28	CMOS	TTL-TS
512x9-Bit BIPORT RAM	4511	32	CMOS	TTL-TS
8kB				
1024x8-Bit static RAM	4118	24	NMOS	TTL-TS
1024x8-Bit static RAM	4801	24	NMOS	TTL-TS
1024x8-Bit static RAM	4801	32	NMOS	TTL-TS
16kB				
16384x1-Bit static RAM	1600	22	CMOS	TTL-TS
16384x1-Bit static RAM	2167	20	CMOS	TTL-TS
16384x1-Bit static RAM	2167	20	NMOS	TTL-TS
4096x4-Bit static RAM	2168	20	NMOS	TTL-TS
4096x4-Bit static RAM	2168	20	CMOS	TTL-TS
4096x4-Bit static RAM	2169	20	NMOS	TTL-TS
4096x4-Bit static RAM	2169	20	CMOS	TTL-TS
2048x8-Bit static RAM	4016	24	NMOS	TTL
2048x8-Bit static RAM	4016	24	NMOS	TTL-TS
4096x4-Bit static RAM	4179	22	CMOS	TTL-TS
4096x4-Bit stat. RAM w. 4-Bit Comparator	4180	22	CMOS	TTL-TS
4096x4-Bit stat. RAM w. 4-Bit Comparator	4180	24	CMOS	TTL-TS
2048x8-Bit static RAM	4802	28	CMOS	TTL-TS
2048x8-Bit static RAM	4802	32	CMOS	TTL-TS
2048x8-Bit static RAM	6116	24	CMOS	TTL
2048x8-Bit static RAM	6116	24	CMOS	TTL-TS
2048x8-Bit static RAM	6116	24	NMOS	TTL-TS
2048x8-Bit static RAM	6116	28	CMOS	TTL-TS
2048x8-Bit static RAM	6116	32	NMOS	TTL-TS
2048x8-Bit static RAM	6116	32	CMOS	TTL-TS

Shortdescription	Family	Pins	Techn.	Output
2048x8-Bit static RAM	6117	24	CMOS	TTL-TS
16384x1-Bit ECL RAM (bipolar)	10480	20	ECL	ECL
4096x4-Bit Cache Address Comparator	62350	24	CMOS	
4096x4-Bit Cache Address Comparator	62351	24	CMOS	
4096x4-Bit static RAM	65770	22	CMOS	TTL-TS
4096x4-Bit static RAM	65772	24	CMOS	TTL-TS
16384x1-Bit ECL RAM (bipolar)	100480	20	ECL	ECL
40kB				
2048x20-Bit stat. RAM w. Comparator	4202	68	CMOS	TTL-TS
64kB				
65536x1-Bit static RAM	1600	22	CMOS	TTL-TS
65536x1-Bit static RAM	1600	24	CMOS	TTL-TS
65536x1-Bit static RAM	1601	22	CMOS	TTL-TS
65536x1-Bit static RAM	1601	24	CMOS	TTL-TS
16384x4-Bit static RAM	1620	22	CMOS	TTL-TS
16384x4-Bit static RAM	1620	24	CMOS	TTL-TS
16384x4-Bit static RAM	1621	22	CMOS	TTL-TS
16384x4-Bit static RAM	1622	24	CMOS	TTL-TS
16384x4-Bit static RAM	1622	28	CMOS	TTL-TS
16384x4-Bit static RAM	1623	24	CMOS	TTL-TS
16384x4-Bit static RAM	1623	28	CMOS	TTL-TS
16384x4-Bit static RAM	1625	22	CMOS	TTL-TS
16384x4-Bit static RAM	1625	24	CMOS	TTL-TS
16384x4-Bit static RAM	1626	28	CMOS	TTL-TS
16384x4-Bit static RAM	1629	24	CMOS	TTL-TS
16384x4-Bit static RAM	1629	28	CMOS	TTL-TS
8192x8-Bit static RAM	1635	28	CMOS	TTL-TS
8192x8-Bit static RAM	1635	32	CMOS	TTL-TS

Short Description	Family	Pins	Techn.	Output
65536x1-Bit static RAM	2600	16	NMOS	TTL-TS
65536x1-Bit static RAM	2600	18	NMOS	TTL-TS
16384x4-Bit stat. RAM + 4-Bit Comparator	4480	24	CMOS	TTL-TS
8192x8-Bit static RAM Zeropower	4808	28	CMOS	TTL-TS
8192x8-Bit static RAM Zeropower	4809	28	CMOS	TTL-TS
8192x8-Bit stat. RAM w. 8-Bit Comparator	4874	28	CMOS	TTL-TS
8192x8-Bit stat. Cache RAM w. Komp.	4880	28	CMOS	TTL-TS
8192x8-Bit static Parity RAM	4898	28	CMOS	TTL-TS
8192x8-Bit static RAM	6164	28	CMOS	TTL-TS
8192x8-Bit static RAM	6164	28	NMOS	TTL-TS
16384x4-Bit synch. stat. RAM with Latch	6292	28	CMOS	LATCH
16384x4-Bit synch. stat. RAM w. Register	6293	28	CMOS	Register
16384x4-Bit synch. stat. RAM w. Register	6294	28	CMOS	Register
16384x4-Bit synch. stat. RAM w. Latch	6295	28	CMOS	Latch
72kB				
8192x9-Bit static RAM	1695	28	CMOS	TTL-TS
8192x9-Bit static RAM	1695	28	NMOS	TTL-TS
8192x9-Bit static RAM	1695	32	CMOS	TTL-TS
8192x9-Bit static RAM	4889	28	CMOS	TTL-TS
8192x9-Bit static Parity RAM	4899	28	CMOS	TTL-TS
256kB				
65536x4-Bit static RAM	1605	22	CMOS	TTL-TS
65536x4-Bit static RAM	1605	24	CMOS	TTL-TS
262144x1-Bit static RAM	1800	24	CMOS	TTL-TS
262144x1-Bit static RAM	1800	28	CMOS	TTL-TS
65536x4-Bit static RAM	1820	24	CMOS	TTL-TS
65536x4-Bit static RAM	1820	28	CMOS	TTL-TS
32768x8-Bit static RAM Zeropower	4830	28	CMOS	TTL-TS
32768x8-Bit static RAM	5255	28	CMOS	TTL-TS
32768x8-Bit static RAM	5256	28	CMOS	TTL-TS
262144x1-Bit static RAM	5257	24	CMOS	TTL-TS
65536x4-Bit static RAM	44252	24	CMOS	TTL-TS
262144x1-Bit static RAM	44253	24	CMOS	TTL-TS
32768x8-Bit static RAM	44256	28	CMOS	TTL-TS
32768x8-Bit pseudo-static RAM	51832	28	CMOS	TTL-TS
65536x4-Bit static RAM	61253	28	CMOS	TTL-TS
32768x8-Bit static RAM	61256	28	CMOS	TTL-TS
1MB				
131072x8-Bit static RAM	48127	32	CMOS	TTL-TS
131072x8-Bit static RAM	48128	32	CMOS	TTL-TS
1048576x1-Bit static RAM	51001	28	CMOS	TTL-TS
262144x4-Bit static RAM	51004	28	CMOS	TTL-TS
131072x8-Bit static RAM	51008	32	CMOS	TTL-TS
131072x8-Bit pseudo-static RAM	518128	32	CMOS	TTL-TS

7. Video RAM

Short Description	Family	Pins	Techn.	Output
10kB				
920 words x 12-Bit x 2 Digital Video RAM	4780	40	CMOS	TTL
1135 words x 9-Bit Digital Video RAM	4760	28	CMOS	TTL
64kB				
65536x1-Bit Multiport Video RAM	4161	20	NMOS	TTL-TS
65536x1-Bit Multiport Video RAM	4161	22	NMOS	TTL-TS
256kB				
65536x4-Bit Multiport Video RAM	4461	24	NMOS	TTL-TS
65536x4-Bit Multi-Port dynam. RAM	47464	24	NMOS	TTL
1MB				
262144x4-Bit Multiport Video RAM	44251	28	CMOS	TTL-TS
262144x4-Bit Vid. RAM (Field Memory)	521000	40	CMOS	TTL
262144x4-Bit dynamic Video-RAM	521000	40	NMOS	TTL
262144x4-Bit dynamic Video-RAM	521000	64	NMOS	TTL
262144x4-Bit Multiport Video RAM	524256	28	CMOS	TTL
262144x4-Bit Multiport Video RAM	524257	28	CMOS	TTL
1,2MB				
327680 words x 4-Bit dynam. Video-RAM	4701	64	NMOS	TTL

Shortdescription	Family	Pins	Techn.	Output

Explanations

I. General - Sections 2 (Data Table)

1. Explanations regarding page references

All types are listed grouped together into families in strict alphanumerical sequence. Only types having the same pin assignments, the same storage matrix and the same type of storage are grouped together to form a family. The configuration of the Data Table is best explained on the basis of an example page (see last but one cover page).
Storage configuration, type of storage, pin No and pin assignments as well as the supply voltages and programming voltages can all be found at a single glance; this applying to all types of the family concerned and completely independently of the manufacturer.

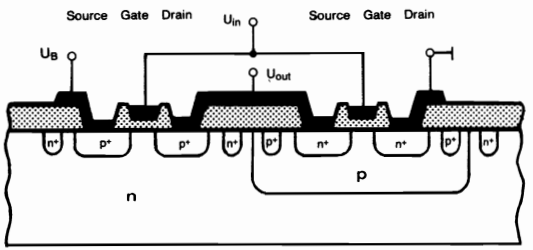
2. Explanations regarding table structure

a) Column "Type"
This column lists all types of the family concerned in strict alphanumerical order.
b) Column "Manuf."
Names of manufacturers are abbreviated for space reasons. Full names and addresses are listed alphabetically on page 1-104 without, however, any pretence of being complete in all details and as regards availability.
c) Column "Case"
This data book contains no precise outline drawings and packages are simply distinguished according to their structures:

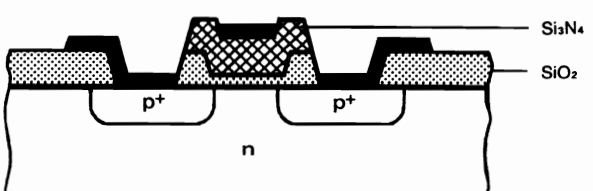
DIC	=	ceramic dual inline package (standard design)
DIP	=	plastic dual inline package (standard design)
FLAT	=	flat package (SMD)
LCC	=	leadless chip carrier - w/o connector leads
PLCC	=	plastic chip carrier
SIC	=	in-line plug-in case w/o connector legs
SIP	=	single inline package
TDIC	=	ceramic dual inline package (slim line, 300 mil)
TDIP	=	plastic dual inline package (slim line, 300 mil)
ZIC	=	zigzag inline case (ceramic)
ZIP	=	zigzag inline case (plastic)

d) Column "Techn."
Abbreviation of technologies concerned.

CMOS	=	complementary metal oxide silicon
ECL	=	emitter coupled logic
NMOS	=	N channel MOS
PMOS	=	P channel MOS
TTL	=	transistor - transistor logic



Cross-section thru a CMOS transistor pair



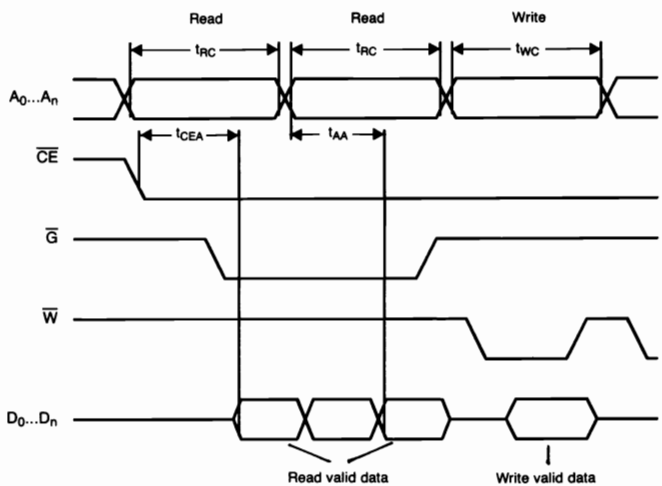
Structure of an NMOS memory transistor

e) Column "T_U°C"
Operating temperature range in which the device will continue to function satisfactorily (ambient temperature).

f) Column "P_{typ}"
Typical power consumption in mW under normal operating conditions (at 25°C Ta [ambient temperature]), unless stated otherwise.

g) Column "$P_{standby}$"
Power consumption in standby operation; applies only to types with standby option.

h) Column "t_{aa}"
Delay in nanoseconds between data input and output of same input pulse (access time).

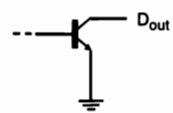


Timing diagram read - read - write

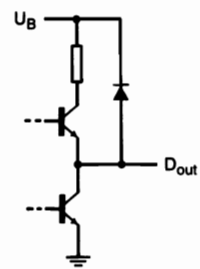
i) Column "t_{ref}"
Delay in milliseconds between start of a signal sequence and the successful reset of the memory to its original condition, periodic recharging of the energy containing the information (on dynamic RAM only) - refresh time.

k) Column "Output"
Abbreviation of basic type of output circuit.

IC-BUS	=	special output for IC´s
I²C-BUS	=	special output for I²C-BUS
MATCH	=	output with match code
Register	=	register output
TTL-OC	=	output with open collector (TTL)
TTL-OD	=	output with open drain (TTL)
TTL-TS	=	tri-state output (TTL)



Outputs with open collector



Tri-state outputs

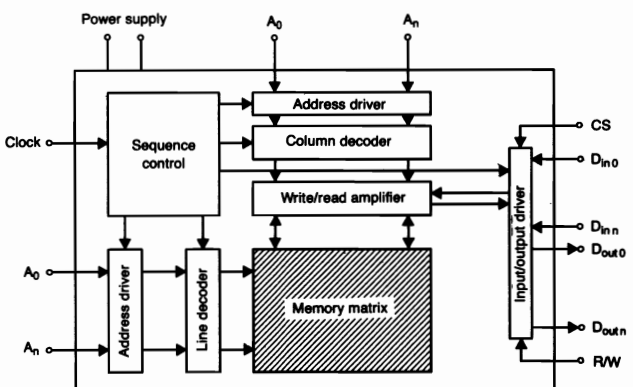
II. Basic explanations regarding memory devices

1. Classification of semiconductor memories

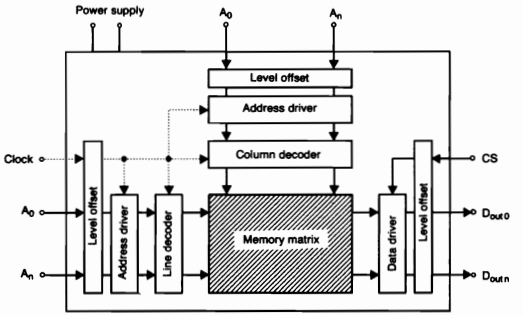
Random access memories (RAM)

Random access memories are probably the most widely used semiconductor memories; actually they are only used as main storage elements for changing programs or data or as buffers and as fast registers.

Everincreasing package densities are producing RAM with higher and higher memory capacity even the mega chip.



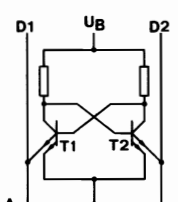
Block diagram of a RAM



Block diagram of a ROM

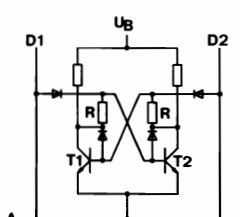
a) Static RAM (sRAM)

Despite the differing technologies for RAM structures the basic function is always the same; two load resistors and two NPN transistors for a flip-flop of which one transistor is ON (logic 1 or H) whilst the other is OFF (logic 0 or L). Only by shutting off the supply voltages or by inverting the condition is a change possible.



a)

Configuration of a static TTL RAM with a single address line standard version (a) and in Schottky diode version (b).

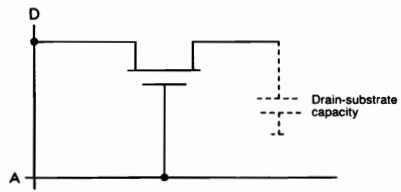


b)

Due to the relatively high power consumption, particularly of bipolar sRAM and the requirement of a great many transistors in MOS technology, dynamic RAM (dRAM) are now finding increasing application.

b) Dynamic RAM (dRAM)

dRAM structures involve almost exclusively MOS technology in which the capacitance is used as the charge storage forming the drain zone of the transistor with the substrate layer. Leakage currents of the charge determining the information necessitate refresh by a current pulse to prevent loss of data.



The advantage of dynamic RAM is their low power consumption, high package density and thus low cost.

2. PROM

These versions differ from read only memories (ROM) merely by being electrically programmable. Due to their long programming times for writing in the information, roughly 50 to 1000 times longer than for reading, these memories are uncertain in popularity. They will retain their stored information even when there is a loss of power supply, unlike RAM.

a) EPROM

EPROM (erasable PROM) can be erased by a strong UV light and then be reprogrammed, after which they can be used to also replace ROM.

b) EEPROM

EEPROM (electrically erasable PROM) must be prepared by an advance, separate erase cycle before being reprogrammed; this cycle must be implemented partly complete and partly word-by-word.

c) One-time programmable EPROM (OTPEPROM)

OTPEPROM are usally EPROM incorporated in a windowless case. Their electrical properties and programming are just the same as for EPROM.

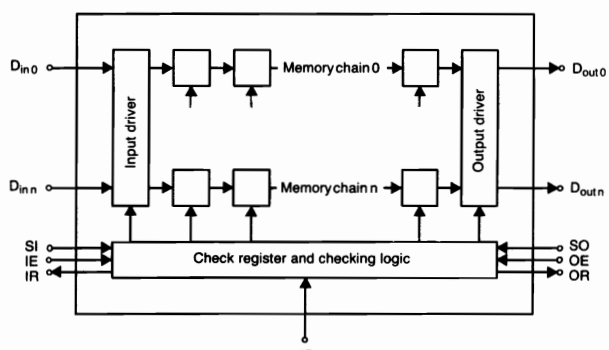
d) PROM

PROM (programmable ROM) can be programmed by the user (by melting certain connections) to achieve the desired information content.

3. FIFO

First-in/first-out memories are a kind of shift register since they allow only one memory location at a time to be read from outside. Addressing is not possible. The main difference to other memories is that the information is presented to the output without necessitating any external influence, i.e. should the memory be empty, the information is instantly available at the output.

FIFO are mainly used for data handling in hardware having differing handling speeds, such as for example, computer and printer.



Block diagram of a FIFO memory device

Abbreviations used in the connection drawing

A0...An	address inputs 0...n
ADQ	address input - data input/output
ALE	address latch enable
AR	address reference
AR0...ARn	address read input 0...n
AW0...AWn	address write input 0...n
BCLR	bit clear control input
BE	block erase
BPE	bulk program enable (data procetion)
BS	block select
BSET	bit set control input
C	compare
CAS	columm address strobe
CE	chip enable
CG0	compare 0 output enable
CG1	compare 1 output enable
CLK	clock
CLR	clear reset
CPS1	serial clock input
CPSO	serial output - clock input
CS	chip select
CTR	control input
$D_0...D_n$	data input/output 0...n
D_{in}	data input
D_{ins}	serial data in
DIR	transceiver direction control
D_{out}	data output
D_{outs}	serial data output
$D_{s0}...D_{sn}$	serial data input/output
DT	data transfer
d.u.	don't use
EMPTY	empty output flag
EP	parity error
FE	enable input
FH	force hit
FL	first load
FM	force miss
FULL	full output flag
G	enable
GND	ground
GS	synchronize enable input
HFULL	half full flag
Hi-Z	high impedance
HOS	H-sync. signal output high-speed
HS	H-sync. signal output
IES	serial input enable
INIT	initialize
INITS	synchronize initialize
INT	open drain interrupt output
IR	input ready
IRE	input ready enable
IRF	input register full output
LDCLK	load clock input
LE	latch enable
Low-Z	low impedance
M	mode control
MATCH	comparator output
Mode	mode
MR	master reset
MS	mode select input
n.c.	not connected
OES	serial output - enable input
OR	output ready
ORE	output register enable
OSC_{in}	oscillator input
OSC_{out}	oscillator output
P	parity enable
PD	presence detect
PE	program enable
PF	power fail interrupt
PGM	program mode
PL	parallel load input
PRE	protect register enable
Prog	program input (EPROM)
PS	pin select
PTC	programing time control

Abbreviations used in the connection drawings

PVC	programm voltage control
Q	output
R	reset
RAS	row address strobe
RC	time constant R/C
RE	read enable
REF	refresh
RR	reset read
RT	retransmit
RW	reset write
R/W	read/write select
SCL	serial clock line
SDA	serial data line
SE	serial enable
SFS	special function select
Shift in	shift in
Shift out	shift out
SRA	split register activity status
SRCLK	serial read clock
SS	start/stop input
ST	strobe
SWCLK	serial write clock
T	test
TOP	transfer out parallel input
TOS	transfer out serial input
TR	register transfer
TTS	transfer to stack input
UNCLK	unload clock input
VCP	program voltage
W	write enable input
WB	write per bit
WM	write mask enable
Word	word length switching input pin (DSC-Mode 910 words by H-level, 858 by L-level)
XI	expansion in
XO	expansion out output

abbreviations of manufacturers

Amd **Advanced Micro Devices Inc.**
USA: 901 Thompson Place, Sunnyvale, CA 94088
BRD: Advanced Micro Devices
W-8000 München 2, Herzog-Heinrich-Straße 3

Exl **EXEL Microelectronics Inc.**
USA: 2150 Commerce Drive, San José, CA 95161-9038

Fch **Fairchild Camera and Instrument Corp.**
USA: 464 Ellis Street, Mountain View, California 94042
A: Fairchild Electronics GmbH
A-1120 Wien, Meldinger Hauptstraße 46
BRD: Fairchild Camera and Instrument GmbH
W-3000 Hannover, Öltzenstraße 15
W-7251 Leonberg, Poststraße 37
W-8080 Fürstenfeldbruck, Industriestraße 10
F: Fairchild Camera & Instrument S.A.
F-92129 Montrouge, Place des Etats - Unis 12
GB: Fairchild Semiconductor
Herts, England EN6 5BU, 230 High Street, Potters Bar
I: Fairchild Semiconducttori S.p.A.
I-20133 Milan, Viale Corsica 7

Fui **Fujitsu Ltd. (Components Group)**
J: 6-1 Marunouchi 1-chome, Chiyoda-ku, Tokyo 100
BRD: Fujitsu Mikroelektronik GmbH,
Arabella Centre, Lyoner Straße 44-48, W-6000 Frankfurt 71

Hit **Hitachi Ltd. (Electronic Devices Group)**
J: 1450 Josuihonmachi, Kodaire City, Tokyo
BRD: Hitachi Europe GmbH (Headquarter)
W-8013 Haar, Hans-Pinsel-Straße 10a
E: Hitachi Electronic Components Division
E-28036 Madrid, Sucursal en España, c/Buganvilla 5
F: Hitachi Electronic, F-94020 Créteil, Immeuble
«Les Gémeaux», 2 Rue Antoine Etex
I: Hitachi Electronic, I-20151 Milano, Via L. Rizzo 8

Inm **INMOS Limited**
GB: 1000 Aztec West, Almondsbury, Bristol BS12 4SQ
BRD: INMOS Business Centre,
SGS-Thomson Microelectronics GmbH, W-8011 Grasbrunn,
Bretonischer Ring 4, Technopark
F: INMOS Business Centre,
SGS-Thomson Microelectronics SA,
F-94253 Gentilly Cedex, 7 Avenue Gallieni, PB 93

Int **Intel Group**
USA: Intel Corp., 3065 Bowers Avenue, Santa Clara, CA 95051
BRD: Intel Semiconductor GmbH,
W-8016 Feldkirchen, Dornacher Straße 1

Isi **Intersil, Inc.**
USA: 10710 North Tantau Avenue, Curpertino, CA 95014
BRD: Spezial Electronic KG
W-8000 München 2, H.-Lingg-Straße 16

Itt **ITT Semiconductors (Intermetall)**
USA: 748 Commerce Way, Woburn, MA 01801
BRD: Intermetall GmbH
W-7800 Freiburg, Hans-Bunte-Straße 19

Mat **Matsushita Electronics Corp.**
J: Nagaokakyo, Kyoto 617
BRD: Panasonic Deutschland GmbH
W-2000 Hamburg 54, Winsbergring 15
F: Panasonic France S.A.
F-92521 Neuilly-sur-Seine Cedex, 139-141 Avenue
Charles de Gaulle
GB: Panasonic Industrial U.K.
Willoughby Road, Bracknell, Berkshire RG12 4FP
I: Panasonic Italia S.P.A.
I-20125 Milano, Via Lucini 19

A=Österreich, B=Belgien, BRD=Bundesrepublik Deutschland, E=Spanien, F=Frankreich, GB=Großbritannien, I=Italien, IRL=Irland, J=Japan, K=Korea, NL=Niederlande

Mhs **MATRA MHS Electronic Center**
F: F-44087 Nantes Cedex 03, La Chantrerie / Route de Gachet CP 3008
BRD: W-8057 Eching, Erfurter Straße 29
GB: Easthampstead Road, Bracknell, Berkshire RG12 1LX
I: I-20148 Milano, Via Vigliani 13

Mic **Micron Technology Inc.**
USA: 2805 East Columbia Road, Boise, Idaho 83706
BRD: W-8011 Aschheim, Marsstraße 3
E: ATD Electronics S.A.
E-28040 Madrid, Plaza Cuidad de Viena 6
F: RepTronic S.A., F-91300 Massy, 1 Rue Marcel Paul
GB: Borehamwood, Hertfordshire, WD6 4SE

Mit **Mitsubishi Electric Corporation**
J: Kita-Itami Works, 4 - 1 Mizuhara, Itami-Shi, Hyogo-Ken Post Code 664
BRD: Mitsubishi Electric Europe GmbH
W-4030 Ratingen 1, Gothaer Straße 8
F: F-92563 Rueil Malmasion Cedex, 55 Avenue de Colmar
GB: Travellers Lane, Hatfield, Herts AL10 8XB
I: I-20041 Agrate Brianza, Palazzo Cassiopea 1

Mmi **Monolithic Memories Inc.**
USA: 2175 Mission College Boulevard, Santa Clara, CA 95054

Mos **Mostek**
USA: 1215 W. Crosby Road, Carrollton, Texas 75006
B: Mostek Europe
B-1170 Brüssel, 150 Chaussee de la Hulpe
BRD: Mostek GmbH
D-8012 Ottobrunn, Zaunkönigstraße 18

Mot **Motorola Semiconductor Products Inc.**
USA: 5005 E. McDowell Road, M370, Phoenix, AZ 85008
BRD: Motorola GmbH, Geschäftsbereich Halbleiter
W-8000 München 82, Schatzbogen 7

Nec **NEC Electronic GmbH (Europa)**
BRD: D-4000 Düsseldorf 30, Oberrather Straße 4
D-3000 Hannover 1, Hindenburgstraße 28/29
D-7000 Stuttgart 30, Heilbronner Straße 314
D-8000 München 2, Arabellastraße 17
E: NEC Electronics S.A., Representacion en España, Edifico «La Caixa»
E-28046 Madrid, Paseo de la Castellana 51
F: NEC Electronics S.A.
F-78142 Velizy Villacoublay Cedex 9, Rue Paul Dautier B.P. 187
GB: NEC Electronics Ltd. (UK)
Cygnus House, Sunrise Park Way, Milton Keynes, MK14 6NP
I: NEC Electronics Italiana S.R.L.
I-20124 Milano, Via Fabio Filzi 25A
I-00189 Rome, P. Le Di Porta Pia, International Business Center
IRL: NEC Electronics Ltd. Dublin Office
Dublin 2, 34/35 South William Street

Nsc **National Semiconductor Corporation**
USA: 2900 Semiconductor Drive, Santa Clara, CA 95052-8090
BRD: National Semiconductor GmbH
D-8080 Fürstenfeldbruck, Industriestraße 10
E: National Semiconductor
E-28036 Madrid, Calle Agustin de Foxa, 27 (9.D)
F: National Semiconductor Expansion 10000
F-92357 Le Plessis Robinison, Route Nationale 186
GB: National Semiconductor Ltd. (UK)
Wiltshire SN2 6UT, the Maple, Kembrey Park Swindon
I: National Semiconductor S.p.A.
I-20089 Rozzano - Milanofiori, Strada 7 - Palazzo R/3

Oki **OKI Electric Industry Co., Ltd.**
J: 10-3 Shibaura 4-Chome, Minato-Ku, Tokyo 108
BRD: OKI Electric Europe GmbH
D-4000 Düsseldorf 11, Emanuel-Leutze-Straße 8

A=Österreich, B=Belgien, BRD=Bundesrepublik Deutschland, E=Spanien, F=Frankreich, GB=Großbritannien, I=Italien, IRL=Irland, J=Japan, K=Korea, NL=Niederlande

Phi **Philips Gloillampen-Fabrieken N.V.**
NL: Eindhoven, Building BA
BRD: Valvo GmbH
W-2000 Hamburg 1, Burchardstraße 19

Rca **RCA Corporation (Solid State Division)**
USA: Route 202, Somerville, NJ 08876
BRD: RCA GmbH
W-2085 Quickborn, Schillerstraße 14

Sam **SAMSUNG Semiconductor**
K: Samsung Main Bldg. 250, 2-ka, Taepyung-Ro., Chung-ku, Seoul
BRD: W-6000 Frankfurt, Friedrich-Ebert-Anlage 2-14
GB: 6 Fl. Victoria House, Southampton Row, WC1, London

Sgs **SGS-ATES Microelettronica S.p.A.** (International Headquarters)
I: I-20041 Agrate Brianza, Via C. Olivetti
BRD: SGS Halbleiter Bauelemente GmbH
W-8018 Grafing, Haindling 17
E: SGS Microelettronica S.p.A.
E-28036 Madrid, Calla Agustin de Foxà 25
F: Societe Generale de Semiconducteurs
F-92120 Montrouge, 21-23 Rue de la Vanne
GB: SGS Semiconductor Limited
Aylesbury, Bucks, Planar House, Walton Street

Sha **Sharp Corporation**
J: 2613-1 Jchinomoyo, Tenri-City, Nava
BRD: Sharp Electronic GmbH
W-200 Hamburg 1, Sonninstr.3

Sie **Siemens Aktiengesellschaft**
BRD: Siemens AG, Bereich Halbleiter
W-8000 München 80, Balanstraße 73
E: E-28020 Madrid, Orense 2, Apartodo 155
F: F-93527 Saint-Denis Cedex 2, 39/47, Bd. Ornano
GB: Windmill Road, Sunbury on Thames, Middlesex TW16 7HS
I: I-20100 Milano, Via Fabio Filzi, 25a
IRL: Unit 8-11 Slaney Road, Finglas Road, Dublin 11

Sig **Signetics Corporation**
USA: 811 E. Arques Avenue, Sunnyvale, CA 94086

Tix **Texas Instruments Inc.**
USA: P.O.-Box 225012, Dallas, TX 75265
BRD: Texas Instruments Deutschland GmbH
W-8050 Freising, Haggertystraße 1
W-1000 Berlin 31, Kurfürstendamm 195-196
W-6236 Eschborn, Düsseldorfer Straße 40
E: Texas Instruments España S.A.
E-28036 Madrid, C/Jose Lazaro Galdino No.6
F: Texas Instruments France
F-78141 Velizy-Villacoublay Cedex, 8-10 Avenue Morane Saulnier
GB: Texas Instruments Ltd.
Manton Lane, Bedford, MK41 7PA
I: Texas Instruments Italia S.p.A., Divisione Semiconduttori
I-02093 Cologne Monzese (Mi), Via Costello della Magliana 38
IRL: Texas Instruments (Ireland)
IRL-Stillorgan, County Dublin, 7/8 Harcourt Strett

Tho **Thomson Semiconducteurs Sales Headquarters**
F: F-78140 Velizy-Villacoublay, 43, Avenue de l'Europe

Tos **Toshiba Corporation**
J: 1-1 Shibaura 1-Chome, Minato-Ku, Tokyo 105
BRD: Toshiba Europa (I.E.) GmbH Electronic Components
W-4000 Düsseldorf 11, Hansaallee 181
W-7250 Leonberg, Eltinger Straße 61
W-8000 München 81, Arabellastraße 33/IV
F: Toshiba Paris
F-93118 Rosny, Sous Bois, Tour de Bureaux de Rosny 2
GB: Toshiba Limited (UK)
Toshiba House, Frimley Road, Frimley, Camberley, Surry GU16 5JJ
I: Toshiba Electronics Italiana S.R.L.
I-20041 Agrate Brianza (Milano), Centro Direzionale Colleoni, Palazzo Orione-Ingresso 3

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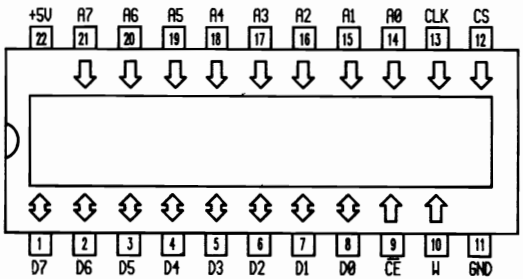
Val **Valvo GmbH**
(Unternehmensbereich Bauelemente der Philips GmbH)
BRD: W-2000 Hamburg 1, Burchardstraße 19
W-3000 Hannover 1, Ikarusallee 1a
W-4300 Essen 1, Lazarettstraße 50
W-6000 Frankfurt 90, Theodor-Heuss-Allee 106
W-7000 Stuttgart 80, Albstadtweg 12
W-7800 Freiburg, Tullastraße 72
W-8000 München 71, Drygalski-Allee 33
W-8500 Nürnberg 10, Bessemerstraße 14

A=Österreich, B=Belgien, BRD=Bundesrepublik Deutschland, E=Spanien, F=Frankreich, GB=Großbritannien, I=Italien, IRL=Irland, J=Japan, K=Korea, NL=Niederlande

section 2

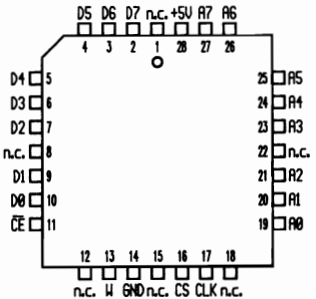
8X350 — 256x8-Bit RAM (bipolar)



$\overline{CE}$	CS	W	CLK	D_n	A_n	Mode
1	X	X	X	Hi-Z	hold	disabled data out
0	1	0	1	X	Hi-Z	input new address
0	1	0	0	Hi-Z	hold	disabled data out
0	0	1	1	data in	hold	write
0	0	1	0	Hi-Z	hold	disabled data out
0	0	0	X	data out	hold	read
0	1	1	1	X	X	not selected
0	1	1	0	Hi-Z	hold	disabled data out

8X350 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 8X350 N	Val	22-DIP	TTL	0...+75	<971		<35		TTL-TS

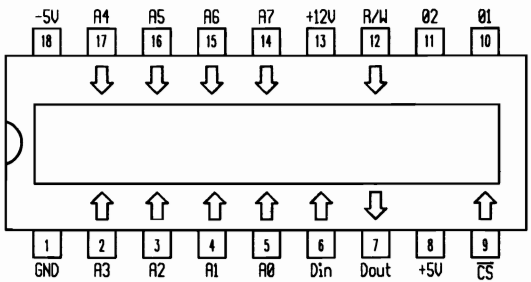
8X350 — 256x8-Bit RAM (bipolar)



$\overline{CE}$	CS	W	CLK	D_n	A_n	Mode
1	X	X	X	Hi-Z	hold	disabled data out
0	1	0	1	X	Hi-Z	input new address
0	1	0	0	Hi-Z	hold	disabled data out
0	0	1	1	data in	hold	write
0	0	1	0	Hi-Z	hold	disabled data out
0	0	0	X	data out	hold	read
0	1	1	1	X	X	not selected
0	1	1	0	Hi-Z	hold	disabled data out

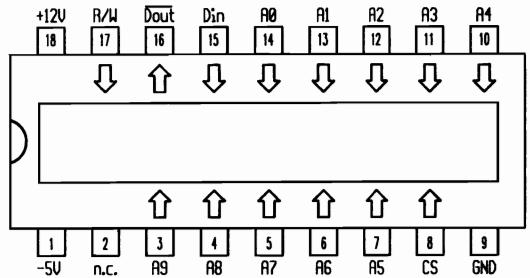
8X350 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 8X350 A	Val	28-PLCC	TTL	0...+75	<971		<35		TTL-TS

402 — 256x1-Bit static RAM



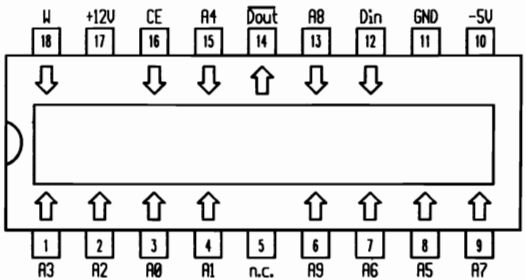
402 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 402 D	Nip	18-DIC	NMOS	-10...+75	$1	$0,3	<450		TTL-TS

404 — 1024x1-Bit dynamic RAM

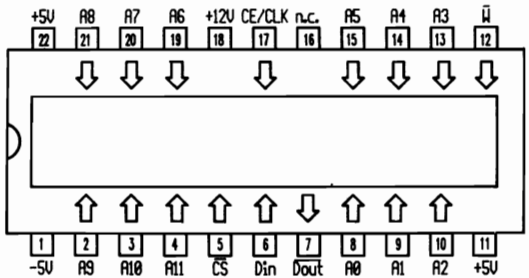


404 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 404 D	Nip	18-DIC	NMOS	0...+75	200	0,2	<450	<2	TTL-TS

405 — 1024x1-Bit static RAM



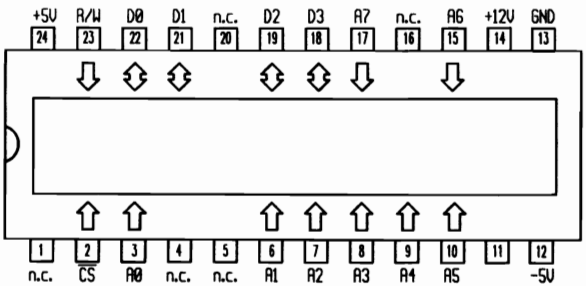
410 — 4096x1-Bit static RAM



405 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 405 D	Nip	18-DIC	NMOS	0...+70	<460	<97	<95		TTL-TS
µPD 405 D-1	Nip	18-DIC	NMOS	0...+70	<513	<97	<80		TTL-TS
µPD 405 D-2	Nip	18-DIC	NMOS	0...+70	<537	<97	<85		TTL-TS

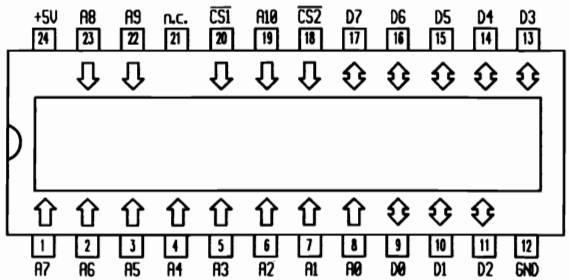
410 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IM 7410 F-11D	Isi	22-DIC	NMOS	0...+70			<70		TTL-TS
IM 7410 F-11P	Isi	22-DIP	NMOS	0...+70			<70		TTL-TS
IM 7410 F-12D	Isi	22-DIC	NMOS	0...+70			<100		TTL-TS
IM 7410 F-12P	Isi	22-DIP	NMOS	0...+70			<100		TTL-TS
µPD 410 D	Nip	22-DIC	NMOS	0...+70	<394	<108	<200		TTL-TS
µPD 410 D-1	Nip	22-DIC	NMOS	0...+70	<490	<108	<150		TTL-TS
µPD 410 D-2	Nip	22-DIC	NMOS	0...+70	<645	<108	<100		TTL-TS

412 — 256x4-Bit static RAM



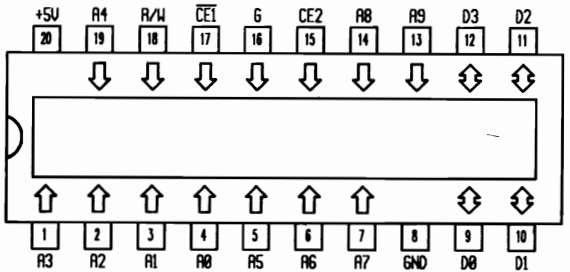
412 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 412 C	Nip	24-DIC	NMOS	-10...+70	<262		<430		TTL-TS
µPD 412 D	Nip	24-DIC	NMOS	-10...+70	<262		<430		TTL-TS

419 — 2048x8-Bit PROM

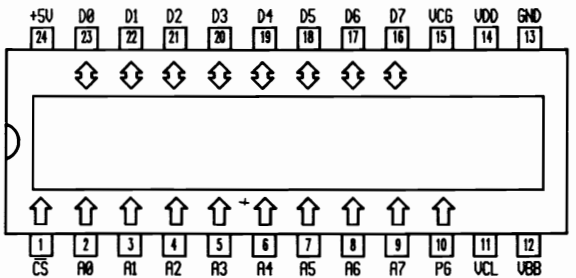


419 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPB 419 C	Nip	24-DIP	TTL	-25...+75	<880		<70		TTL-TS
µPB 419 C-1	Nip	24-DIP	TTL	-25...+75	<880		<60		TTL-TS
µPB 419 C-2	Nip	24-DIP	TTL	-25...+75	<880		<50		TTL-TS
µPB 419 D	Nip	24-DIC	TTL	-25...+75	<880		<70		TTL-TS
µPB 419 D-1	Nip	24-DIC	TTL	-25...+75	<880		<60		TTL-TS
µPB 419 D-2	Nip	24-DIC	TTL	-25...+75	<880		<50		TTL-TS

445 — 1024x4-Bit static RAM



454 — 256x8-Bit EEPROM



Logiktabelle siehe Seite 2-8
Function table see page 2-8
Tableau logique voir page 2-8
Per tavola di logica vedi pagina 2-8
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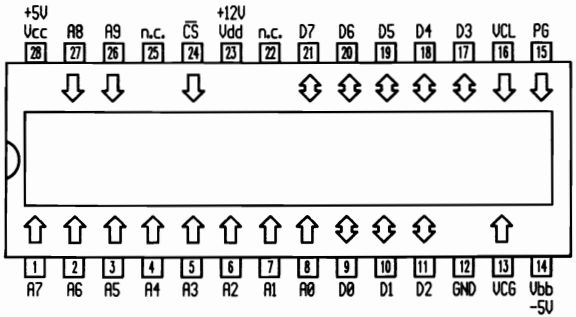
445 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 445 LC	Nip	20-DIP	CMOS	-10...+70	<165	<0,055	<650		TTL-TS
µPD 445 LC-1	Nip	20-DIP	CMOS	-10...+70	<165	<0,055	<450		TTL-TS

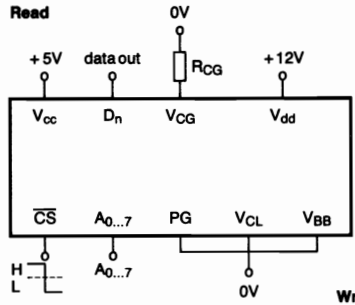
454 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 454 D	Nip	24-DIC	NMOS	-10...+70	670		<800		TTL-TS

458 — 1024x8-Bit EEPROM



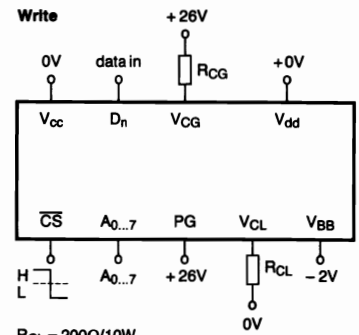
458 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 458 D	Nip	28-DIC	NMOS	-10...+70	935		<450		TTL-TS

Read



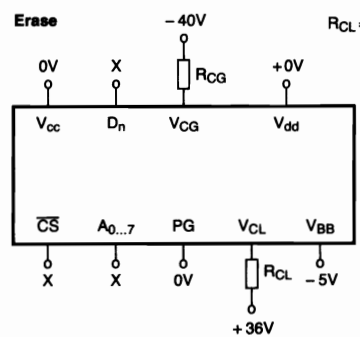
R_{CG} = 10KΩ/¼W

Write

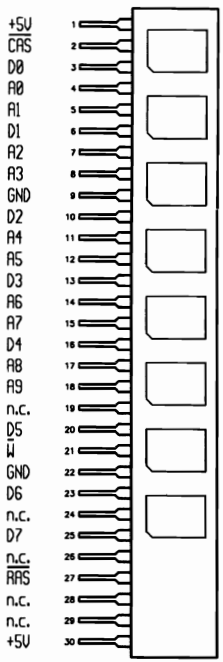


R_{CL} = 200Ω/10W

Erase

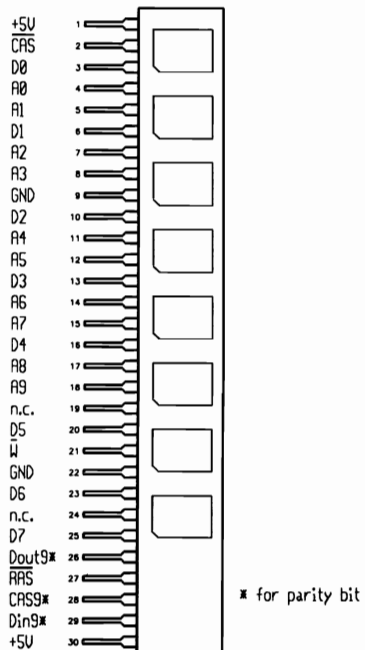


1000 — 1048576x8-Bit dynamic RAM-Modul



1000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 481000-10	Sam	30-SIP	NMOS	0...+70			<100	<8	TTL-TS
KMM 481000-12	Sam	30-SIP	NMOS	0...+70			<120	<8	TTL-TS
KMM 581000-10	Sam	30-SIC	NMOS	0...+70			<100	<8	TTL-TS
KMM 581000-12	Sam	30-SIC	NMOS	0...+70			<120	<8	TTL-TS
THM 81000 L-10	Tos	30-SIP	CMOS	0...+70	<2640	<44	<100	<8	TTL-TS
THM 81000 L-12	Tos	30-SIP	CMOS	0...+70	<2200	<44	<120	<8	TTL-TS
THM 81000 S-10	Tos	30-SIC	CMOS	0...+70	<2640	<44	<100	<8	TTL-TS
THM 81000 S-12	Tos	30-SIC	CMOS	0...+70	<2200	<44	<120	<8	TTL-TS

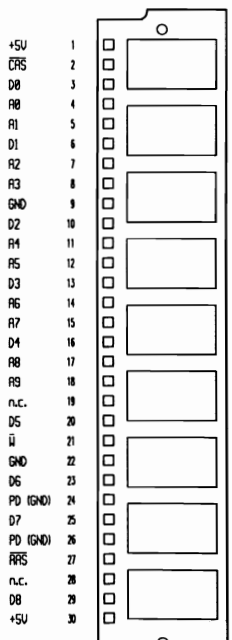
1000 — 1048576x9-Bit dynamic RAM-Modul



1000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYM 91000 L-60	Sie	30-SIP	NMOS	0...+70	<4455	<99	<60	<8	TTL-TS
HYM 91000 L-70	Sie	30-SIP	NMOS	0...+70	<3960	<99	<70	<8	TTL-TS
HYM 91000 L-80	Sie	30-SIP	NMOS	0...+70	<3465	<99	<80	<8	TTL-TS
HYM 91000 LL-60	Sie	30-SIP	NMOS	0...+70	<4455	<99	<60	<64	TTL-TS
HYM 91000 LL-70	Sie	30-SIP	NMOS	0...+70	<3960	<99	<70	<64	TTL-TS
HYM 91000 S-60	Sie	30-SIC	NMOS	0...+70	<4455	<99	<60	<8	TTL-TS
HYM 91000 S-70	Sie	30-SIC	NMOS	0...+70	<3960	<99	<70	<8	TTL-TS
HYM 91000 S-80	Sie	30-SIC	NMOS	0...+70	<3465	<99	<80	<8	TTL-TS
HYM 91000 SL-60	Sie	30-SIC	NMOS	0...+70	<4455	<99	<60	<64	TTL-TS
HYM 91000 SL-70	Sie	30-SIC	NMOS	0...+70	<3960	<99	<70	<64	TTL-TS
KMM 491000-10	Sam	30-SIP	NMOS	0...+70			<100	<8	TTL-TS
KMM 491000-12	Sam	30-SIP	NMOS	0...+70			<120	<8	TTL-TS
KMM 591000-10	Sam	30-SIC	NMOS	0...+70			<100	<8	TTL-TS
KMM 591000-12	Sam	30-SIC	NMOS	0...+70			<120	<8	TTL-TS
THM 91000 L-10	Tos	30-SIP	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91000 L-12	Tos	30-SIP	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS
THM 91000 S-10	Tos	30-SIC	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91000 S-12	Tos	30-SIC	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS

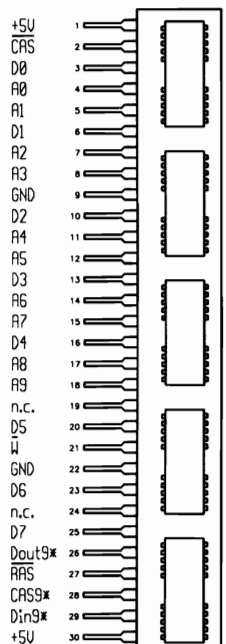
1000

1048576x9-Bit dyn. RAM-Modul (page mode)



1000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 91010 S-10	Tos	30-SIC	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91010 S-12	Tos	30-SIC	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS

1000	1048576x9-Bit dyn. RAM-Modul (page mode)

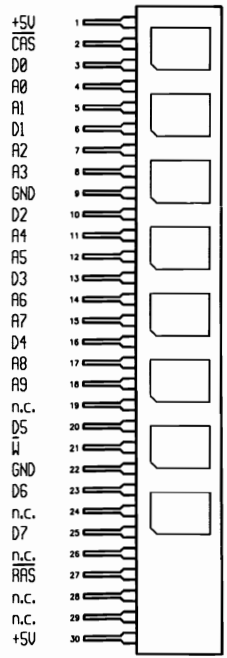


* for parity bit

1000 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 91020 L-10	Tos	30-SIP	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91020 L-12	Tos	30-SIP	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS

1001

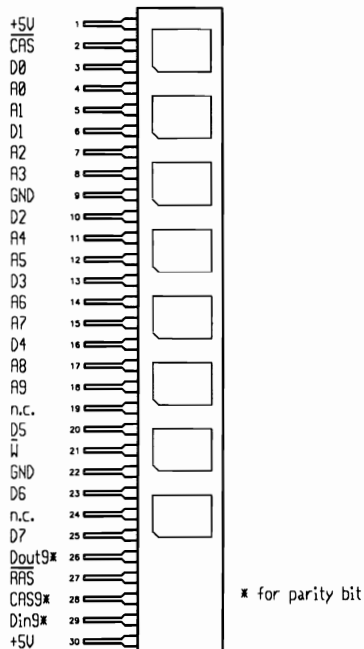
1048576x8-Bit dyn. RAM-Modul (nibble m.)



1001 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 481001-10	Sam	30-SIP	NMOS	0...+70			<100	<8	TTL-TS
KMM 481001-12	Sam	30-SIP	NMOS	0...+70			<120	<8	TTL-TS
KMM 581001-10	Sam	30-SIC	NMOS	0...+70			<100	<8	TTL-TS
KMM 581001-12	Sam	30-SIC	NMOS	0...+70			<120	<8	TTL-TS
THM 81001 L-10	Tos	30-SIP	CMOS	0...+70	<2640	<44	<100	<8	TTL-TS
THM 81001 L-12	Tos	30-SIP	CMOS	0...+70	<2200	<44	<120	<8	TTL-TS
THM 81001 S-10	Tos	30-SIC	CMOS	0...+70	<2640	<44	<100	<8	TTL-TS
THM 81001 S-12	Tos	30-SIC	CMOS	0...+70	<2200	<44	<120	<8	TTL-TS

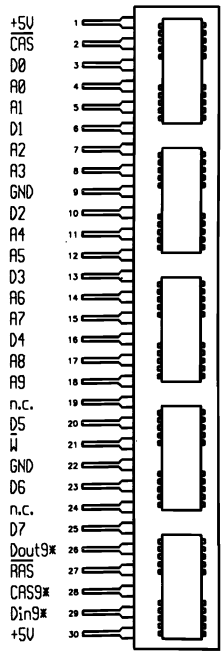
1001

1048576x9-Bit dyn. RAM-Modul (nibble m.)



1001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 491001-10	Sam	30-SIP	NMOS	0...+70			<100	<8	TTL-TS
KMM 491001-12	Sam	30-SIP	NMOS	0...+70			<120	<8	TTL-TS
KMM 591001-10	Sam	30-SIC	NMOS	0...+70			<100	<8	TTL-TS
KMM 591001-12	Sam	30-SIC	NMOS	0...+70			<120	<8	TTL-TS
THM 91001 L-10	Tos	30-SIP	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91001 L-12	Tos	30-SIP	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS
THM 91001 S-10	Tos	30-SIC	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91001 S-12	Tos	30-SIC	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS

1001 — 1048576x9-Bit dyn. RAM-Modul (nibble m.)

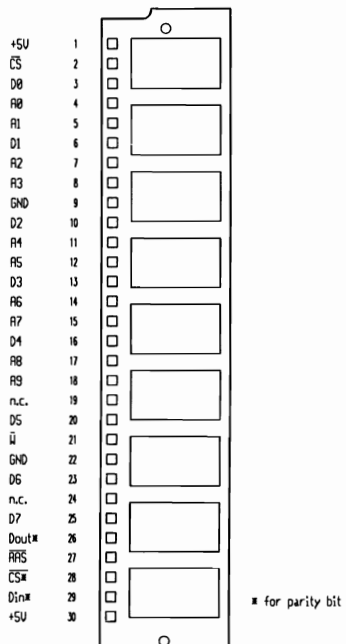


* for parity bit

1001 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 91021 L-10	Tos	30-SIP	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91021 L-12	Tos	30-SIP	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS

1002

1048576x9-Bit dyn. RAM-Modul (static c.)

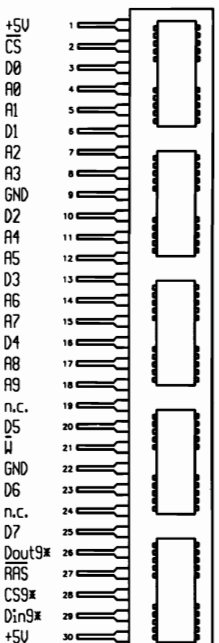


* for parity bit

1002 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 91002 L-10	Tos	30-SIP	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91002 L-12	Tos	30-SIP	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS
THM 91002 S-10	Tos	30-SIC	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91002 S-12	Tos	30-SIC	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS

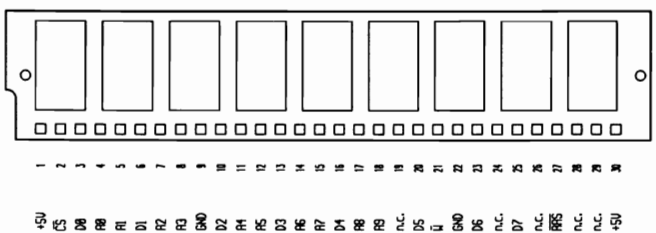
1002 — 1048576x9-Bit dyn. RAM-Modul (static c.)

Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 91022 L-10	Tos	30-SIP	CMOS	0...+70	<2970	<49,5	<100	<8	TTL-TS
THM 91022 L-12	Tos	30-SIP	CMOS	0...+70	<2475	<49,5	<120	<8	TTL-TS



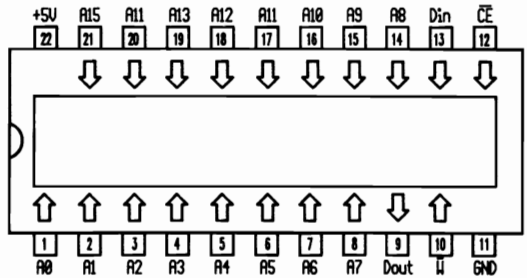
* for parity bit

1002 — 1048576x8-Bit dyn. RAM-Modul (static c.)



1600 — 65536x1-Bit statisches RAM

65536x1-Bit static RAM · 65536x1-Bit statique RAM
65536x1-Bit RAM statico · 65536x1-Bit estática RAM



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

1002 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 81002 L-10	Tos	30-SIP	CMOS	0...+70	<2640	<44	<100	<8	TTL-TS
THM 81002 L-12	Tos	30-SIP	CMOS	0...+70	<2200	<44	<120	<8	TTL-TS
THM 81002 S-10	Tos	30-SIC	CMOS	0...+70	<2640	<44	<100	<8	TTL-TS
THM 81002 S-12	Tos	30-SIC	CMOS	0...+70	<2200	<44	<120	<8	TTL-TS

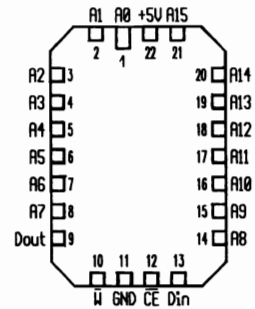
1600 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1600 DC-45	Fch	22-TDIC	CMOS	0...+70	<385	<27,5	<45		TTL-TS
F 1600 DC-55	Fch	22-TDIC	CMOS	0...+70	<385	<27,5	<55		TTL-TS
F 1600 DC-70	Fch	22-TDIC	CMOS	0...+70	<385	<27,5	<70		TTL-TS
F 1600 DM-55	Fch	22-TDIC	CMOS	-55...+125	<385	<49,5	<55		TTL-TS
F 1600 DM-70	Fch	22-TDIC	CMOS	-55...+125	<385	<49,5	<70		TTL-TS
F 1600 PC-45	Fch	22-TDIP	CMOS	0...+70	<385	<27,5	<45		TTL-TS
F 1600 PC-55	Fch	22-TDIP	CMOS	0...+70	<385	<27,5	<55		TTL-TS
F 1600 PC-70	Fch	22-TDIP	CMOS	0...+70	<385	<27,5	<70		TTL-TS

1600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6287 LP-45	Hit	22-DIP	CMOS	0...+70	<550	<0,55	<45		TTL-TS
HM 6287 LP-55	Hit	22-DIP	CMOS	0...+70	<550	<0,55	<55		TTL-TS
HM 6287 LP-70	Hit	22-DIP	CMOS	0...+70	<550	<0,55	<70		TTL-TS
HM 6287 P-45	Hit	22-DIP	CMOS	0...+70	<550	<11	<45		TTL-TS
HM 6287 P-55	Hit	22-DIP	CMOS	0...+70	<550	<11	<55		TTL-TS
HM 6287 P-70	Hit	22-DIP	CMOS	0...+70	<550	<11	<70		TTL-TS
HM 6787	Hit	22-TDIP	CMOS	0...+70	<550	<110	<25		TTL-TS
HM 6787-30	Hit	22-TDIP	CMOS	0...+70	<550	<110	<30		TTL-TS
HM1 65687 -2	Mhs	22-DIC	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
HM1 65687 -5	Mhs	22-DIC	CMOS	0...+70	<275	<55	<45		TTL-TS
HM1 65687 -9	Mhs	22-DIC	CMOS	-40...+85	<412,5	<82,5	<55		TTL-TS
HM1 65687 B-2	Mhs	22-DIC	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
HM1 65687 B-5	Mhs	22-DIC	CMOS	0...+70	<275	<55	<35		TTL-TS
HM1 65687 B-9	Mhs	22-DIC	CMOS	-40...+85	<412,5	<82,5	<45		TTL-TS
HM1 65687 C-2	Mhs	22-DIC	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM1 65687 C-5	Mhs	22-DIC	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS
HM1 65687 C-9	Mhs	22-DIC	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM1 65687 S-2	Mhs	22-DIC	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM1 65687 S-5	Mhs	22-DIC	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
HM1 65687 S-9	Mhs	22-DIC	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM1 65787 H-5	Mhs	22-DIC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM1 65787 K-2	Mhs	22-DIC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM1 65787 K-5	Mhs	22-DIC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM1 65787 K-9	Mhs	22-DIC	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM1 65787 M-2	Mhs	22-DIC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM1 65787 M-5	Mhs	22-DIC	CMOS	0...+70	<275	<165	<45		TTL-TS
HM1 65787 M-9	Mhs	22-DIC	CMOS	-40...+85	<385	<165	<45		TTL-TS
HM3 65687 -2	Mhs	22-TDIP	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
HM3 65687 -5	Mhs	22-TDIP	CMOS	0...+70	<275	<55	<45		TTL-TS
HM3 65687 -9	Mhs	22-TDIP	CMOS	-40...+85	<412,5	<82,5	<55		TTL-TS
HM3 65687 B-2	Mhs	22-TDIP	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
HM3 65687 B-5	Mhs	22-TDIP	CMOS	0...+70	<275	<55	<35		TTL-TS
HM3 65687 B-9	Mhs	22-TDIP	CMOS	-40...+85	<412,5	<82,5	<45		TTL-TS
HM3 65687 C-2	Mhs	22-TDIP	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM3 65687 C-5	Mhs	22-TDIP	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS
HM3 65687 C-9	Mhs	22-TDIP	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM3 65687 S-2	Mhs	22-TDIP	CMOS	-55...+125	<550	<110	<45		TTL-TS

1600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM3 65687 S-5	Mhs	22-TDIP	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
HM3 65687 S-9	Mhs	22-TDIP	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM3 65787 H-5	Mhs	22-DIP	CMOS	0...+70	<385	<165	<25		TTL-TS
HM3 65787 K-2	Mhs	22-DIP	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM3 65787 K-5	Mhs	22-DIP	CMOS	0...+70	<385	<165	<35		TTL-TS
HM3 65787 K-9	Mhs	22-DIP	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM3 65787 M-2	Mhs	22-DIP	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM3 65787 M-5	Mhs	22-DIP	CMOS	0...+70	<275	<165	<45		TTL-TS
HM3 65787 M-9	Mhs	22-DIP	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1600 LS-45M	Inm	22-DIC	CMOS	-55...+125	<385	<110	<45		TTL-TS
IMS 1600 LS-55M	Inm	22-DIC	CMOS	-55...+125	<385	<110	<55		TTL-TS
IMS 1600 LS-70M	Inm	22-DIC	CMOS	-55...+125	<385	<110	<70		TTL-TS
IMS 1600 P-25	Inm	22-DIP	CMOS	0...+70	<423,5	<137,5	<25		TTL-TS
IMS 1600 P-30	Inm	22-DIP	CMOS	0...+70	<423,5	<137,5	<30		TTL-TS
IMS 1600 P-35	Inm	22-DIP	CMOS	0...+70	<385	<137,5	<35		TTL-TS
IMS 1600 P-45	Inm	22-DIP	CMOS	0...+70	<385	<137,5	<45		TTL-TS
IMS 1600 P-55	Inm	22-DIP	CMOS	0...+70	<385	<137,5	<55		TTL-TS
IMS 1600 S-25	Inm	22-DIC	CMOS	0...+70	<423,5	<137,5	<25		TTL-TS
IMS 1600 S-30	Inm	22-DIC	CMOS	0...+70	<423,5	<137,5	<30		TTL-TS
IMS 1600 S-35	Inm	22-DIC	CMOS	0...+70	<385	<137,5	<35		TTL-TS
IMS 1600 S-45	Inm	22-DIC	CMOS	0...+70	<385	<137,5	<45		TTL-TS
IMS 1600 S-45M	Inm	22-DIC	CMOS	-55...+125	<385	<137,5	<45		TTL-TS
IMS 1600 S-55	Inm	22-DIC	CMOS	0...+70	<385	<137,5	<55		TTL-TS
IMS 1600 S-55M	Inm	22-DIC	CMOS	-55...+125	<385	<137,5	<55		TTL-TS
IMS 1600 S-70M	Inm	22-DIC	CMOS	-55...+125	<385	<137,5	<70		TTL-TS
M5M 5187 AP-25	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<25		TTL-TS
M5M 5187 AP-35	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<35		TTL-TS
M5M 5187 AP-45	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<45		TTL-TS
M5M 5187 AP-55	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<55		TTL-TS
M5M 5187 BP-15	Mit	22-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
M5M 5187 BP-20	Mit	22-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
M5M 5187 BP-25	Mit	22-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
MCM 6287 P-25	Mot	22-DIP	CMOS	0...+70	<660	<110	<25		TTL-TS
MCM 6287 P-35	Mot	22-DIP	CMOS	0...+70	<605	<110	<35		TTL-TS
MK 41H87 N-25	Sgs	22-DIP	CMOS	0...+70	<385	<44	<25		TTL-TS
MK 41H87 N-35	Sgs	22-DIP	CMOS	0...+70	<385	<44	<35		TTL-TS
MK 41H87 N-45	Sgs	22-DIP	CMOS	0...+70	<385	<44	<45		TTL-TS

1600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 5561 P-45	Tos	22-TDIP	CMOS	0...+70	<550	<5,5	<45		TTL-TS
TC 5561 P-55	Tos	22-TDIP	CMOS	0...+70	<550	<5,5	<55		TTL-TS
TC 5561 P-70	Tos	22-TDIP	CMOS	0...+70	<550	<5,5	<70		TTL-TS
TC 5562 P-35	Tos	22-TDIP	CMOS	0...+70	<550	<110	<35		TTL-TS
TC 5562 P-45	Tos	22-TDIP	CMOS	0...+70	<550	<110	<45		TTL-TS
TC 5562 P-55	Tos	22-TDIP	CMOS	0...+70	<550	<110	<55		TTL-TS
6287-35 BXAJC	Mot	22-TDIC	CMOS	-55...+125	<660	<27,5	<35		TTL-TS
6287-45 BXAJC	Mot	22-TDIC	CMOS	-55...+125	<660	<27,5	<45		TTL-TS

1600 — 65536x1-Bit static RAM

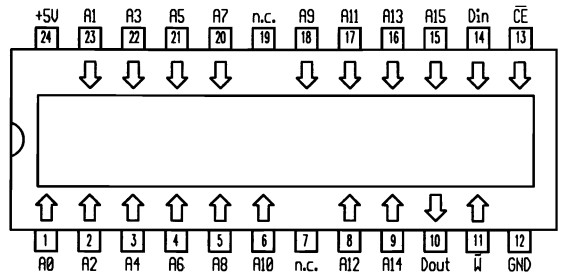


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

1600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1600 LC-45	Fch	22-LCC	CMOS	0...+70	<385	<27,5	<45		TTL-TS
F 1600 LC-55	Fch	22-LCC	CMOS	0...+70	<385	<27,5	<55		TTL-TS
F 1600 LC-70	Fch	22-LCC	CMOS	0...+70	<385	<27,5	<70		TTL-TS
F 1600 LM-55	Fch	22-LCC	CMOS	-55...+125	<385	<49,5	<55		TTL-TS
F 1600 LM-70	Fch	22-LCC	CMOS	-55...+125	<385	<49,5	<70		TTL-TS
HM 6287 CG-45	Hit	22-LCC	CMOS	0...+70	<550	<11	<45		TTL-TS
HM 6287 CG-55	Hit	22-LCC	CMOS	0...+70	<550	<11	<55		TTL-TS
HM 6287 CG-70	Hit	22-LCC	CMOS	0...+70	<550	<11	<70		TTL-TS

1600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6787 CG	Hit	22-LCC	CMOS	0...+70	<550	<110	<25		TTL-TS
HM 6787 CG-30	Hit	22-LCC	CMOS	0...+70	<550	<110	<30		TTL-TS
HM4 65687 -2	Mhs	22-LCC	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
HM4 65687 -5	Mhs	22-LCC	CMOS	0...+70	<275	<55	<45		TTL-TS
HM4 65687 -9	Mhs	22-LCC	CMOS	-40...+85	<412,5	<82,5	<55		TTL-TS
HM4 65687 B-2	Mhs	22-LCC	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
HM4 65687 B-5	Mhs	22-LCC	CMOS	0...+70	<275	<55	<35		TTL-TS
HM4 65687 B-9	Mhs	22-LCC	CMOS	-40...+85	<412,5	<82,5	<45		TTL-TS
HM4 65687 C-2	Mhs	22-LCC	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM4 65687 C-5	Mhs	22-LCC	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS
HM4 65687 C-9	Mhs	22-LCC	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM4 65687 S-2	Mhs	22-LCC	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM4 65687 S-5	Mhs	22-LCC	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
HM4 65687 S-9	Mhs	22-LCC	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM4 65787 H-5	Mhs	22-LCC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM4 65787 K-2	Mhs	22-LCC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM4 65787 K-5	Mhs	22-LCC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM4 65787 K-9	Mhs	22-LCC	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM4 65787 M-2	Mhs	22-LCC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM4 65787 M-5	Mhs	22-LCC	CMOS	0...+70	<275	<165	<45		TTL-TS
HM4 65787 M-9	Mhs	22-LCC	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1600 LN-45M	Inm	22-LCC	CMOS	-55...+125	<385	<110	<45		TTL-TS
IMS 1600 LN-55M	Inm	22-LCC	CMOS	-55...+125	<385	<110	<55		TTL-TS
IMS 1600 LN-70M	Inm	22-LCC	CMOS	-55...+125	<385	<110	<70		TTL-TS
IMS 1600 N-45M	Inm	22-LCC	CMOS	-55...+125	<385	<137,5	<45		TTL-TS
IMS 1600 N-55M	Inm	22-LCC	CMOS	-55...+125	<385	<137,5	<55		TTL-TS
IMS 1600 N-70M	Inm	22-LCC	CMOS	-55...+125	<385	<137,5	<70		TTL-TS
IMS 1600 W-25	Inm	22-LCC	CMOS	0...+70	<423,5	<137,5	<25		TTL-TS
IMS 1600 W-30	Inm	22-LCC	CMOS	0...+70	<423,5	<137,5	<30		TTL-TS
IMS 1600 W-35	Inm	22-LCC	CMOS	0...+70	<385	<137,5	<35		TTL-TS
IMS 1600 W-45	Inm	22-LCC	CMOS	0...+70	<385	<137,5	<45		TTL-TS
IMS 1600 W-55	Inm	22-LCC	CMOS	0...+70	<385	<137,5	<55		TTL-TS
6287-35 BUAJC	Mot	22-LCC	CMOS	-55...+125	<660	<27,5	<35		TTL-TS
6287-45 BUAJC	Mot	22-LCC	CMOS	-55...+125	<660	<27,5	<45		TTL-TS

1600 — 65363x1-Bit static RAM

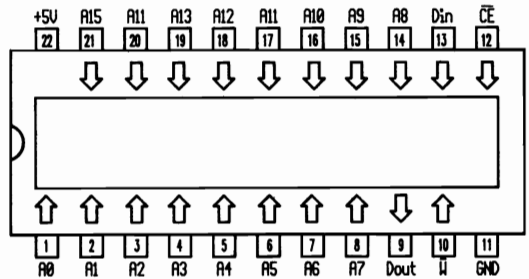


$\overline{CS}$	$\overline{W}$	D_{In}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

1600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HMT 65687 -2	Mhs	24-FLAT	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
HMT 65687 -5	Mhs	24-FLAT	CMOS	0...+70	<275	<55	<45		TTL-TS
HMT 65687 -9	Mhs	24-FLAT	CMOS	-40...+85	<412,5	<82,5	<55		TTL-TS
HMT 65687 B-2	Mhs	24-FLAT	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
HMT 65687 B-5	Mhs	24-FLAT	CMOS	0...+70	<275	<55	<35		TTL-TS
HMT 65687 B-9	Mhs	24-FLAT	CMOS	-40...+85	<412,5	<82,5	<45		TTL-TS
HMT 65687 C-2	Mhs	24-FLAT	CMOS	-55...+125	<550	<110	<55		TTL-TS
HMT 65687 C-5	Mhs	24-FLAT	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS

1600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HMT 65687 C-9	Mhs	24-FLAT	CMOS	-40...+85	<550	<110	<55		TTL-TS
HMT 65687 S-2	Mhs	24-FLAT	CMOS	-55...+125	<550	<110	<45		TTL-TS
HMT 65687 S-5	Mhs	24-FLAT	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
HMT 65687 S-9	Mhs	24-FLAT	CMOS	-40...+85	<550	<110	<45		TTL-TS
HMT 65787 H-5	Mhs	24-FLAT	CMOS	0...+70	<385	<165	<25		TTL-TS
HMT 65787 K-2	Mhs	24-FLAT	CMOS	-55...+125	<385	<165	<35		TTL-TS
HMT 65787 K-5	Mhs	24-FLAT	CMOS	0...+70	<385	<165	<35		TTL-TS
HMT 65787 K-9	Mhs	24-FLAT	CMOS	-40...+85	<385	<165	<35		TTL-TS
HMT 65787 M-2	Mhs	24-FLAT	CMOS	-55...+125	<385	<165	<45		TTL-TS
HMT 65787 M-5	Mhs	24-FLAT	CMOS	0...+70	<275	<165	<45		TTL-TS
HMT 65787 M-9	Mhs	24-FLAT	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1600 E-25	Inm	24-FLAT	CMOS	0...+70	<423,5	<137,5	<25		TTL-TS
IMS 1600 E-30	Inm	24-FLAT	CMOS	0...+70	<423,5	<137,5	<30		TTL-TS
IMS 1600 E-35	Inm	24-FLAT	CMOS	0...+70	<385	<137,5	<35		TTL-TS
IMS 1600 E-45	Inm	24-FLAT	CMOS	0...+70	<385	<137,5	<45		TTL-TS
IMS 1600 E-55	Inm	24-FLAT	CMOS	0...+70	<385	<137,5	<55		TTL-TS
M5M 5187 AJ-25	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<25		TTL-TS
M5M 5187 AJ-35	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<35		TTL-TS
M5M 5187 AJ-45	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<45		TTL-TS
M5M 5187 AJ-55	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<55		TTL-TS
M5M 5187 BJ-15	Mit	24-FLAT	CMOS	0...+70	<550	<220	<15		TTL-TS
M5M 5187 BJ-20	Mit	24-FLAT	CMOS	0...+70	<550	<220	<20		TTL-TS
M5M 5187 BJ-25	Mit	24-FLAT	CMOS	0...+70	<550	<220	<25		TTL-TS
MCM 6287 J-25	Mot	24-FLAT	CMOS	0...+70	<660	<110	<25		TTL-TS
MCM 6287 J-35	Mot	24-FLAT	CMOS	0...+70	<605	<110	<35		TTL-TS
TC 5561 J-45	Tos	24-FLAT	CMOS	0...+70	<550	<5,5	<45		TTL-TS
TC 5561 J-55	Tos	24-FLAT	CMOS	0...+70	<550	<5,5	<55		TTL-TS
TC 5561 J-70	Tos	24-FLAT	CMOS	0...+70	<550	<5,5	<70		TTL-TS
TC 5562 J-35	Tos	24-FLAT	CMOS	0...+70	<550	<110	<35		TTL-TS
TC 5562 J-45	Tos	24-FLAT	CMOS	0...+70	<550	<110	<45		TTL-TS
TC 5562 J-55	Tos	24-FLAT	CMOS	0...+70	<550	<110	<55		TTL-TS

1601 — 65536x1-Bit static RAM

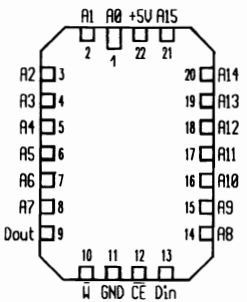


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

1601 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1601 DC-45	Fch	22-TDIC	CMOS	0...+70	<385	<11	<45		TTL-TS
F 1601 DC-55	Fch	22-TDIC	CMOS	0...+70	<385	<11	<55		TTL-TS
F 1601 DC-70	Fch	22-TDIC	CMOS	0...+70	<385	<11	<70		TTL-TS
F 1601 DM-55	Fch	22-TDIC	CMOS	-55...+125	<385	<49,5	<55		TTL-TS
F 1601 DM-70	Fch	22-TDIC	CMOS	-55...+125	<385	<49,5	<70		TTL-TS
F 1601 PC-45	Fch	22-TDIP	CMOS	0...+70	<385	<11	<45		TTL-TS
F 1601 PC-55	Fch	22-TDIP	CMOS	0...+70	<385	<11	<55		TTL-TS
F 1601 PC-70	Fch	22-TDIP	CMOS	0...+70	<385	<11	<70		TTL-TS

1601 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1601 LP-35	Inm	22-DIP	CMOS	0...+70	<385	<82,5	<35		TTL-TS
IMS 1601 LP-45	Inm	22-DIP	CMOS	0...+70	<385	<82,5	<45		TTL-TS
IMS 1601 LP-55	Inm	22-DIP	CMOS	0...+70	<385	<82,5	<55		TTL-TS
IMS 1601 LS-35	Inm	22-DIC	CMOS	0...+70	<385	<82,5	<35		TTL-TS
IMS 1601 LS-45	Inm	22-DIC	CMOS	0...+70	<385	<82,5	<45		TTL-TS
IMS 1601 LS-55	Inm	22-DIC	CMOS	0...+70	<385	<82,5	<55		TTL-TS

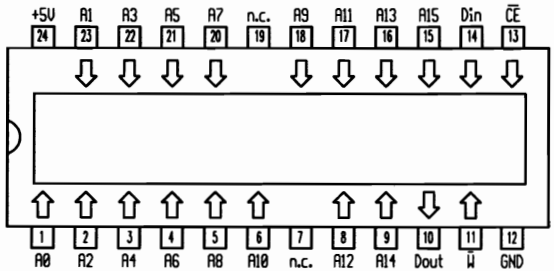
1601 — 65536x1-Bit static RAM



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

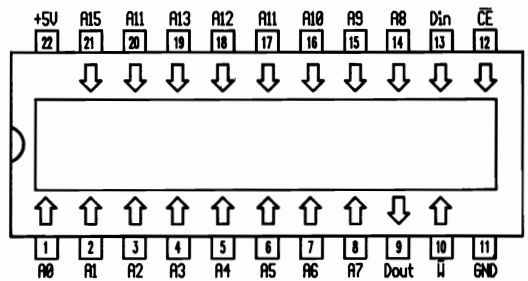
1601 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1601 LC-45	Fch	22-LCC	CMOS	0...+70	<385	<11	<45		TTL-TS
F 1601 LC-55	Fch	22-LCC	CMOS	0...+70	<385	<11	<55		TTL-TS
F 1601 LC-70	Fch	22-LCC	CMOS	0...+70	<385	<11	<70		TTL-TS
F 1601 LM-55	Fch	22-LCC	CMOS	-55...+125	<385	<49,5	<55		TTL-TS
F 1601 LM-70	Fch	22-LCC	CMOS	-55...+125	<385	<49,5	<70		TTL-TS
IMS 1601 LW-35	Inm	22-LCC	CMOS	0...+70	<385	<82,5	<35		TTL-TS
IMS 1601 LW-45	Inm	22-LCC	CMOS	0...+70	<385	<82,5	<45		TTL-TS
IMS 1601 LW-55	Inm	22-LCC	CMOS	0...+70	<385	<82,5	<55		TTL-TS

1601 — 65536x1-Bit static RAM



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

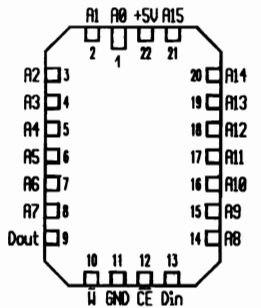
1605 — 65536x4-Bit static RAM



1601 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1601 LE-35	Inm	24-FLAT	CMOS	0...+70	<385	<82,5	<35		TTL-TS
IMS 1601 LE-45	Inm	24-FLAT	CMOS	0...+70	<385	<82,5	<45		TTL-TS
IMS 1601 LE-55	Inm	24-FLAT	CMOS	0...+70	<385	<82,5	<55		TTL-TS

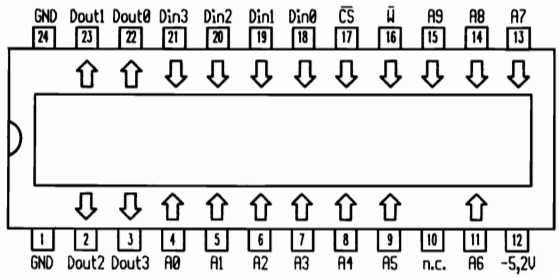
1605 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1605 P-15	Inm	22-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1605 P-20	Inm	22-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1605 P-25	Inm	22-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1605 S-15	Inm	22-DIC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1605 S-20	Inm	22-DIC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1605 S-25	Inm	22-DIC	CMOS	0...+70	<550	<220	<25		TTL-TS

1605 — 65536x4-Bit static RAM



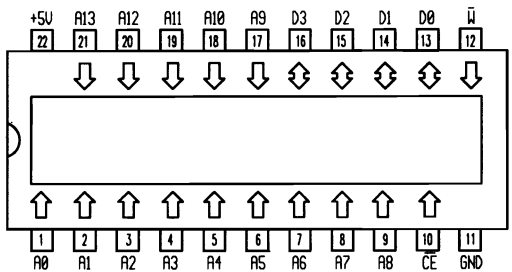
1605 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1605 W-15	Inm	22-LCC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1605 W-20	Inm	22-LCC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1605 W-25	Inm	22-LCC	CMOS	0...+70	<550	<220	<25		TTL-TS

1605 — 65536x4-Bit static RAM



1605 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1605 E-15	Inm	24-FLAT	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1605 E-20	Inm	24-FLAT	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1605 E-25	Inm	24-FLAT	CMOS	0...+70	<550	<220	<25		TTL-TS

1620 — 16384x4-Bit static RAM

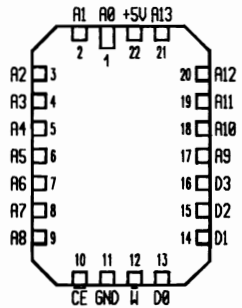


$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

1620 Type	Man	Case	Techn.	TU°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1620 DC	Fch	22-TDIC	CMOS	0...+70	<385	<110	<35		TTL-TS
F 1620 DM	Fch	22-TDIC	CMOS	-55...+125	<385	<110	<45		TTL-TS
HM 6288 P-35	Hit	22-DIP	CMOS	0...+70	330	<11	<35		TTL-TS
HM 6288 P-45	Hit	22-DIP	CMOS	0...+70	330	<11	<45		TTL-TS
HM 6288 P-55	Hit	22-DIP	CMOS	0...+70	330	<11	<55		TTL-TS
HM 6788	Hit	22-TDIP	CMOS	0...+70	<660	<55	<30		TTL-TS
HM1 65788 H-5	Mhs	22-DIC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM1 65788 K-2	Mhs	22-DIC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM1 65788 K-5	Mhs	22-DIC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM1 65788 K-9	Mhs	22-DIC	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM1 65788 M-2	Mhs	22-DIC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM1 65788 M-5	Mhs	22-DIC	CMOS	0...+70	<275	<165	<45		TTL-TS
HM1 65788 M-9	Mhs	22-DIC	CMOS	-40...+85	<385	<165	<45		TTL-TS
HM3 65788 H-5	Mhs	22-DIP	CMOS	0...+70	<385	<165	<25		TTL-TS
HM3 65788 K-2	Mhs	22-DIP	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM3 65788 K-5	Mhs	22-DIP	CMOS	0...+70	<385	<165	<35		TTL-TS
HM3 65788 K-9	Mhs	22-DIP	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM3 65788 M-2	Mhs	22-DIP	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM3 65788 M-5	Mhs	22-DIP	CMOS	0...+70	<275	<165	<45		TTL-TS
HM3 65788 M-9	Mhs	22-DIP	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1620 LS-45M	Inm	22-DIC	CMOS	-55...+125	<550	<110	<45		TTL-TS
IMS 1620 LS-55M	Inm	22-DIC	CMOS	-55...+125	<550	<110	<55		TTL-TS
IMS 1620 LS-70M	Inm	22-DIC	CMOS	-55...+125	<550	<110	<70		TTL-TS
IMS 1620 P-25	Inm	22-DIP	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1620 P-30	Inm	22-DIP	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1620 P-35	Inm	22-DIP	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1620 P-45	Inm	22-DIP	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1620 P-55	Inm	22-DIP	CMOS	0...+70	<550	<137,5	<55		TTL-TS
IMS 1620 S-25	Inm	22-DIC	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1620 S-30	Inm	22-DIC	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1620 S-35	Inm	22-DIC	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1620 S-45	Inm	22-DIC	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1620 S-45M	Inm	22-DIC	CMOS	-55...+125	<550	<165	<45		TTL-TS
IMS 1620 S-55	Inm	22-DIC	CMOS	0...+70	<550	<137,5	<55		TTL-TS
IMS 1620 S-55M	Inm	22-DIC	CMOS	-55...+125	<550	<165	<55		TTL-TS
IMS 1620 S-70M	Inm	22-DIC	CMOS	-55...+125	<550	<165	<70		TTL-TS
M5M 5188 AP-25	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<25		TTL-TS
M5M 5188 AP-35	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<35		TTL-TS
M5M 5188 AP-45	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<45		TTL-TS
M5M 5188 AP-55	Mit	22-DIP	CMOS	0...+70	<550	<137,5	<55		TTL-TS
M5M 5188 BP-15	Mit	22-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
M5M 5188 BP-20	Mit	22-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
M5M 5188 BP-25	Mit	22-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
MCM 6288 P-25	Mot	22-DIP	CMOS	0...+70	<660	<110	<25		TTL-TS
MCM 6288 P-30	Mot	22-DIP	CMOS	0...+70	<660	<110	<30		TTL-TS

1620 Type	Man	Case	Techn.	T_{Uj}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6288 P-35	Mot	22-DIP	CMOS	0...+70	<605	<110	<35		TTL-TS
TC 55416 P-25	Tos	22-DIP	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 55416 P-35	Tos	22-DIP	CMOS	0...+70	<550	<110	<35		TTL-TS
TC 55416 P-45	Tos	22-DIP	CMOS	0...+70	<550	<110	<45		TTL-TS
6288-35 BXAJC	Mot	22-TDIC	CMOS	-55...+125	<660	<27,5	<35		TTL-TS
6288-45 BXAJC	Mot	22-TDIC	CMOS	-55...+125	<660	<27,5	<45		TTL-TS

1620 — 16384x4-Bit static RAM

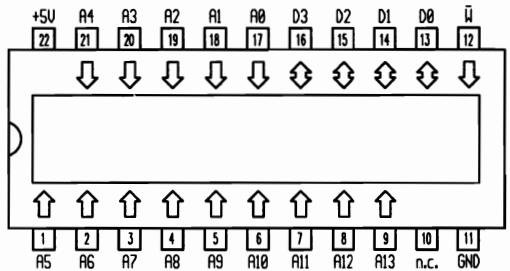


$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

1620 Type	Man	Case	Techn.	T_{Uj}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1620 LC	Fch	22-LCC	CMOS	0...+70	<385	<110	<35		TTL-TS
F 1620 LM	Fch	22-LCC	CMOS	-55...+125	<385	<110	<45		TTL-TS
HM4 65688 -2	Mhs	22-LCC	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HM4 65688 -5	Mhs	22-LCC	CMOS	0...+70	<275	<55	<45		TTL-TS
HM4 65688 -9	Mhs	22-LCC	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HM4 65688 B-2	Mhs	22-LCC	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HM4 65688 B-5	Mhs	22-LCC	CMOS	0...+70	<275	<55	<35		TTL-TS
HM4 65688 B-9	Mhs	22-LCC	CMOS	-40...+85	<412	<82,5	<45		TTL-TS

1620 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65688 C-2	Mhs	22-LCC	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM4 65688 C-5	Mhs	22-LCC	CMOS	0...+70	<412	<82,5	<45		TTL-TS
HM4 65688 C-9	Mhs	22-LCC	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM4 65688 S-2	Mhs	22-LCC	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM4 65688 S-5	Mhs	22-LCC	CMOS	0...+70	<412	<82,5	<35		TTL-TS
HM4 65688 S-9	Mhs	22-LCC	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM4 65788 H-5	Mhs	22-LCC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM4 65788 K-2	Mhs	22-LCC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM4 65788 K-5	Mhs	22-LCC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM4 65788 K-9	Mhs	22-LCC	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM4 65788 M-2	Mhs	22-LCC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM4 65788 M-5	Mhs	22-LCC	CMOS	0...+70	<275	<165	<45		TTL-TS
HM4 65788 M-9	Mhs	22-LCC	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1620 LN-45M	Inm	22-LCC	CMOS	-55...+125	<550	<110	<45		TTL-TS
IMS 1620 LN-55M	Inm	22-LCC	CMOS	-55...+125	<550	<110	<55		TTL-TS
IMS 1620 LN-70M	Inm	22-LCC	CMOS	-55...+125	<550	<110	<70		TTL-TS
IMS 1620 N-45M	Inm	22-LCC	CMOS	-55...+125	<550	<165	<45		TTL-TS
IMS 1620 N-55M	Inm	22-LCC	CMOS	-55...+125	<550	<165	<55		TTL-TS
IMS 1620 N-70M	Inm	22-LCC	CMOS	-55...+125	<550	<165	<70		TTL-TS
IMS 1620 W-25	Inm	22-LCC	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1620 W-30	Inm	22-LCC	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1620 W-35	Inm	22-LCC	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1620 W-45	Inm	22-LCC	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1620 W-55	Inm	22-LCC	CMOS	0...+70	<550	<137,5	<55		TTL-TS
6288-35 BUAJC	Mot	22-LCC	CMOS	-55...+125	<660	<27,5	<35		TTL-TS
6288-45 BUAJC	Mot	22-LCC	CMOS	-55...+125	<660	<27,5	<45		TTL-TS

1620 — 16384x4-Bit static RAM

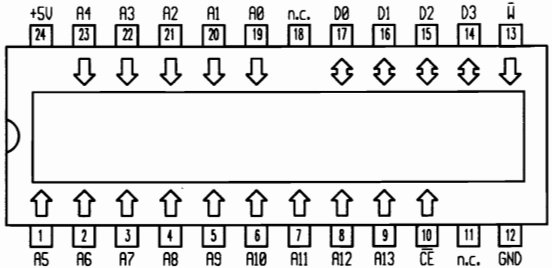


$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

1620 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65688 -2	Mhs	22-DIC	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HM1 65688 -5	Mhs	22-DIC	CMOS	0...+70	<275	<55	<45		TTL-TS
HM1 65688 -9	Mhs	22-DIC	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HM1 65688 B-2	Mhs	22-DIC	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HM1 65688 B-5	Mhs	22-DIC	CMOS	0...+70	<275	<55	<35		TTL-TS
HM1 65688 B-9	Mhs	22-DIC	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HM1 65688 C-2	Mhs	22-DIC	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM1 65688 C-5	Mhs	22-DIC	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS

1620 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65688 C-9	Mhs	22-DIC	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM1 65688 S-2	Mhs	22-DIC	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM1 65688 S-5	Mhs	22-DIC	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
HM1 65688 S-9	Mhs	22-DIC	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM3 65688 -2	Mhs	22-TDIP	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HM3 65688 -5	Mhs	22-TDIP	CMOS	0...+70	<275	<55	<45		TTL-TS
HM3 65688 -9	Mhs	22-TDIP	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HM3 65688 B-2	Mhs	22-TDIP	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
HM3 65688 B-5	Mhs	22-TDIP	CMOS	0...+70	<275	<55	<35		TTL-TS
HM3 65688 B-9	Mhs	22-TDIP	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HM3 65688 C-2	Mhs	22-TDIP	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM3 65688 C-5	Mhs	22-TDIP	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS
HM3 65688 C-9	Mhs	22-TDIP	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM3 65688 S-2	Mhs	22-TDIP	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM3 65688 S-5	Mhs	22-TDIP	CMOS	0...+70	<412	<82,5	<35		TTL-TS
HM3 65688 S-9	Mhs	22-TDIP	CMOS	-40...+85	<550	<110	<45		TTL-TS

1620 — 16384x4-Bit static RAM

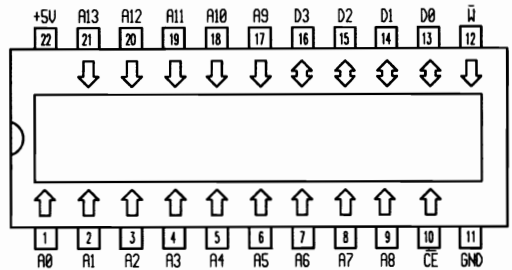


$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

1620 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HMT 65688 -2	Mhs	24-FLAT	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HMT 65688 -5	Mhs	24-FLAT	CMOS	0...+70	<275	<55	<45		TTL-TS
HMT 65688 -9	Mhs	24-FLAT	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HMT 65688 B-2	Mhs	24-FLAT	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HMT 65688 B-5	Mhs	24-FLAT	CMOS	0...+70	<275	<55	<35		TTL-TS
HMT 65688 B-9	Mhs	24-FLAT	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HMT 65688 C-2	Mhs	24-FLAT	CMOS	-55...+125	<550	<110	<55		TTL-TS
HMT 65688 C-5	Mhs	24-FLAT	CMOS	0...+70	<412	<82,5	<45		TTL-TS

1620 Type	Man	Case	Techn.	T$_U$°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HMT 65688 C-9	Mhs	24-FLAT	CMOS	-40...+85	<550	<110	<55		TTL-TS
HMT 65688 S-2	Mhs	24-FLAT	CMOS	-55...+125	<550	<110	<45		TTL-TS
HMT 65688 S-5	Mhs	24-FLAT	CMOS	0...+70	<412	<82,5	<35		TTL-TS
HMT 65688 S-9	Mhs	24-FLAT	CMOS	-40...+85	<550	<110	<45		TTL-TS
HMT 65788 H-5	Mhs	24-FLAT	CMOS	0...+70	<385	<165	<25		TTL-TS
HMT 65788 K-2	Mhs	24-FLAT	CMOS	-55...+125	<385	<165	<35		TTL-TS
HMT 65788 K-5	Mhs	24-FLAT	CMOS	0...+70	<385	<165	<35		TTL-TS
HMT 65788 K-9	Mhs	24-FLAT	CMOS	-40...+85	<385	<165	<35		TTL-TS
HMT 65788 M-2	Mhs	24-FLAT	CMOS	-55...+125	<385	<165	<45		TTL-TS
HMT 65788 M-5	Mhs	24-FLAT	CMOS	0...+70	<275	<165	<45		TTL-TS
HMT 65788 M-9	Mhs	24-FLAT	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1620 E-25	Inm	24-FLAT	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1620 E-30	Inm	24-FLAT	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1620 E-35	Inm	24-FLAT	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1620 E-45	Inm	24-FLAT	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1620 E-55	Inm	24-FLAT	CMOS	0...+70	<550	<137,5	<55		TTL-TS
M5M 5188 AJ-25	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<25		TTL-TS
M5M 5188 AJ-35	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<35		TTL-TS
M5M 5188 AJ-45	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<45		TTL-TS
M5M 5188 AJ-55	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<55		TTL-TS
M5M 5188 BJ-15	Mit	24-FLAT	CMOS	0...+70	<550	<220	<15		TTL-TS
M5M 5188 BJ-20	Mit	24-FLAT	CMOS	0...+70	<550	<220	<20		TTL-TS
M5M 5188 BJ-25	Mit	24-FLAT	CMOS	0...+70	<550	<220	<25		TTL-TS
TC 55416 J-25	Tos	24-FLAT	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 55416 J-35	Tos	24-FLAT	CMOS	0...+70	<550	<110	<35		TTL-TS
TC 55416 J-45	Tos	24-FLAT	CMOS	0...+70	<550	<110	<45		TTL-TS

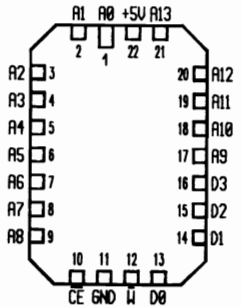
1621 — 16384x4-Bit static RAM



CE	W	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

1621 Type	Man	Case	Techn.	T$_U$°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1621 DC	Fch	22-TDIC	CMOS	0...+70	<385	<110	<35		TTL-TS
F 1621 DM	Fch	22-TDIC	CMOS	-55...+125	<385	<110	<45		TTL-TS

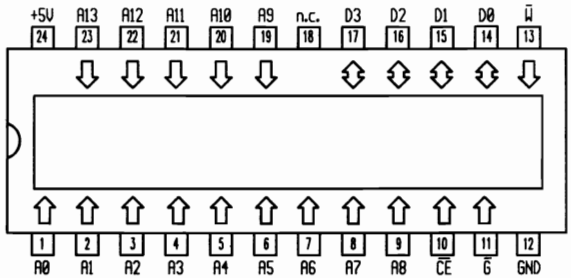
1621 — 16384x4-Bit static RAM



$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

1621 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1621 LC	Fch	22-LCC	CMOS	0...+70	<385	<110	<35		TTL-TS
F 1621 LM	Fch	22-LCC	CMOS	-55...+125	<385	<110	<45		TTL-TS

1622 — 16384x4-Bit static RAM

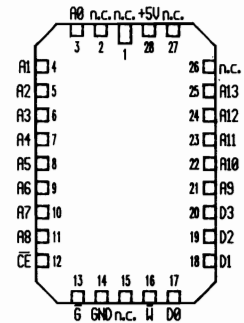


$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

1622 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1622 DC	Fch	24-TDIC	CMOS	0...+70	<495	<110	<35		TTL-TS
F 1622 DM	Fch	24-TDIC	CMOS	-55...+125	<495	<110	<45		TTL-TS
HM1 65789 H-5	Mhs	24-DIC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM1 65789 K-2	Mhs	24-DIC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM1 65789 K-5	Mhs	24-DIC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM1 65789 M-2	Mhs	24-DIC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM1 65789 M-5	Mhs	24-DIC	CMOS	0...+70	<275	<165	<45		TTL-TS
HM3 65789 H-5	Mhs	24-DIP	CMOS	0...+70	<385	<165	<25		TTL-TS

1622 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM3 65789 K-2	Mhs	24-DIP	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM3 65789 K-5	Mhs	24-DIP	CMOS	0...+70	<385	<165	<35		TTL-TS
HM3 65789 M-2	Mhs	24-DIP	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM3 65789 M-5	Mhs	24-DIP	CMOS	0...+70	<275	<165	<45		TTL-TS
HMT 65789 H-5	Mhs	24-FLAT	CMOS	0...+70	<385	<165	<25		TTL-TS
HMT 65789 K-2	Mhs	24-FLAT	CMOS	-55...+125	<385	<165	<35		TTL-TS
HMT 65789 K-5	Mhs	24-FLAT	CMOS	0...+70	<385	<165	<35		TTL-TS
HMT 65789 M-2	Mhs	24-FLAT	CMOS	-55...+125	<385	<165	<45		TTL-TS
HMT 65789 M-5	Mhs	24-FLAT	CMOS	0...+70	<275	<165	<45		TTL-TS
M5M 5189 AJ-25	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<25		TTL-TS
M5M 5189 AJ-35	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<35		TTL-TS
M5M 5189 AJ-45	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<45		TTL-TS
M5M 5189 AJ-55	Mit	24-FLAT	CMOS	0...+70	<550	<137,5	<55		TTL-TS
M5M 5189 AP-25	Mit	24-DIP	CMOS	0...+70	<550	<137,5	<25		TTL-TS
M5M 5189 AP-35	Mit	24-DIP	CMOS	0...+70	<550	<137,5	<35		TTL-TS
M5M 5189 AP-45	Mit	24-DIP	CMOS	0...+70	<550	<137,5	<45		TTL-TS
M5M 5189 AP-55	Mit	24-DIP	CMOS	0...+70	<550	<137,5	<55		TTL-TS
M5M 5189 BJ-15	Mit	24-FLAT	CMOS	0...+70	<550	<220	<15		TTL-TS
M5M 5189 BJ-20	Mit	24-FLAT	CMOS	0...+70	<550	<220	<20		TTL-TS
M5M 5189 BJ-25	Mit	24-FLAT	CMOS	0...+70	<550	<220	<25		TTL-TS
M5M 5189 BP-15	Mit	24-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
M5M 5189 BP-20	Mit	24-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
M5M 5189 BP-25	Mit	24-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
MCM 6290 J-25	Mot	24-FLAT	CMOS	0...+70	<660	<110	<25		TTL-TS
MCM 6290 J-30	Mot	24-FLAT	CMOS	0...+70	<660	<110	<30		TTL-TS
MCM 6290 J-35	Mot	24-FLAT	CMOS	0...+70	<605	<110	<35		TTL-TS
MCM 6290 P-25	Mot	24-TDIP	CMOS	0...+70	<660	<110	<25		TTL-TS
MCM 6290 P-30	Mot	24-TDIP	CMOS	0...+70	<660	<110	<30		TTL-TS
MCM 6290 P-35	Mot	24-TDIP	CMOS	0...+70	<605	<110	<35		TTL-TS
TC 55417 J-25	Tos	24-FLAT	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 55417 J-35	Tos	24-FLAT	CMOS	0...+70	<550	<110	<35		TTL-TS
TC 55417 J-45	Tos	24-FLAT	CMOS	0...+70	<550	<110	<45		TTL-TS
TC 55417 P-25	Tos	24-DIP	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 55417 P-35	Tos	24-DIP	CMOS	0...+70	<550	<110	<35		TTL-TS
TC 55417 P-45	Tos	24-DIP	CMOS	0...+70	<550	<110	<45		TTL-TS

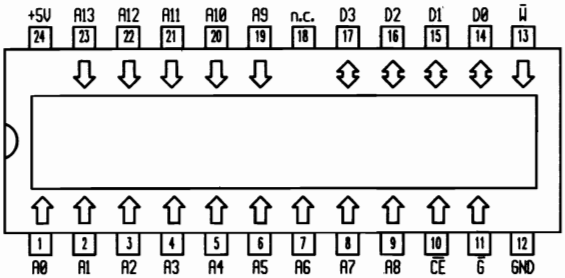
1622 — 16384x4-Bit static RAM



$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

1622 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1622 LC	Fch	28-LCC	CMOS	0...+70	<495	<110	<35		TTL-TS
F 1622 LM	Fch	28-LCC	CMOS	-55...+125	<495	<110	<45		TTL-TS
HM4 65789 H-5	Mhs	28-LCC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM4 65789 K-2	Mhs	28-LCC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM4 65789 K-5	Mhs	28-LCC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM4 65789 M-2	Mhs	28-LCC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM4 65789 M-5	Mhs	28-LCC	CMOS	0...+70	<275	<165	<45		TTL-TS

1623 — 16384x4-Bit static RAM

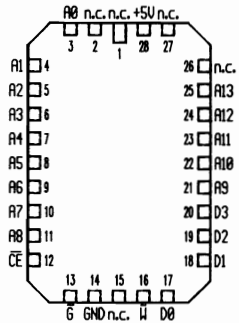


$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

1623 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1623 DC	Fch	24-TDIC	CMOS	0...+70	<495	<110	<35		TTL-TS
F 1623 DM	Fch	24-TDIC	CMOS	-55...+125	<495	<110	<45		TTL-TS
IMS 1624 E-25	Inm	24-FLAT	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1624 E-30	Inm	24-FLAT	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1624 E-35	Inm	24-FLAT	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1624 E-45	Inm	24-FLAT	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1624 E-55	Inm	24-FLAT	CMOS	0...+70	<550	<137,5	<55		TTL-TS
IMS 1624 LS-45M	Inm	24-DIC	CMOS	-55...+125	<550	<110	<45		TTL-TS
IMS 1624 LS-55M	Inm	24-DIC	CMOS	-55...+125	<550	<110	<55		TTL-TS
IMS 1624 LS-70M	Inm	24-DIC	CMOS	-55...+125	<550	<110	<70		TTL-TS
IMS 1624 P-25	Inm	24-DIP	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1624 P-30	Inm	24-DIP	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1624 P-35	Inm	24-DIP	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1624 P-45	Inm	24-DIP	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1624 P-55	Inm	24-DIP	CMOS	0...+70	<550	<137,5	<55		TTL-TS
IMS 1624 S-25	Inm	24-DIC	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1624 S-30	Inm	24-DIC	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1624 S-35	Inm	24-DIC	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1624 S-45	Inm	24-DIC	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1624 S-45M	Inm	24-DIC	CMOS	-55...+125	<550	<165	<45		TTL-TS
IMS 1624 S-55	Inm	24-DIC	CMOS	0...+70	<550	<137,5	<55		TTL-TS
IMS 1624 S-55M	Inm	24-DIC	CMOS	-55...+125	<550	<165	<55		TTL-TS
IMS 1624 S-70M	Inm	24-DIC	CMOS	-55...+125	<550	<165	<70		TTL-TS

1623

16384x4-Bit static RAM

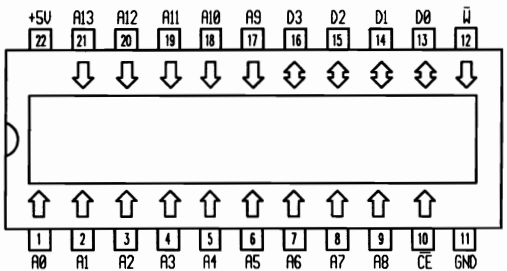


$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

1623 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 1623 LC	Fch	28-LCC	CMOS	0...+70	<495	<110	<35		TTL-TS
F 1623 LM	Fch	28-LCC	CMOS	-55...+125	<495	<110	<45		TTL-TS
IMS 1624 LN-45M	Inm	28-LCC	CMOS	-55...+125	<550	<110	<45		TTL-TS
IMS 1624 LN-55M	Inm	28-LCC	CMOS	-55...+125	<550	<110	<55		TTL-TS
IMS 1624 LN-70M	Inm	28-LCC	CMOS	-55...+125	<550	<110	<70		TTL-TS
IMS 1624 N-45M	Inm	28-LCC	CMOS	-55...+125	<550	<165	<45		TTL-TS
IMS 1624 N-55M	Inm	28-LCC	CMOS	-55...+125	<550	<165	<55		TTL-TS
IMS 1624 N-70M	Inm	28-LCC	CMOS	-55...+125	<550	<165	<70		TTL-TS

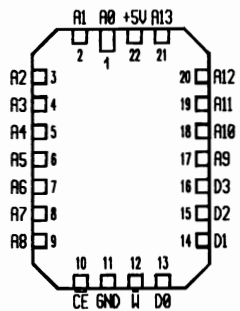
1623 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1624 W-25	Inm	28-LCC	CMOS	0...+70	<605	<137,5	<25		TTL-TS
IMS 1624 W-30	Inm	28-LCC	CMOS	0...+70	<605	<137,5	<30		TTL-TS
IMS 1624 W-35	Inm	28-LCC	CMOS	0...+70	<550	<137,5	<35		TTL-TS
IMS 1624 W-45	Inm	28-LCC	CMOS	0...+70	<550	<137,5	<45		TTL-TS
IMS 1624 W-55	Inm	28-LCC	CMOS	0...+70	<550	<137,5	<55		TTL-TS

1625 — 16384x4-Bit static RAM



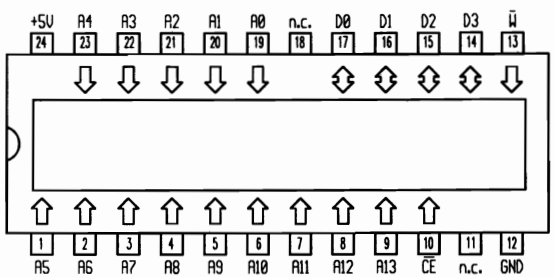
1625 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1625 P-15	Inm	22-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1625 P-20	Inm	22-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1625 P-25	Inm	22-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1625 S-15	Inm	22-DIC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1625 S-20	Inm	22-DIC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1625 S-25	Inm	22-DIC	CMOS	0...+70	<550	<220	<25		TTL-TS

1625 — 16384x4-Bit static RAM



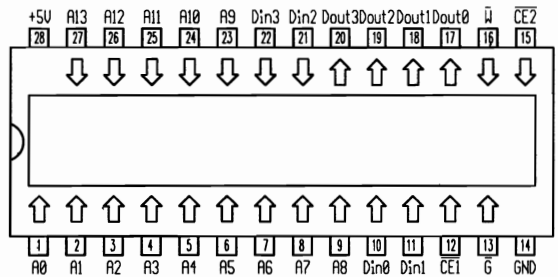
1625 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1625 W-15	Inm	22-LCC	CMOS	0...+70	<550	<210	<15		TTL-TS
IMS 1625 W-20	Inm	22-LCC	CMOS	0...+70	<550	<210	<20		TTL-TS
IMS 1625 W-25	Inm	22-LCC	CMOS	0...+70	<550	<210	<25		TTL-TS

1625 — 16384x4-Bit static RAM



1625 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1625 E-15	Inm	24-FLAT	CMOS	0...+70	<550	<210	<15		TTL-TS
IMS 1625 E-20	Inm	24-FLAT	CMOS	0...+70	<550	<210	<20		TTL-TS
IMS 1625 E-25	Inm	24-FLAT	CMOS	0...+70	<550	<210	<25		TTL-TS

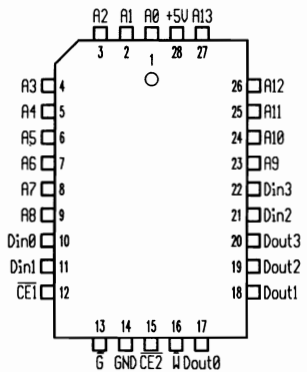
1626 — 16384x4-Bit static RAM



1626 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65790 H-5	Mhs	28-DIC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM1 65790 K-2	Mhs	28-DIC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM1 65790 K-5	Mhs	28-DIC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM1 65790 M-2	Mhs	28-DIC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM1 65790 M-5	Mhs	28-DIC	CMOS	0...+70	<275	<165	<45		TTL-TS
HM1 65791 H-5	Mhs	28-TDIC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM1 65791 K-2	Mhs	28-TDIC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM1 65791 K-5	Mhs	28-TDIC	CMOS	0...+70	<385	<165	<35		TTL-TS

1626 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65791 K-9	Mhs	28-TDIC	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM1 65791 M-2	Mhs	28-TDIC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM1 65791 M-5	Mhs	28-TDIC	CMOS	0...+70	<385	<165	<45		TTL-TS
HM1 65791 M-9	Mhs	28-TDIC	CMOS	-40...+85	<385	<165	<45		TTL-TS
HM3 65790 H-5	Mhs	28-DIP	CMOS	0...+70	<385	<165	<25		TTL-TS
HM3 65790 K-2	Mhs	28-DIP	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM3 65790 K-5	Mhs	28-DIP	CMOS	0...+70	<385	<165	<35		TTL-TS
HM3 65790 M-2	Mhs	28-DIP	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM3 65790 M-5	Mhs	28-DIP	CMOS	0...+70	<275	<165	<45		TTL-TS
HM3 65791 H-5	Mhs	28-TDIP	CMOS	0...+70	<385	<165	<25		TTL-TS
HM3 65791 K-2	Mhs	28-TDIP	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM3 65791 K-5	Mhs	28-TDIP	CMOS	0...+70	<385	<165	<35		TTL-TS
HM3 65791 K-9	Mhs	28-TDIP	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM3 65791 M-2	Mhs	28-TDIP	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM3 65791 M-5	Mhs	28-TDIP	CMOS	0...+70	<385	<165	<45		TTL-TS
HM3 65791 M-9	Mhs	28-TDIP	CMOS	-40...+85	<385	<165	<45		TTL-TS
HMT 65790 H-5	Mhs	28-FLAT	CMOS	0...+70	<385	<165	<25		TTL-TS
HMT 65790 K-2	Mhs	28-FLAT	CMOS	-55...+125	<385	<165	<35		TTL-TS
HMT 65790 K-5	Mhs	28-FLAT	CMOS	0...+70	<385	<165	<35		TTL-TS
HMT 65790 M-2	Mhs	28-FLAT	CMOS	-55...+125	<385	<165	<45		TTL-TS
HMT 65790 M-5	Mhs	28-FLAT	CMOS	0...+70	<275	<165	<45		TTL-TS
HMT 65791 H-5	Mhs	28-FLAT	CMOS	0...+70	<385	<165	<25		TTL-TS
HMT 65791 K-2	Mhs	28-FLAT	CMOS	-55...+125	<385	<165	<35		TTL-TS
HMT 65791 K-5	Mhs	28-FLAT	CMOS	0...+70	<385	<165	<35		TTL-TS
HMT 65791 K-9	Mhs	28-FLAT	CMOS	-40...+85	<385	<165	<35		TTL-TS
HMT 65791 M-2	Mhs	28-FLAT	CMOS	-55...+125	<385	<165	<45		TTL-TS
HMT 65791 M-5	Mhs	28-FLAT	CMOS	0...+70	<385	<165	<45		TTL-TS
HMT 65791 M-9	Mhs	28-FLAT	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1626 E-15	Inm	28-FLAT	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1626 E-20	Inm	28-FLAT	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1626 E-25	Inm	28-FLAT	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1626 P-15	Inm	28-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1626 P-20	Inm	28-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1626 P-25	Inm	28-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1626 S-15	Inm	28-DIC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1626 S-20	Inm	28-DIC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1626 S-25	Inm	28-DIC	CMOS	0...+70	<550	<220	<25		TTL-TS

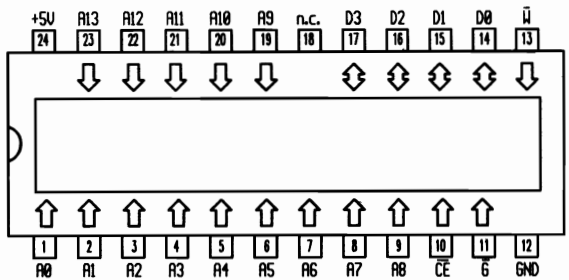
1626 — **16384x4-Bit static RAM**



1626 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65790 H-5	Mhs	28-LCC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM4 65790 K-2	Mhs	28-LCC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM4 65790 K-5	Mhs	28-LCC	CMOS	0...+70	<385	<165	<35		TTL-TS
HM4 65790 M-2	Mhs	28-LCC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM4 65790 M-5	Mhs	28-LCC	CMOS	0...+70	<275	<165	<45		TTL-TS
HM4 65791 H-5	Mhs	28-LCC	CMOS	0...+70	<385	<165	<25		TTL-TS
HM4 65791 K-2	Mhs	28-LCC	CMOS	-55...+125	<385	<165	<35		TTL-TS
HM4 65791 K-5	Mhs	28-LCC	CMOS	0...+70	<385	<165	<35		TTL-TS

1626 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65791 K-9	Mhs	28-LCC	CMOS	-40...+85	<385	<165	<35		TTL-TS
HM4 65791 M-2	Mhs	28-LCC	CMOS	-55...+125	<385	<165	<45		TTL-TS
HM4 65791 M-5	Mhs	28-LCC	CMOS	0...+70	<385	<165	<45		TTL-TS
HM4 65791 M-9	Mhs	28-LCC	CMOS	-40...+85	<385	<165	<45		TTL-TS
IMS 1626 W-15	Inm	28-LCC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1626 W-20	Inm	28-LCC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1626 W-25	Inm	28-LCC	CMOS	0...+70	<550	<220	<25		TTL-TS

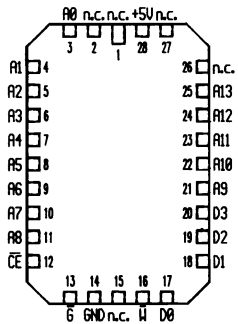
1629 — 16384x4-Bit static RAM



1629 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1629 E-15	Inm	24-FLAT	CMOS	0...+70	<550	<210	<15		TTL-TS
IMS 1629 E-20	Inm	24-FLAT	CMOS	0...+70	<550	<210	<20		TTL-TS
IMS 1629 E-25	Inm	24-FLAT	CMOS	0...+70	<550	<210	<25		TTL-TS
IMS 1629 P-15	Inm	24-DIP	CMOS	0...+70	<550	<210	<15		TTL-TS
IMS 1629 P-20	Inm	24-DIP	CMOS	0...+70	<550	<210	<20		TTL-TS
IMS 1629 P-25	Inm	24-DIP	CMOS	0...+70	<550	<210	<25		TTL-TS
IMS 1629 S-15	Inm	24-DIC	CMOS	0...+70	<550	<210	<15		TTL-TS
IMS 1629 S-20	Inm	24-DIC	CMOS	0...+70	<550	<210	<20		TTL-TS

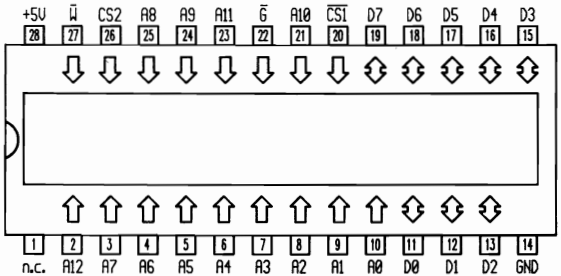
1629 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1629 S-25	Inm	24-DIC	CMOS	0...+70	<550	<210	<25		TTL-TS

1629 — 16384x4-Bit static RAM



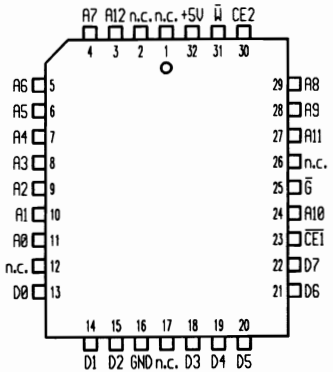
1629 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1629 W-15	Inm	28-LCC	CMOS	0...+70	<550	<210	<15		TTL-TS
IMS 1629 W-20	Inm	28-LCC	CMOS	0...+70	<550	<210	<20		TTL-TS
IMS 1629 W-25	Inm	28-LCC	CMOS	0...+70	<550	<210	<25		TTL-TS

1635 — 8192x8-Bit static RAM

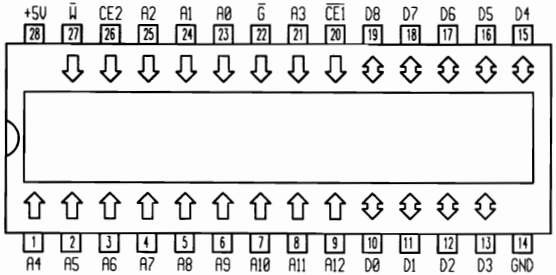


1635 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1635 E-15	Inm	28-FLAT	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1635 E-20	Inm	28-FLAT	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1635 E-25	Inm	28-FLAT	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1635 P-15	Inm	28-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1635 P-20	Inm	28-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1635 P-25	Inm	28-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1635 S-15	Inm	28-DIC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1635 S-20	Inm	28-DIC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1635 S-25	Inm	28-DIC	CMOS	0...+70	<550	<220	<25		TTL-TS
TC 5588 J-20	Tos	28-FLAT	CMOS	0...+70	<660	<110	<20		TTL-TS
TC 5588 J-25	Tos	28-FLAT	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 5588 J-35	Tos	28-FLAT	CMOS	0...+70	<660	<110	<35		TTL-TS
TC 5588 P-20	Tos	28-TDIP	CMOS	0...+70	<660	<110	<20		TTL-TS
TC 5588 P-25	Tos	28-TDIP	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 5588 P-35	Tos	28-TDIP	CMOS	0...+70	<660	<110	<35		TTL-TS

1635 — 8192x8-Bit static RAM



1695 — 8192x9-Bit static RAM



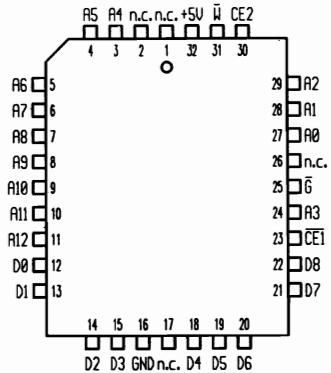
W̄	CS1	CS2	Ḡ	D_n	Mode
X	H	X	X	Hi-Z	not selected (power down)
X	X	L	X	Hi-Z	not selected (power down)
H	L	H	H	Hi-Z	output disabled
H	L	H	L	data out	read
L	L	H	X	data in	write

1635 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1635 W-15	Inm	32-LCC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1635 W-20	Inm	32-LCC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1635 W-25	Inm	32-LCC	CMOS	0...+70	<550	<220	<25		TTL-TS

1695 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM3 65779 K-5	Mhs	28-TDIP	CMOS	0...+70	<660	<137,5	<35		TTL-TS
HM3 65779 M-5	Mhs	28-TDIP	CMOS	0...+70	<660	<137,5	<45		TTL-TS
HM3 65779 N-5	Mhs	28-TDIP	CMOS	0...+70	<660	<137,5	<55		TTL-TS
HMT 65779 K-5	Mhs	28-FLAT	CMOS	0...+70	<660	<137,5	<35		TTL-TS
HMT 65779 M-5	Mhs	28-FLAT	CMOS	0...+70	<660	<137,5	<45		TTL-TS
HMT 65779 N-5	Mhs	28-FLAT	CMOS	0...+70	<660	<137,5	<55		TTL-TS
IMS 1695 E-15	Inm	28-FLAT	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1695 E-20	Inm	28-FLAT	CMOS	0...+70	<550	<220	<20		TTL-TS

1695 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1695 E-25	Inm	28-FLAT	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1695 P-15	Inm	28-DIP	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1695 P-20	Inm	28-DIP	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1695 P-25	Inm	28-DIP	CMOS	0...+70	<550	<220	<25		TTL-TS
IMS 1695 S-15	Inm	28-DIC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1695 S-20	Inm	28-DIC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1695 S-25	Inm	28-DIC	CMOS	0...+70	<550	<220	<25		TTL-TS
M5M 5179 P-35	Mit	28-TDIP	CMOS	0...+70	<660	<137,5	<35		TTL-TS
M5M 5179 P-45	Mit	28-TDIP	CMOS	0...+70	<660	<137,5	<45		TTL-TS
M5M 5179 P-55	Mit	28-TDIP	CMOS	0...+70	<660	<137,5	<55		TTL-TS
TC 5589 J-20	Tos	28-FLAT	CMOS	0...+70	<660	<110	<20		TTL-TS
TC 5589 J-25	Tos	28-FLAT	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 5589 J-35	Tos	28-FLAT	CMOS	0...+70	<660	<110	<35		TTL-TS
TC 5589 P-20	Tos	28-TDIP	CMOS	0...+70	<660	<110	<20		TTL-TS
TC 5589 P-25	Tos	28-TDIP	CMOS	0...+70	<660	<110	<25		TTL-TS
TC 5589 P-35	Tos	28-TDIP	CMOS	0...+70	<660	<110	<35		TTL-TS
TMM 2089 P-35	Tos	28-TDIP	NMOS	0...+70	<135	<15	<35		TTL-TS
TMM 2089 P-45	Tos	28-TDIP	NMOS	0...+70	<135	<15	<45		TTL-TS
TMM 2089 P-55	Tos	28-TDIP	NMOS	0...+70	<135	<15	<55		TTL-TS

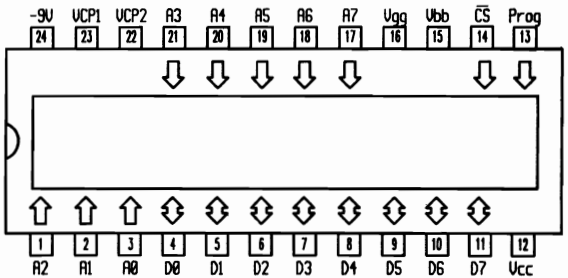
1695 — 8192x9-Bit static RAM



$\overline{W}$	$\overline{CS1}$	CS2	$\overline{G}$	D_n	Mode
X	H	X	X	Hi-Z	not selected (power down)
X	X	L	X	Hi-Z	not selected (power down)
H	L	H	H	Hi-Z	output disabled
H	L	H	L	data out	read
L	L	H	X	data in	write

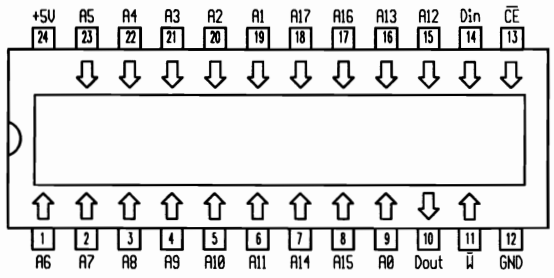
1695 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1695 W-15	Inm	32-LCC	CMOS	0...+70	<550	<220	<15		TTL-TS
IMS 1695 W-20	Inm	32-LCC	CMOS	0...+70	<550	<220	<20		TTL-TS
IMS 1695 W-25	Inm	32-LCC	CMOS	0...+70	<550	<220	<25		TTL-TS

1702 — 256x8-Bit EPROM



1702 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 1702A I	Sig	24-DIC	NMOS	0...+70	<540		<1000		TTL-TS

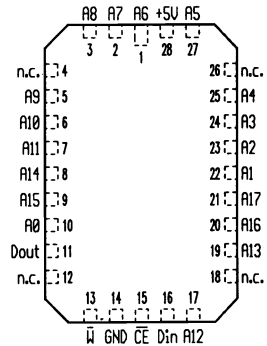
1800 — 262144x1-Bit static RAM



1800 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
FCB 61C251-20 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<20		TTL-TS
FCB 61C251-20 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<20		TTL-TS
FCB 61C251-25 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<25		TTL-TS
FCB 61C251-25 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<25		TTL-TS
FCB 61C251-35 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<35		TTL-TS
FCB 61C251-35 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<35		TTL-TS
FCB 61C251-45 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<45		TTL-TS
FCB 61C251-45 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<45		TTL-TS

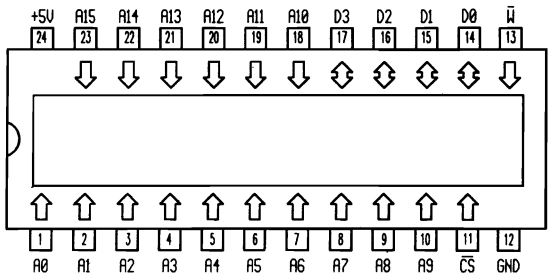
1800 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1800 E-25	Inm	24-FLAT	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1800 E-30	Inm	24-FLAT	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1800 E-35	Inm	24-FLAT	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1800 E-45	Inm	24-FLAT	CMOS	0...+70	<660	<165	<45		TTL-TS
IMS 1800 P-25	Inm	24-DIP	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1800 P-30	Inm	24-DIP	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1800 P-35	Inm	24-DIP	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1800 P-45	Inm	24-DIP	CMOS	0...+70	<660	<165	<45		TTL-TS
IMS 1800 S-25	Inm	24-DIC	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1800 S-30	Inm	24-DIC	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1800 S-35	Inm	24-DIC	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1800 S-45	Inm	24-DIC	CMOS	0...+70	<660	<165	<45		TTL-TS
MCM 6207 L-25	Mot	24-TDIC	CMOS	0...+70	<660		<25		TTL-TS
MCM 6207 L-35	Mot	24-TDIC	CMOS	0...+70	<605		<35		TTL-TS
MCM 6207 P-25	Mot	24-TDIP	CMOS	0...+70	<660		<25		TTL-TS
MCM 6207 P-35	Mot	24-TDIP	CMOS	0...+70	<605		<35		TTL-TS

1800 262144x1-Bit static RAM



1800 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1800 W-25	Inm	28-LCC	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1800 W-30	Inm	28-LCC	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1800 W-35	Inm	28-LCC	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1800 W-45	Inm	28-LCC	CMOS	0...+70	<660	<165	<45		TTL-TS

1820 — 65536x4-Bit static RAM

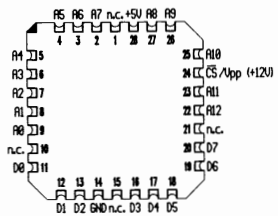


$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

1820 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1820 E-25	Inm	24-FLAT	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1820 E-30	Inm	24-FLAT	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1820 E-35	Inm	24-FLAT	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1820 E-45	Inm	24-FLAT	CMOS	0...+70	<660	<165	<45		TTL-TS
IMS 1820 P-25	Inm	24-DIP	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1820 P-30	Inm	24-DIP	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1820 P-35	Inm	24-DIP	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1820 P-45	Inm	24-DIP	CMOS	0...+70	<660	<165	<45		TTL-TS

1820 Typ · Type · Tipo	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1820 S-25	Inm	24-DIC	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1820 S-30	Inm	24-DIC	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1820 S-35	Inm	24-DIC	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1820 S-45	Inm	24-DIC	CMOS	0...+70	<660	<165	<45		TTL-TS
M5M 5258 AJ-25	Mit	24-FLAT	CMOS	0...+70	<412,5	<55	<25		TTL-TS
M5M 5258 AJ-30	Mit	24-FLAT	CMOS	0...+70	<412,5	<55	<30		TTL-TS
M5M 5258 AP-25	Mit	24-DIP	CMOS	0...+70	<412,5	<55	<25		TTL-TS
M5M 5258 AP-30	Mit	24-DIP	CMOS	0...+70	<412,5	<55	<30		TTL-TS
M5M 5258 BJ-15	Mit	24-FLAT	CMOS	0...+70	<412,5	<55	<15		TTL-TS
M5M 5258 BJ-20	Mit	24-FLAT	CMOS	0...+70	<412,5	<55	<20		TTL-TS
M5M 5258 BP-15	Mit	24-DIP	CMOS	0...+70	<412,5	<55	<15		TTL-TS
M5M 5258 BP-20	Mit	24-DIP	CMOS	0...+70	<412,5	<55	<20		TTL-TS
M5M 5258 J-35	Mit	24-FLAT	CMOS	0...+70	<420	<11	<35		TTL-TS
M5M 5258 J-45	Mit	24-FLAT	CMOS	0...+70	<420	<11	<45		TTL-TS
M5M 5258 J-45L	Mit	24-FLAT	CMOS	0...+70	<420	<0,55	<45		TTL-TS
M5M 5258 P-35	Mit	24-DIP	CMOS	0...+70	<420	<11	<35		TTL-TS
M5M 5258 P-45	Mit	24-DIP	CMOS	0...+70	<420	<11	<45		TTL-TS
M5M 5258 P-45L	Mit	24-DIP	CMOS	0...+70	<420	<0,55	<45		TTL-TS
MCM 6208 L-25	Mot	24-TDIC	CMOS	0...+70	<660		<25		TTL-TS
MCM 6208 L-35	Mot	24-TDIC	CMOS	0...+70	<605		<35		TTL-TS
MCM 6208 P-25	Mot	24-TDIP	CMOS	0...+70	<660		<25		TTL-TS
MCM 6208 P-35	Mot	24-TDIP	CMOS	0...+70	<605		<35		TTL-TS

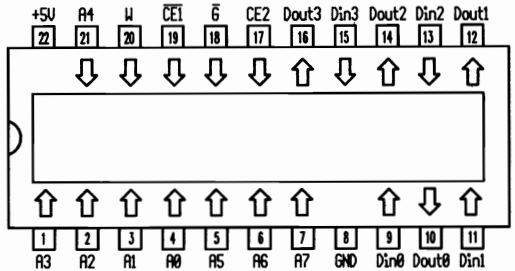
1820 — 65536x4-Bit static RAM



$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1820 W-25	Inm	28-LCC	CMOS	0...+70	<660	<165	<25		TTL-TS
IMS 1820 W-30	Inm	28-LCC	CMOS	0...+70	<660	<165	<30		TTL-TS
IMS 1820 W-35	Inm	28-LCC	CMOS	0...+70	<660	<165	<35		TTL-TS
IMS 1820 W-45	Inm	28-LCC	CMOS	0...+70	<660	<165	<45		TTL-TS

2101 — 256x4-Bit static RAM



$\overline{CE1}$	CE2	$\overline{G}$	W	D_{out}	Mode
H	X	X	X	Hi-Z	not sselected
X	L	X	X	Hi-Z	not selected
X	X	H	H	Hi-Z	output disabled
L	H	H	L	Hi-Z	write
L	H	L	L	data in	write
L	H	L	H	data out	read

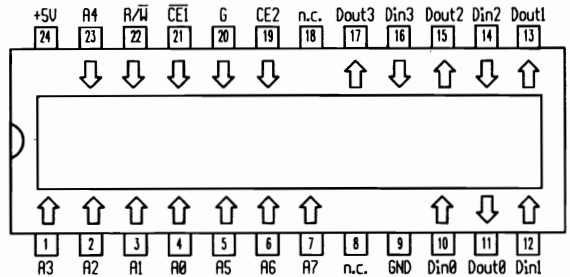
Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2101-1 DC	Amd	22-DIC	NMOS	0...+70	<367		<500		TTL-TS
Am 2101-1 PC	Amd	22-DIP	NMOS	0...+70	<367		<500		TTL-TS
Am 2101-2 DC	Amd	22-DIC	NMOS	0...+70	<367		<650		TTL-TS
Am 2101-2 PC	Amd	22-DIP	NMOS	0...+70	<367		<650		TTL-TS
Am 2101 DC	Amd	22-DIC	NMOS	0...+70	<367		<1000		TTL-TS
Am 2101 PC	Amd	22-DIP	NMOS	0...+70	<367		<1000		TTL-TS
Am 9101 ADC	Amd	22-DIC	NMOS	0...+70	<289		<500		TTL-TS
Am 9101 APC	Amd	22-DIP	NMOS	0...+70	<289		<500		TTL-TS

2101 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9101 BDC	Amd	22-DIC	NMOS	0...+70	<289		<400		TTL-TS
Am 9101 BPC	Amd	22-DIP	NMOS	0...+70	<289		<400		TTL-TS
Am 9101 CDC	Amd	22-DIC	NMOS	0...+70	<315		<300		TTL-TS
Am 9101 CPC	Amd	22-DIP	NMOS	0...+70	<315		<300		TTL-TS
Am 9101 DDC	Amd	22-DIC	NMOS	0...+70	<315		<250		TTL-TS
Am 9101 DPC	Amd	22-DIP	NMOS	0...+70	<315		<250		TTL-TS
Am 9101 EDC	Amd	22-DIC	NMOS	0...+70	<315		<200		TTL-TS
Am 9101 EPC	Amd	22-DIP	NMOS	0...+70	<315		<200		TTL-TS
Am 91L01 ADC	Amd	22-DIC	NMOS	0...+70	<173		<500		TTL-TS
Am 91L01 APC	Amd	22-DIP	NMOS	0...+70	<173		<500		TTL-TS
Am 91L01 BDC	Amd	22-DIC	NMOS	0...+70	<173		<400		TTL-TS
Am 91L01 BPC	Amd	22-DIP	NMOS	0...+70	<173		<400		TTL-TS
Am 91L01 CDC	Amd	22-DIC	NMOS	0...+70	<189		<300		TTL-TS
Am 91L01 CPC	Amd	22-DIP	NMOS	0...+70	<189		<300		TTL-TS
HM 435101	Hit	22-DIP	CMOS	0...+70	<142	<0,52	<650		TTL-TS
HM 435101-1	Hit	22-DIP	CMOS	0...+70	<142	<0,52	<450		TTL-TS
HM 435101 P	Hit	22-DIP	CMOS	0...+70	<142	<79µ	<650		TTL-TS
HM 435101 P-1	Hit	22-DIP	CMOS	0...+70	<142	<79µ	<450		TTL-TS
HM 435101 V	Hit	22-DIP	CMOS	0...+70	<152	<39µ	<650		TTL-TS
HM 435101 VP	Hit	22-DIP	CMOS	0...+70	<159	<41µ	<650		TTL-TS
LH 5101	Sha	22-DIP	CMOS	0...+70	<142	<0.52	<800		TTL-TS
LH 5101 L3	Sha	22-DIP	CMOS	0...+70	<142	<0.52	<650		TTL-TS
LH 5101 S	Sha	22-DIP	CMOS	0...+70	<39	<30µ	<3000		TTL-TS
LH 5101 W	Sha	22-DIP	CMOS	0...+70	<148	<0.55	<800		TTL-TS
M 58721 P	Mit	22-DIP	NMOS	0...+70	<315		<450		TTL-TS
M 58721 S	Mit	22-DIC	NMOS	0...+70	<315		<450		TTL-TS
M5L2101 AP	Mit	22-DIP	NMOS	0...+70	<315		<350		TTL-TS
M5L2101 AP-2	Mit	22-DIP	NMOS	0...+70	<315		<250		TTL-TS
M5L2101 AP-4	Mit	22-DIP	NMOS	0...+70	<315		<450		TTL-TS
M5L2101 AS	Mit	22-DIC	NMOS	0...+70	<315		<350		TTL-TS
M5L2101 AS-2	Mit	22-DIC	NMOS	0...+70	<315		<250		TTL-TS
M5L2101 AS-4	Mit	22-DIC	NMOS	0...+70	<315		<450		TTL-TS
M5L5101 LP-1	Mit	22-DIP	CMOS	0...+70	<148	<0.55	<450		TTL-TS
MB 8101 N	Fui	22-DIP	NMOS	0...+70	<367		<450		TTL-TS
MCM 5101 C-65	Mot	22-DIC	CMOS	0...+70	<110	<1	<650		TTL-TS
MCM 5101 C-80	Mot	22-DIC	CMOS	0...+70	<125	<2,5	<800		TTL-TS
MCM 51L01 C-45	Mot	22-DIC	CMOS	0...+70	<110	<50µ	<450		TTL-TS

2101 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 51L01 C-65	Mot	22-DIC	CMOS	0...+70	<110	<50µ	<650		TTL-TS
MCM 5101 P-65	Mot	22-DIP	CMOS	0...+70	<110	<1	<650		TTL-TS
MCM 5101 P-80	Mot	22-DIP	CMOS	0...+70	<125	<2,5	<800		TTL-TS
MCM 51L01 P-45	Mot	22-DIP	CMOS	0...+70	<110	<50µ	<450		TTL-TS
MCM 51L01 P-65	Mot	22-DIP	CMOS	0...+70	<110	<50µ	<650		TTL-TS
MCM 145101-1 L	Mot	22-DIC	CMOS	0...+70	<142	<52µ	<450		TTL-TS
MCM 145101-1 P	Mot	22-DIP	CMOS	0...+70	<142	<52µ	<450		TTL-TS
MCM 145101-3 L	Mot	22-DIC	CMOS	0...+70	<142	<1	<650		TTL-TS
MCM 145101-3 P	Mot	22-DIP	CMOS	0...+70	<142	<1	<650		TTL-TS
MCM 145101-8 L	Mot	22-DIC	CMOS	0...+70	<157	<2,6	<800		TTL-TS
MCM 145101-8 P	Mot	22-DIP	CMOS	0...+70	<157	<2,6	<800		TTL-TS
MM 2101	Nsc	22-DIP	NMOS	0...+70	<367		<1000		TTL-TS
MM 2101-1	Nsc	22-DIP	NMOS	0...+70	<367		<500		TTL-TS
MM 2101-2	Nsc	22-DIP	NMOS	0...+70	<367		<650		TTL-TS
MM 2101 A	Nsc	22-DIC	NMOS	0...+70	<289		<350		TTL-TS
MM 2101 AL	Nsc	22-DIC	NMOS	0...+70	<231		<350		TTL-TS
N 2101 F	Sig	22-DIC	NMOS	0...+70	<315		<1000		TTL-TS
N 2101-1 F	Sig	22-DIC	NMOS	0...+70	<315		<500		TTL-TS
N 2101-2 F	Sig	22-DIC	NMOS	0...+70	<315		<650		TTL-TS
N 2101 N	Sig	22-DIP	NMOS	0...+70	<315		<1000		TTL-TS
N 2101-1 N	Sig	22-DIP	NMOS	0...+70	<315		<500		TTL-TS
N 2101-2 N	Sig	22-DIP	NMOS	0...+70	<315		<650		TTL-TS
PCD 5101 P	Val	22-DIP	CMOS	-25...+70	<110	<0,55	<150		TTL-TS
TC 5017 P-1	Tos	22-DIP	CMOS	-30...+85	<137	<0.55	<650		TTL-TS
TC 5017 P-2	Tos	22-DIP	CMOS	-30...+85	<137	<0.55	<1000		TTL-TS
TC 5501 D	Tos	22-DIC	CMOS	-30...+85	<82	<0.55	<400		TTL-TS
TC 5501 D-1	Tos	22-DIC	CMOS	-30...+85	<82	<0.55	<600		TTL-TS
TC 5501 P	Tos	22-DIP	CMOS	-30...+85	<82	<0.55	<400		TTL-TS
TC 5501 P-1	Tos	22-DIP	CMOS	-30...+85	<82	<0.55	<600		TTL-TS
TMS 4039	Tix	22-DIP	NMOS	0...+70	<367		<1000		TTL-TS
TMS 4039-1	Tix	22-DIP	NMOS	0...+70	<367		<650		TTL-TS
TMS 4039-2	Tix	22-DIP	NMOS	0...+70	<367		<450		TTL-TS
2101 A	Int	22-DIP	NMOS	0...+70	<315		<350		TTL-TS
2101 A-2	Int	22-DIP	NMOS	0...+70	<367		<250		TTL-TS
2101 A-4	Int	22-DIP	NMOS	0...+70	<315		<450		TTL-TS
5101-8	Int	22-DIP	CMOS	0...+70	<157	<2,6	<800		TTL-TS
5101 L	Int	22-DIP	CMOS	0...+70	<142	<52µ	<650		TTL-TS

2101 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
5101 L-1	Int	22-DIP	CMOS	0...+70	<142	<52µ	<450		TTL-TS
5101 L-3	Int	22-DIP	CMOS	0...+70	<142	<1	<650		TTL-TS
µPD 2101 ALC	Nip	22-DIC	NMOS	-10...+70	<315		<350		TTL-TS
µPD 2101 ALC-2	Nip	22-DIC	NMOS	-10...+70	<315		<250		TTL-TS
µPD 2101 ALC-4	Nip	22-DIC	NMOS	-10...+70	<315		<450		TTL-TS
µPD 5101 C-E	Nip	22-DIC	CMOS	-10...+70	<115	<5,25µ	<800		TTL-TS
µPD 5101 LC	Nip	22-DIP	CMOS	0...+70	<149	<0,055	<650		TTL-TS
µPD 5101 LC-1	Nip	22-DIP	CMOS	0...+70	<149	<0,055	<450		TTL-TS

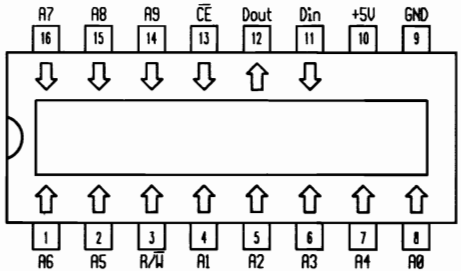
2101 — 256x4-Bit static RAM



$\overline{CE1}$	CE2	$\overline{G}$	W	D_{out}	Mode
H	X	X	X	Hi-Z	not selected
X	L	X	X	Hi-Z	not selected
X	X	H	H	Hi-Z	output disabled
L	H	H	L	Hi-Z	write
L	H	L	L	data in	write
L	H	L	H	data out	read

2101 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCD 5101 T	Val	24-FLAT	CMOS	-25...+70	<110	<0,55	<150		TTL-TS

2102 — 1024x1-Bit static RAM



CE	R/W	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	L	write »0«
L	L	H	H	write »1«
L	H	X	data out	read

2102 Typ · Type · Tipo	Herst. Manuf. Fabr. Prod. Fabr.	Gehäuse Case Boîtier Carcassa Cápsula	Techn. Techn. Techn. Tecn. Tecn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
Am 9102 ADC	Amd	16-DIC	NMOS	0...+70	<262		<500		TTL-TS
Am 9102 APC	Amd	16-DIP	NMOS	0...+70	<262		<500		TTL-TS
Am 9102 BDC	Amd	16-DIC	NMOS	0...+70	<262		<400		TTL-TS
Am 9102 BPC	Amd	16-DIP	NMOS	0...+70	<262		<400		TTL-TS
Am 9102 CDC	Amd	16-DIC	NMOS	0...+70	<289		<300		TTL-TS
Am 9102 CPC	Amd	16-DIP	NMOS	0...+70	<289		<300		TTL-TS
Am 9102 DC	Amd	16-DIC	NMOS	0...+70	<262		<1000		TTL-TS
Am 9102 DDC	Amd	16-DIC	NMOS	0...+70	<289		<250		TTL-TS

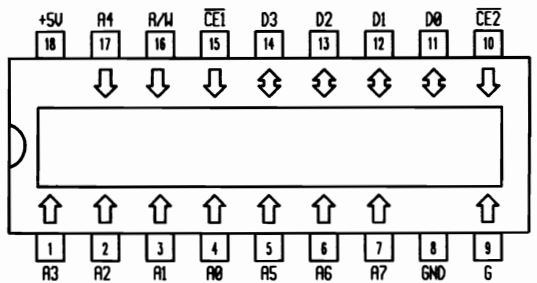
2102 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9102 DPC	Amd	16-DIP	NMOS	0...+70	<289		<250		TTL-TS
Am 9102 EDC	Amd	16-DIC	NMOS	0...+70	<289		<200		TTL-TS
Am 9102 EPC	Amd	16-DIP	NMOS	0...+70	<289		<200		TTL-TS
Am 91L02 ADC	Amd	16-DIC	NMOS	0...+70	<157		<500		TTL-TS
Am 91L02 APC	Amd	16-DIP	NMOS	0...+70	<157		<500		TTL-TS
Am 91L02 BDC	Amd	16-DIC	NMOS	0...+70	<157		<400		TTL-TS
Am 91L02 BPC	Amd	16-DIP	NMOS	0...+70	<157		<400		TTL-TS
Am 91L02 CDC	Amd	16-DIC	NMOS	0...+70	<173		<300		TTL-TS
Am 91L02 CPC	Amd	16-DIP	NMOS	0...+70	<173		<300		TTL-TS
Am 91L02 DC	Amd	16-DIC	NMOS	0...+70	<157		<650		TTL-TS
Am 91L02 PC	Amd	16-DIP	NMOS	0...+70	<157		<650		TTL-TS
Am 9102 PC	Amd	16-DIP	NMOS	0...+70	<262		<650		TTL-TS
M 58751 P	Mit	16-DIP	NMOS	0...+70	<210		<450		TTL-TS
M 58751 S	Mit	16-DIC	NMOS	0...+70	<210		<450		TTL-TS
M5L2102 AP-4	Mit	16-DIP	NMOS	0...+70	<210		<450		TTL-TS
M5L2102 AS-4	Mit	16-DIC	NMOS	0...+70	<210		<450		TTL-TS
MB 8102	Fui	16-DIP	NMOS	0...+70	<367		<450		TTL-TS
MCM 2102 L	Mot	16-DIC	NMOS	0...+70	<368		<1000		TTL-TS
MCM 2102 L1	Mot	16-DIC	NMOS	0...+70	<368		<500		TTL-TS
MCM 2102 L2	Mot	16-DIC	NMOS	0...+70	<368		<650		TTL-TS
MCM 2102A L	Mot	16-DIC	NMOS	0...+70	<368		<350		TTL-TS
MCM 2102A L2	Mot	16-DIC	NMOS	0...+70	<368		<250		TTL-TS
MCM 2102A L4	Mot	16-DIC	NMOS	0...+70	<368		<450		TTL-TS
MCM 2102 P	Mot	16-DIP	NMOS	0...+70	<368		<1000		TTL-TS
MCM 2102 P1	Mot	16-DIP	NMOS	0...+70	<368		<500		TTL-TS
MCM 2102 P2	Mot	16-DIP	NMOS	0...+70	<368		<650		TTL-TS
MCM 2102A P	Mot	16-DIP	NMOS	0...+70	<368		<350		TTL-TS
MCM 2102A P2	Mot	16-DIP	NMOS	0...+70	<368		<250		TTL-TS
MCM 2102A P4	Mot	16-DIP	NMOS	0...+70	<368		<450		TTL-TS
MM 2102-1J	Nsc	16-DIC	NMOS	0...+70	<367		<500		TTL-TS
MM 2102-1N	Nsc	16-DIP	NMOS	0...+70	<367		<500		TTL-TS
MM 2102-2J	Nsc	16-DIC	NMOS	0...+70	<367		<650		TTL-TS
MM 2102-2N	Nsc	16-DIP	NMOS	0...+70	<367		<650		TTL-TS
MM 2102 A-2J	Nsc	16-DIC	NMOS	0...+70	<262		<250		TTL-TS
MM 2102 A-2 LJ	Nsc	16-DIC	NMOS	0...+70	<173		<250		TTL-TS
MM 2102 A-2 LN	Nsc	16-DIP	NMOS	0...+70	<173		<250		TTL-TS
MM 2102 A-2N	Nsc	16-DIP	NMOS	0...+70	<262		<250		TTL-TS

2102 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MM 2102 A-4J	Nsc	16-DIC	NMOS	0...+70	<262		<450		TTL-TS
MM 2102 A-4 LJ	Nsc	16-DIC	NMOS	0...+70	<173		<450		TTL-TS
MM 2102 A-4 LN	Nsc	16-DIP	NMOS	0...+70	<173		<450		TTL-TS
MM 2102 A-4N	Nsc	16-DIP	NMOS	0...+70	<262		<450		TTL-TS
MM 2102 A-6J	Nsc	16-DIC	NMOS	0...+70	<262		<650		TTL-TS
MM 2102 A-6 LJ	Nsc	16-DIC	NMOS	0...+70	<173		<650		TTL-TS
MM 2102 A-6 LN	Nsc	16-DIP	NMOS	0...+70	<173		<650		TTL-TS
MM 2102 A-6N	Nsc	16-DIP	NMOS	0...+70	<262		<650		TTL-TS
MM 2102 AJ	Nsc	16-DIC	NMOS	0...+70	<262		<350		TTL-TS
MM 2102 ALJ	Nsc	16-DIC	NMOS	0...+70	<173		<350		TTL-TS
MM 2102 ALN	Nsc	16-DIP	NMOS	0...+70	<173		<350		TTL-TS
MM 2102 AN	Nsc	16-DIP	NMOS	0...+70	<262		<350		TTL-TS
MM 2102 J	Nsc	16-DIC	NMOS	0...+70	<367		<1000		TTL-TS
MM 2102 N	Nsc	16-DIP	NMOS	0...+70	<367		<1000		TTL-TS
N 2102 F	Sig	16-DIC	NMOS	0...+70	<315		<1000		TTL-TS
N 2102-1 F	Sig	16-DIC	NMOS	0...+70	<315		<500		TTL-TS
N 2102-2 F	Sig	16-DIC	NMOS	0...+70	<315		<650		TTL-TS
N 2102A F	Sig	16-DIC	NMOS	0...+70	<289		<350		TTL-TS
N 2102A-2 F	Sig	16-DIC	NMOS	0...+70	<341		<250		TTL-TS
N 2102A-4 F	Sig	16-DIC	NMOS	0...+70	<289		<450		TTL-TS
N 2102A-6 F	Sig	16-DIC	NMOS	0...+70	<289		<650		TTL-TS
N 2102AL F	Sig	16-DIC	NMOS	0...+70	<174	<35	<350		TTL-TS
N 2102AL-2 F	Sig	16-DIC	NMOS	0...+70	<236	<42	<250		TTL-TS
N 2102AL-4 F	Sig	16-DIC	NMOS	0...+70	<174	<35	<450		TTL-TS
N 21F02 F	Sig	16-DIC	NMOS	0...+70	<315		<350		TTL-TS
N 21F02-2 F	Sig	16-DIC	NMOS	0...+70	<315		<250		TTL-TS
N 21F02-4 F	Sig	16-DIC	NMOS	0...+70	<315		<450		TTL-TS
N 21L02 F	Sig	16-DIC	NMOS	0...+70	<210		<1000		TTL-TS
N 21L02-1 F	Sig	16-DIC	NMOS	0...+70	<210		<500		TTL-TS
N 21L02-2 F	Sig	16-DIC	NMOS	0...+70	<210		<650		TTL-TS
N 21L02-3 F	Sig	16-DIC	NMOS	0...+70	<210		<400		TTL-TS
N 2102 I	Sig	16-DIC	NMOS	0...+70	<315		<1000		TTL-TS
N 2102-1 I	Sig	16-DIC	NMOS	0...+70	<315		<500		TTL-TS
N 2102-2 I	Sig	16-DIC	NMOS	0...+70	<315		<650		TTL-TS
N 2102A I	Sig	16-DIC	NMOS	0...+70	<289		<350		TTL-TS
N 2102A-2 I	Sig	16-DIC	NMOS	0...+70	<341		<250		TTL-TS
N 2102A-4 I	Sig	16-DIC	NMOS	0...+70	<289		<450		TTL-TS

2102 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 2102A-6 I	Sig	16-DIC	NMOS	0...+70	<289		<650		TTL-TS
N 2102AL I	Sig	16-DIC	NMOS	0...+70	<174	<35	<350		TTL-TS
N 2102AL-2 I	Sig	16-DIC	NMOS	0...+70	<236	<42	<250		TTL-TS
N 2102AL-4 I	Sig	16-DIC	NMOS	0...+70	<174	<35	<450		TTL-TS
N 21F02 I	Sig	16-DIC	NMOS	0...+70	<315		<350		TTL-TS
N 21F02-2 I	Sig	16-DIC	NMOS	0...+70	<315		<250		TTL-TS
N 21F02-4 I	Sig	16-DIC	NMOS	0...+70	<315		<450		TTL-TS
N 21L02 I	Sig	16-DIC	NMOS	0...+70	<210		<1000		TTL-TS
N 21L02-1 I	Sig	16-DIC	NMOS	0...+70	<210		<500		TTL-TS
N 21L02-2 I	Sig	16-DIC	NMOS	0...+70	<210		<650		TTL-TS
N 21L02-3 I	Sig	16-DIC	NMOS	0...+70	<210		<400		TTL-TS
N 2102 N	Sig	16-DIP	NMOS	0...+70	<315		<1000		TTL-TS
N 2102-1 N	Sig	16-DIP	NMOS	0...+70	<315		<500		TTL-TS
N 2102-2 N	Sig	16-DIP	NMOS	0...+70	<315		<650		TTL-TS
N 2102A N	Sig	16-DIP	NMOS	0...+70	<289		<350		TTL-TS
N 2102A-2 N	Sig	16-DIP	NMOS	0...+70	<341		<250		TTL-TS
N 2102A-4 N	Sig	16-DIP	NMOS	0...+70	<289		<450		TTL-TS
N 2102A-6 N	Sig	16-DIP	NMOS	0...+70	<289		<650		TTL-TS
N 2102AL N	Sig	16-DIP	NMOS	0...+70	<174	<35	<350		TTL-TS
N 2102AL-2 N	Sig	16-DIP	NMOS	0...+70	<236	<42	<250		TTL-TS
N 2102AL-4 N	Sig	16-DIP	NMOS	0...+70	<174	<35	<450		TTL-TS
N 21F02 N	Sig	16-DIP	NMOS	0...+70	<315		<350		TTL-TS
N 21F02-2 N	Sig	16-DIP	NMOS	0...+70	<315		<250		TTL-TS
N 21F02-4 N	Sig	16-DIP	NMOS	0...+70	<315		<450		TTL-TS
N 21L02 N	Sig	16-DIP	NMOS	0...+70	<210		<1000		TTL-TS
N 21L02-1 N	Sig	16-DIP	NMOS	0...+70	<210		<500		TTL-TS
N 21L02-2 N	Sig	16-DIP	NMOS	0...+70	<210		<650		TTL-TS
N 21L02-3 N	Sig	16-DIP	NMOS	0...+70	<210		<400		TTL-TS
TMM 313 P	Tos	16-DIP	NMOS	-10...+80	<367		<350		TTL-TS
TMM 313 P-1	Tos	16-DIP	NMOS	-10...+80	<367		<250		TTL-TS
TMM 313 P-4	Tos	16-DIP	NMOS	-10...+80	<367		<450		TTL-TS
TMS 4033 LJ	Tix	16-DIC	NMOS	0...+70	<367		<450		TTL-TS
TMS 4033 LN	Tix	16-DIP	NMOS	0...+70	<367		<450		TTL-TS
TMS 4034 LJ	Tix	16-DIC	NMOS	0...+70	<367		<650		TTL-TS
TMS 4034 LN	Tix	16-DIP	NMOS	0...+70	<367		<650		TTL-TS
TMS 4035 LJ	Tix	16-DIC	NMOS	0...+70	<367		<1000		TTL-TS
TMS 4035 LN	Tix	16-DIP	NMOS	0...+70	<367		<1000		TTL-TS

2102 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
2102-1 DC	Fch	16-DIP	NMOS	0...+70	<262		<450		TTL-TS
2102-2 DC	Fch	16-DIP	NMOS	0...+70	<262		<650		TTL-TS
2102 A	Int	16-DIP	NMOS	0...+70	<289		<350		TTL-TS
2102 A-2	Int	16-DIP	NMOS	0...+70	<341		<250		TTL-TS
2102 A-4	Int	16-DIP	NMOS	0...+70	<289		<450		TTL-TS
2102 A-6	Int	16-DIP	NMOS	0...+70	<289		<650		TTL-TS
2102 AL	Int	16-DIP	NMOS	0...+70	<173		<350		TTL-TS
2102 AL-2	Int	16-DIP	NMOS	0...+70	<173		<250		TTL-TS
2102 AL-4	Int	16-DIP	NMOS	0...+70	<173		<450		TTL-TS
2102-DC	Fch	16-DIP	NMOS	0...+70	<262		<1000		TTL-TS
2102-F DC	Fch	16-DIP	NMOS	0...+70	<262		<350		TTL-TS
21L02	Fch	16-DIP	NMOS	0...+70	<157		<650		TTL-TS
21L02 A	Fch	16-DIP	NMOS	0...+70	<157		<500		TTL-TS
21L02 B	Fch	16-DIP	NMOS	0...+70	<157		<400		TTL-TS
2102 R	Fch	16-DIP	NMOS	0...+70	<289		<200		TTL-TS
µPD 2102 ALC	Nip	16-DIC	NMOS	-10...+70	<368		<350		TTL-TS
µPD 2102 ALC-2	Nip	16-DIC	NMOS	-10...+70	<368		<250		TTL-TS
µPD 2102 ALC-4	Nip	16-DIC	NMOS	-10...+70	<368		<450		TTL-TS

2111 — 256x4-Bit static RAM

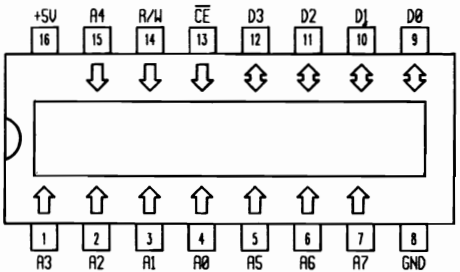


2111 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2111-1 DC	Amd	18-DIC	NMOS	0...+70	<367		<500		TTL-TS
Am 2111-1 PC	Amd	18-DIP	NMOS	0...+70	<367		<500		TTL-TS
Am 2111-2 DC	Amd	18-DIC	NMOS	0...+70	<367		<650		TTL-TS
Am 2111-2 PC	Amd	18-DIP	NMOS	0...+70	<367		<650		TTL-TS
Am 2111 DC	Amd	18-DIC	NMOS	0...+70	<367		<1000		TTL-TS
Am 2111 PC	Amd	18-DIP	NMOS	0...+70	<367		<1000		TTL-TS
Am 9111 ADC	Amd	18-DIC	NMOS	0...+70	<289		<500		TTL-TS
Am 9111 APC	Amd	18-DIP	NMOS	0...+70	<289		<500		TTL-TS

2111 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9111 BDC	Amd	18-DIC	NMOS	0...+70	<289		<400		TTL-TS
Am 9111 BPC	Amd	18-DIP	NMOS	0...+70	<289		<400		TTL-TS
Am 9111 CDC	Amd	18-DIC	NMOS	0...+70	<315		<300		TTL-TS
Am 9111 CPC	Amd	18-DIP	NMOS	0...+70	<315		<300		TTL-TS
Am 9111 DDC	Amd	18-DIC	NMOS	0...+70	<315		<250		TTL-TS
Am 9111 DPC	Amd	18-DIP	NMOS	0...+70	<315		<250		TTL-TS
Am 9111 EDC	Amd	18-DIC	NMOS	0...+70	<315		<200		TTL-TS
Am 9111 EPC	Amd	18-DIP	NMOS	0...+70	<315		<200		TTL-TS
Am 91L11 ADC	Amd	18-DIC	NMOS	0...+70	<173		<500		TTL-TS
Am 91L11 APC	Amd	18-DIP	NMOS	0...+70	<173		<500		TTL-TS
Am 91L11 BDC	Amd	18-DIC	NMOS	0...+70	<173		<400		TTL-TS
Am 91L11 BPC	Amd	18-DIP	NMOS	0...+70	<173		<400		TTL-TS
Am 91L11 CDC	Amd	18-DIC	NMOS	0...+70	<189		<300		TTL-TS
Am 91L11 CPC	Amd	18-DIP	NMOS	0...+70	<189		<300		TTL-TS
LH 2111 A2	Sha	18-DIP	NMOS		<370		<250		TTL-TS
LH 2111 A4	Sha	18-DIP	NMOS		<370		<450		TTL-TS
M 58722 P	Mit	18-DIP	NMOS	0...+70	<315		<450		TTL-TS
M5L2111 AP	Mit	18-DIP	NMOS	0...+70	<315		<350		TTL-TS
M5L2111 AP-2	Mit	18-DIP	NMOS	0...+70	<315		<250		TTL-TS
M5L2111 AP-4	Mit	18-DIP	NMOS	0...+70	<315		<450		TTL-TS
M5L2111 AS	Mit	18-DIC	NMOS	0...+70	<315		<350		TTL-TS
M5L2111 AS-2	Mit	18-DIC	NMOS	0...+70	<315		<250		TTL-TS
M5L2111 AS-4	Mit	18-DIC	NMOS	0...+70	<315		<450		TTL-TS
MB 8111 N	Fui	18-DIP	NMOS	0...+70	<367		<450		TTL-TS
MCM 2111A L	Mot	18-DIC	NMOS	0...+70	<368		<350		TTL-TS
MCM 2111A L2	Mot	18-DIC	NMOS	0...+70	<368		<250		TTL-TS
MCM 2111A L4	Mot	18-DIC	NMOS	0...+70	<368		<450		TTL-TS
MCM 2111A P	Mot	18-DIP	NMOS	0...+70	<368		<350		TTL-TS
MCM 2111A P2	Mot	18-DIP	NMOS	0...+70	<368		<250		TTL-TS
MCM 2111A P4	Mot	18-DIP	NMOS	0...+70	<368		<450		TTL-TS
MCM 68111 AL	Mot	18-DIC	NMOS	0...+70	<367		<450		TTL-TS
MCM 68111 AP	Mot	18-DIP	NMOS	0...+70	<367		<450		TTL-TS
MM 2111	Nsc	18-DIP	NMOS	0...+70	<367		<1000		TTL-TS
MM 2111-1	Nsc	18-DIP	NMOS	0...+70	<367		<500		TTL-TS
MM 2111-2	Nsc	18-DIP	NMOS	0...+70	<367		<650		TTL-TS
N 2111 I	Sig	18-DIC	NMOS	0...+70	<315		<1000		TTL-TS
N 2111-1 I	Sig	18-DIC	NMOS	0...+70	<315		<500		TTL-TS

2111 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 2111-2 I	Sig	18-DIC	NMOS	0...+70	<315		<650		TTL-TS
N 2111 N	Sig	18-DIP	NMOS	0...+70	<315		<1000		TTL-TS
N 2111-1 N	Sig	18-DIP	NMOS	0...+70	<315		<500		TTL-TS
N 2111-2 N	Sig	18-DIP	NMOS	0...+70	<315		<650		TTL-TS
TMM 311 P	Tos	18-DIP	NMOS	-20...+80	<367		<1000		TTL-TS
TMM 311 P-1	Tos	18-DIP	NMOS	-20...+80	<367		<650		TTL-TS
TMS 4042-1 LJ	Tix	18-DIC	NMOS	0...+70	<367		<650		TTL-TS
TMS 4042-1 LN	Tix	18-DIP	NMOS	0...+70	<367		<650		TTL-TS
TMS 4042-2 LJ	Tix	18-DIC	NMOS	0...+70	<367		<450		TTL-TS
TMS 4042-2 LN	Tix	18-DIP	NMOS	0...+70	<367		<450		TTL-TS
TMS 4042 LJ	Tix	18-DIC	NMOS	0...+70	<367		<1000		TTL-TS
TMS 4042 LN	Tix	18-DIP	NMOS	0...+70	<367		<1000		TTL-TS
2111 A	Int	18-DIP	NMOS	0...+70	<315		<350		TTL-TS
2111 A-2	Int	18-DIP	NMOS	0...+70	<367		<250		TTL-TS
2111 A-4	Int	18-DIP	NMOS	0...+70	<315		<450		TTL-TS
µPD 2111 ALC	Nip	18-DIC	NMOS	-10...+70	<289		<350		TTL-TS
µPD 2111 ALC-2	Nip	18-DIC	NMOS	-10...+70	<289		<250		TTL-TS
µPD 2111 ALC-4	Nip	18-DIC	NMOS	-10...+70	<289		<450		TTL-TS

2112 — 256x4-Bit static RAM

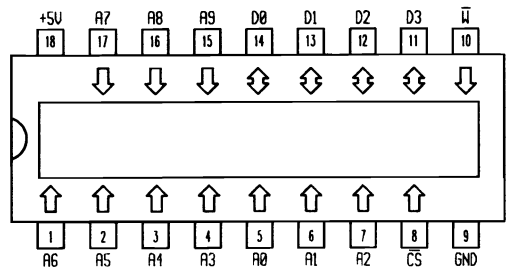


2112 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9112 EDC	Amd	16-DIC	NMOS	0...+70	<315		<200		TTL-TS
Am 9112 EPC	Amd	16-DIP	NMOS	0...+70	<315		<200		TTL-TS
Am 91L12 ADC	Amd	16-DIC	NMOS	0...+70	<173		<500		TTL-TS
Am 91L12 APC	Amd	16-DIP	NMOS	0...+70	<173		<500		TTL-TS
Am 91L12 BDC	Amd	16-DIC	NMOS	0...+70	<173		<400		TTL-TS
Am 91L12 BPC	Amd	16-DIP	NMOS	0...+70	<173		<400		TTL-TS
Am 91L12 CDC	Amd	16-DIC	NMOS	0...+70	<173		<300		TTL-TS
Am 91L12 CPC	Amd	16-DIP	NMOS	0...+70	<173		<300		TTL-TS
M 58723 P	Mit	16-DIP	NMOS	0...+70	<315		<450		TTL-TS
M 58723 S	Mit	16-DIC	NMOS	0...+70	<315		<450		TTL-TS
M5L2112 AP	Mit	16-DIP	NMOS	0...+70	<210		<350		TTL-TS
M5L2112 AP-2	Mit	16-DIP	NMOS	0...+70	<210		<250		TTL-TS
M5L2112 AP-4	Mit	16-DIP	NMOS	0...+70	<210		<450		TTL-TS
M5L2112 AS	Mit	16-DIC	NMOS	0...+70	<210		<350		TTL-TS
M5L2112 AS-2	Mit	16-DIC	NMOS	0...+70	<210		<250		TTL-TS
M5L2112 AS-4	Mit	16-DIC	NMOS	0...+70	<210		<450		TTL-TS
MB 8112 N	Fui	16-DIP	NMOS	0...+70	<367		<450		TTL-TS
MCM 2112A L	Mot	16-DIC	NMOS	0...+70	<368		<350		TTL-TS
MCM 2112A L2	Mot	16-DIC	NMOS	0...+70	<368		<250		TTL-TS
MCM 2112A L4	Mot	16-DIC	NMOS	0...+70	<368		<450		TTL-TS
MCM 2112A P	Mot	16-DIP	NMOS	0...+70	<368		<350		TTL-TS
MCM 2112A P2	Mot	16-DIP	NMOS	0...+70	<368		<250		TTL-TS
MCM 2112A P4	Mot	16-DIP	NMOS	0...+70	<368		<450		TTL-TS
MCM 68112 A	Mot	16-DIP	NMOS	0...+70	<367		<450		TTL-TS
MCM 68112 AL	Mot	16-DIC	NMOS	0...+70	<367		<450		TTL-TS
MCM 68112 AP	Mot	16-DIP	NMOS	0...+70	<367		<450		TTL-TS
MM 2112	Nsc	16-DIP	NMOS	0...+70	<367		<1000		TTL-TS
MM 2112-2	Nsc	16-DIP	NMOS	0...+70	<367		<650		TTL-TS
MM 2112 A	Nsc	16-DIP	NMOS	0...+70	<289		<350		TTL-TS
MM 2112 A-2	Nsc	16-DIP	NMOS	0...+70	<289		<250		TTL-TS
MM 2112 A-4	Nsc	16-DIP	NMOS	0...+70	<289		<450		TTL-TS
MM 2112 A-4 L	Nsc	16-DIP	NMOS	0...+70	<231		<450		TTL-TS
MM 2112 A-6	Nsc	16-DIP	NMOS	0...+70	<289		<650		TTL-TS
MM 2112 A-6 L	Nsc	16-DIP	NMOS	0...+70	<231		<650		TTL-TS
MM 2112 A-L	Nsc	16-DIP	NMOS	0...+70	<231		<350		TTL-TS
N 2112 F	Sig	16-DIC	NMOS	0...+70	<315		<1000		TTL-TS
N 2112-1 F	Sig	16-DIC	NMOS	0...+70	<315		<500		TTL-TS

2112 Typ · Type · Tipo	Herst. Manuf. Fabr. Prod. Fabr.	Gehäuse Case Boîtier Carcassa Cápsula	Techn. Techn. Techn. Tecn. Tecn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
Am 9112 ADC	Amd	16-DIC	NMOS	0...+70	<289		<500		TTL-TS
Am 9112 APC	Amd	16-DIP	NMOS	0...+70	<289		<500		TTL-TS
Am 9112 BDC	Amd	16-DIC	NMOS	0...+70	<289		<400		TTL-TS
Am 9112 BPC	Amd	16-DIP	NMOS	0...+70	<289		<400		TTL-TS
Am 9112 CDC	Amd	16-DIC	NMOS	0...+70	<315		<300		TTL-TS
Am 9112 CPC	Amd	16-DIP	NMOS	0...+70	<315		<300		TTL-TS
Am 9112 DDC	Amd	16-DIC	NMOS	0...+70	<315		<250		TTL-TS
Am 9112 DPC	Amd	16-DIP	NMOS	0...+70	<315		<250		TTL-TS

2112 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 2112-2 F	Sig	16-DIC	NMOS	0...+70	<315		<650		TTL-TS
N 2112 N	Sig	16-DIP	NMOS	0...+70	<315		<1000		TTL-TS
N 2112-1 N	Sig	16-DIP	NMOS	0...+70	<315		<500		TTL-TS
N 2112-2 N	Sig	16-DIP	NMOS	0...+70	<315		<650		TTL-TS
TMM 312 P	Tos	16-DIP	NMOS	-20...+80	<367		<1000		TTL-TS
TMM 312 P-1	Tos	16-DIP	NMOS	-20...+80	<367		<650		TTL-TS
TMS 4043-1 JL	Tix	16-DIC	NMOS	0...+70	<367		<650		TTL-TS
TMS 4043-1 NL	Tix	16-DIP	NMOS	0...+70	<367		<650		TTL-TS
TMS 4043-2 JL	Tix	16-DIC	NMOS	0...+70	<367		<450		TTL-TS
TMS 4043-2 NL	Tix	16-DIP	NMOS	0...+70	<367		<450		TTL-TS
TMS 4043 JL	Tix	16-DIC	NMOS	0...+70	<367		<1000		TTL-TS
TMS 4043 NL	Tix	16-DIP	NMOS	0...+70	<367		<1000		TTL-TS
2112 A	Int	16-DIP	NMOS	0...+70	<315		<350		TTL-TS
2112 A-2	Int	16-DIP	NMOS	0...+70	<367		<250		TTL-TS
2112 A-4	Int	16-DIP	NMOS	0...+70	<315		<450		TTL-TS

2114 — 1024x4-Bit static RAM



2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9114 BDC	Amd	18-DIC	NMOS	0...+70	<315		<450		TTL-TS
Am 9114 BPC	Amd	18-DIP	NMOS	0...+70	<315		<450		TTL-TS
Am 9114 CDC	Amd	18-DIC	NMOS	0...+70	<315		<300		TTL-TS
Am 9114 CPC	Amd	18-DIP	NMOS	0...+70	<315		<300		TTL-TS
Am 9114 EDC	Amd	18-DIC	NMOS	0...+70	<315		<200		TTL-TS
Am 9114 EPC	Amd	18-DIP	NMOS	0...+70	<315		<200		TTL-TS
Am 91L14 BDC	Amd	18-DIC	NMOS	0...+70	<210		<450		TTL-TS
Am 91L14 BPC	Amd	18-DIP	NMOS	0...+70	<210		<450		TTL-TS

2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
Am 91L14 CDC	Amd	18-DIC	NMOS	0...+70	<210		<300		TTL-TS
Am 91L14 CPC	Amd	18-DIP	NMOS	0...+70	<210		<300		TTL-TS
Am 91L14 EPC	Amd	18-DIP	NMOS	0...+70	<262		<200		TTL-TS
Am 9124 BDC	Amd	18-DIC	NMOS	0...+70	<315	<105	<450		TTL-TS
Am 9124 BPC	Amd	18-DIP	NMOS	0...+70	<315	<105	<450		TTL-TS
Am 9124 CDC	Amd	18-DIC	NMOS	0...+70	<315	<105	<300		TTL-TS
Am 9124 CPC	Amd	18-DIP	NMOS	0...+70	<315	<105	<300		TTL-TS
Am 9124 EDC	Amd	18-DIC	NMOS	0...+70	<315	<105	<200		TTL-TS
Am 9124 EPC	Amd	18-DIP	NMOS	0...+70	<315	<105	<200		TTL-TS
Am 91L24 BDC	Amd	18-DIC	NMOS	0...+70	<210	<79	<450		TTL-TS
Am 91L24 BPC	Amd	18-DIP	NMOS	0...+70	<210	<79	<450		TTL-TS
Am 91L24 CDC	Amd	18-DIC	NMOS	0...+70	<210	<79	<300		TTL-TS
Am 91L24 CPC	Amd	18-DIP	NMOS	0...+70	<210	<79	<300		TTL-TS
Am 91L24 E	Amd	18-DIP	NMOS	0...+70	<262	<79	<200		TTL-TS
F 2114-2 D	Fch	18-DIC	NMOS	0...+70	<525		<200		TTL-TS
F 2114-2 P	Fch	18-DIP	NMOS	0...+70	<525		<200		TTL-TS
F 2114-3 D	Fch	18-DIC	NMOS	0...+70	<525		<300		TTL-TS
F 2114-3 P	Fch	18-DIP	NMOS	0...+70	<525		<300		TTL-TS
F 2114 D	Fch	18-DIC	NMOS	0...+70	<525		<450		TTL-TS
F 2114 LD	Fch	18-DIC	NMOS	0...+70	<262		<450		TTL-TS
F 2114 LD-2	Fch	18-DIC	NMOS	0...+70	<262		<200		TTL-TS
F 2114 LD-3	Fch	18-DIC	NMOS	0...+70	<262		<300		TTL-TS
F 2114 LP	Fch	18-DIP	NMOS	0...+70	<262		<450		TTL-TS
F 2114 LP-2	Fch	18-DIP	NMOS	0...+70	<262		<200		TTL-TS
F 2114 LP-3	Fch	18-DIP	NMOS	0...+70	<262		<300		TTL-TS
F 2114 P	Fch	18-DIP	NMOS	0...+70	<525		<450		TTL-TS
HM 472114 A-1	Hit	18-DIC	NMOS	0...+70	200		<150		TTL-TS
HM 472114 A-2	Hit	18-DIC	NMOS	0...+70	200		<200		TTL-TS
HM 472114-3	Hit	18-DIC	NMOS	0...+70	200		<300		TTL-TS
HM 472114-4	Hit	18-DIC	NMOS	0...+70	200		<450		TTL-TS
HM 472114 AP-1	Hit	18-DIP	NMOS	0...+70	200		<150		TTL-TS
HM 472114 AP-2	Hit	18-DIP	NMOS	0...+70	200		<200		TTL-TS
HM 472114 P-3	Hit	18-DIP	NMOS	0...+70	200		<300		TTL-TS
HM 472114 P-4	Hit	18-DIP	NMOS	0...+70	200		<450		TTL-TS
IM 2114-2 DN	Isi	18-DIC	NMOS	0...+70	<525		<200		TTL-TS
IM 2114-2 PN	Isi	18-DIP	NMOS	0...+70	<525		<200		TTL-TS
IM 2114-3 DN	Isi	18-DIC	NMOS	0...+70	<525		<300		TTL-TS

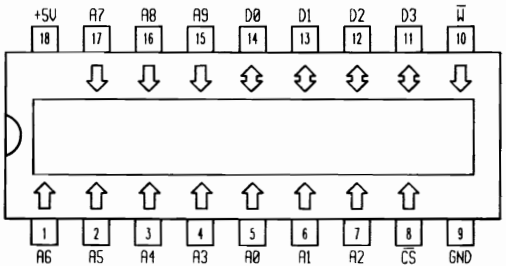
2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IM 2114-3 PN	Isi	18-DIP	NMOS	0...+70	<525		<300		TTL-TS
IM 2114 2CDN	Isi	18-DIC	NMOS	0...+70	<709		<200		TTL-TS
IM 2114 2CPN	Isi	18-DIP	NMOS	0...+70	<709		<200		TTL-TS
IM 2114 3CDN	Isi	18-DIC	NMOS	0...+70	<709		<300		TTL-TS
IM 2114 3CPN	Isi	18-DIP	NMOS	0...+70	<709		<300		TTL-TS
IM 2114 CDN	Isi	18-DIC	NMOS	0...+70	<709		<450		TTL-TS
IM 2114 CPN	Isi	18-DIP	NMOS	0...+70	<709		<450		TTL-TS
IM 2114 L2CDN	Isi	18-DIC	NMOS	0...+70	<367		<200		TTL-TS
IM 2114 L2CPN	Isi	18-DIP	NMOS	0...+70	<367		<200		TTL-TS
IM 2114 L3CDN	Isi	18-DIC	NMOS	0...+70	<367		<300		TTL-TS
IM 2114 L3CPN	Isi	18-DIP	NMOS	0...+70	<367		<300		TTL-TS
IM 2114 LCDN	Isi	18-DIC	NMOS	0...+70	<367		<450		TTL-TS
IM 2114 LCPN	Isi	18-DIP	NMOS	0...+70	<367		<450		TTL-TS
IM 2114 LDN	Isi	18-DIC	NMOS	0...+70	<367		<450		TTL-TS
IM 2114 LPN	Isi	18-DIP	NMOS	0...+70	<367		<450		TTL-TS
IM 7114 L2CDN	Isi	18-DIC	NMOS	0...+70	<262		<200		TTL-TS
IM 7114 L2CPN	Isi	18-DIP	NMOS	0...+70	<262		<200		TTL-TS
IM 7114 L3CDN	Isi	18-DIC	NMOS	0...+70	<262		<300		TTL-TS
IM 7114 L3CPN	Isi	18-DIP	NMOS	0...+70	<262		<300		TTL-TS
IM 7114 LCDN	Isi	18-DIC	NMOS	0...+70	<262		<450		TTL-TS
IM 7114 LCPN	Isi	18-DIP	NMOS	0...+70	<262		<450		TTL-TS
LH 2114 H1	Sha	18-DIP	NMOS	0...+70	<682		<100		TTL-TS
LH 2114 H2	Sha	18-DIP	NMOS	0...+70	<367		<150		TTL-TS
LH 2114 H3	Sha	18-DIP	NMOS	0...+70	<367		<300		TTL-TS
LH 5114-4	Sha	18-DIP	CMOS	0...+70	<82,5	<55µ	<450		TTL-TS
LH 5114-5	Sha	18-DIP	CMOS	0...+70	<82,5	<55µ	<550		TTL-TS
LH 5114-6	Sha	18-DIP	CMOS	0...+70	<82,5	<55µ	<650		TTL-TS
M58981P-30	Mit	18-DIC	CMOS	0...+70	<220	<55µ	<300		TTL-TS
M58981P-45	Mit	18-DIC	CMOS	0...+70	<220	<55µ	<450		TTL-TS
M5L2114 LP	Mit	18-DIP	NMOS	0...+70	<357		<450		TTL-TS
M5L2114 LP-2	Mit	18-DIP	NMOS	0...+70	<357		<200		TTL-TS
M5L2114 LP-3	Mit	18-DIP	NMOS	0...+70	<357		<300		TTL-TS
M5L2114 LS	Mit	18-DIC	NMOS	0...+70	<357		<450		TTL-TS
M5L2114 LS-2	Mit	18-DIC	NMOS	0...+70	<357		<200		TTL-TS
M5L2114 LS-3	Mit	18-DIC	NMOS	0...+70	<357		<300		TTL-TS
MB 8114 E	Fui	18-DIP	NMOS	0...+70	<525		<200		TTL-TS
MB 8114 EL	Fui	18-DIP	NMOS	0...+70	<367		<200		TTL-TS

2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MB 8114 N	Fui	18-DIP	NMOS	0...+70	<525		<300		TTL-TS
MB 8114 NL	Fui	18-DIP	NMOS	0...+70	<367		<300		TTL-TS
MBM 2114 A-10L	Fui	18-DIP	NMOS	-10...+85	<220		<100		TTL-TS
MBM 2114 A-15L	Fui	18-DIP	NMOS	-10...+85	<220		<150		TTL-TS
MBM 2114 A-20	Fui	18-DIP	NMOS	-10...+85	<385		<200		TTL-TS
MBM 2114 A-20L	Fui	18-DIP	NMOS	-10...+85	<220		<200		TTL-TS
MBM 2114 A-4	Fui	18-DIP	NMOS	0...+70	<385		<200		TTL-TS
MBM 2114 A-5	Fui	18-DIP	NMOS	0...+70	<385		<250		TTL-TS
MBM 2114 AL-1	Fui	18-DIP	NMOS	0...+70	<220		<100		TTL-TS
MBM 2114 AL-2	Fui	18-DIP	NMOS	0...+70	<220		<120		TTL-TS
MBM 2114 AL-3	Fui	18-DIP	NMOS	0...+70	<220		<150		TTL-TS
MBM 2114 AL-4	Fui	18-DIP	NMOS	0...+70	<220		<200		TTL-TS
MCM 2114-20	Mot	18-DIP	NMOS	0...+70	<522		<200		TTL-TS
MCM 2114-25	Mot	18-DIP	NMOS	0...+70	<522		<250		TTL-TS
MCM 2114-30	Mot	18-DIP	NMOS	0...+70	<522		<300		TTL-TS
MCM 2114-45	Mot	18-DIP	NMOS	0...+70	<522		<450		TTL-TS
MCM 21L14-20	Mot	18-DIC	NMOS	0...+70	<357		<200		TTL-TS
MCM 21L14-25	Mot	18-DIC	NMOS	0...+70	<357		<250		TTL-TS
MCM 21L14-30	Mot	18-DIC	NMOS	0...+70	<357		<300		TTL-TS
MCM 21L14-45	Mot	18-DIC	NMOS	0...+70	<357		<450		TTL-TS
MM 2114 N	Nsc	18-DIP	NMOS	0...+70	<550		<450		TTL-TS
MM 2114 N-15	Nsc	18-DIP	NMOS	0...+70	<550		<150		TTL-TS
MM 2114 N-15 L	Nsc	18-DIP	NMOS	0...+70	<385		<150		TTL-TS
MM 2114 N-2	Nsc	18-DIP	NMOS	0...+70	<550		<200		TTL-TS
MM 2114 N-2 L	Nsc	18-DIP	NMOS	0...+70	<385		<200		TTL-TS
MM 2114 N-25	Nsc	18-DIP	NMOS	0...+70	<550		<250		TTL-TS
MM 2114 N-25 L	Nsc	18-DIP	NMOS	0...+70	<385		<250		TTL-TS
MM 2114 N-30	Nsc	18-DIP	NMOS	0...+70	<550		<300		TTL-TS
MM 2114 N-30 L	Nsc	18-DIP	NMOS	0...+70	<385		<300		TTL-TS
MM 2114 N-L	Nsc	18-DIP	NMOS	0...+70	<385		<450		TTL-TS
MSM 2114 RS	Oki	18-DIP	NMOS	0...+70	<396		<450		TTL-TS
MSM 2114 RS-2	Oki	18-DIP	NMOS	0...+70	<396		<300		TTL-TS
MSM 2114 RS-3	Oki	18-DIP	NMOS	0...+70	<396		<200		TTL-TS
MSM 5114-2RS	Oki	18-DIP	CMOS	0...+70	<33	<0,11	<200		TTL-TS
MSM 5114-3RS	Oki	18-DIP	CMOS	0...+70	<33	<0,11	<300		TTL-TS
MWS 5114-5 D	Rca	18-DIC	CMOS	0...+70	<24	<120µ	<650		TTL-TS
MWS 5114-5 E	Rca	18-DIP	CMOS	0...+70	<24	<120µ	<650		TTL-TS

2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MWS 5114 D	Rca	18-DIC	CMOS	0...+70	<24	<90µ	<650		TTL-TS
MWS 5114 E	Rca	18-DIP	CMOS	0...+70	<24	<90µ	<650		TTL-TS
NMC 2114 AJ	Nsc	18-DIC	NMOS	0...+70	<275		<120		TTL-TS
NMC 2114 AN	Nsc	18-DIP	NMOS	0...+70	<275		<120		TTL-TS
NMC 2114 APJ	Nsc	18-DIC	NMOS	0...+70	<82,5		<120		TTL-TS
NMC 2114 APN	Nsc	18-DIP	NMOS	0...+70	<82,5		<120		TTL-TS
TC 5114 AD-2	Tos	18-DIC	CMOS	-30...+85	<49,5	<0,11	<200		TTL-TS
TC 5114 AD-3	Tos	18-DIC	CMOS	-30...+85	<49,5	<0,11	<300		TTL-TS
TC 5114 AP-2	Tos	18-DIP	CMOS	-30...+85	<49,5	<0,11	<200		TTL-TS
TC 5114 AP-3	Tos	18-DIP	CMOS	-30...+85	<49,5	<0,11	<300		TTL-TS
TC 5114 DL-2	Tos	18-DIC	CMOS	-30...+85	<49,5	<5,5µ	<200		TTL-TS
TC 5114 DL-3	Tos	18-DIC	CMOS	-30...+85	<49,5	<5,5µ	<300		TTL-TS
TC 5114 PL-2	Tos	18-DIP	CMOS	-30...+85	<49,5	<5,5µ	<200		TTL-TS
TC 5114 PL-3	Tos	18-DIP	CMOS	-30...+85	<49,5	<5,5µ	<300		TTL-TS
TC 5514 AD	Tos	18-DIC	CMOS	-30...+85	<44	<0,11	<200		TTL-TS
TC 5514 AP	Tos	18-DIP	CMOS	-30...+85	<44	<0,11	<200		TTL-TS
TC 5514 D	Tos	18-DIC	CMOS	-30...+85	<137	<0,11	<450		TTL-TS
TC 5514 P	Tos	18-DIP	CMOS	-30...+85	<137	<0,11	<450		TTL-TS
TC 5514 P-1	Tos	18-DIP	CMOS	-30...+85	<110	<0,11	<650		TTL-TS
TC 5514 P-2	Tos	18-DIP	CMOS	-30...+85	<110	<0,11	<800		TTL-TS
TMM 314 AP	Tos	18-DIP	NMOS	0...+70	<550		<450		TTL-TS
TMM 314 AP-1	Tos	18-DIP	NMOS	0...+70	<550		<200		TTL-TS
TMM 314 AP-3	Tos	18-DIP	NMOS	0...+70	<495		<300		TTL-TS
TMM 314 APL	Tos	18-DIP	NMOS	0...+70	<385		<450		TTL-TS
TMM 314 APL-1	Tos	18-DIP	NMOS	0...+70	<385		<200		TTL-TS
TMM 314 APL-3	Tos	18-DIP	NMOS	0...+70	<352		<300		TTL-TS
TMS 2114-15 NL	Tix	18-DIP	NMOS	0...+70	<550		<150		TTL-TS
TMS 2114-20 NL	Tix	18-DIP	NMOS	0...+70	<550		<200		TTL-TS
TMS 2114-25 NL	Tix	18-DIP	NMOS	0...+70	<550		<250		TTL-TS
TMS 2114-45 NL	Tix	18-DIP	NMOS	0...+70	<525		<450		TTL-TS
TMS 2114 L-15 NL	Tix	18-DIP	NMOS	0...+70	<330		<150		TTL-TS
TMS 2114 L-20 NL	Tix	18-DIP	NMOS	0...+70	<330		<200		TTL-TS
TMS 2114 L-25 NL	Tix	18-DIP	NMOS	0...+70	<330		<250		TTL-TS
TMS 2114 L-45 NL	Tix	18-DIP	NMOS	0...+70	<315		<450		TTL-TS
TMS 4045-20 JL	Tix	18-DIC	NMOS	0...+70	<440		<200		TTL-TS
TMS 4045-20 NL	Tix	18-DIP	NMOS	0...+70	<440		<200		TTL-TS
TMS 40L45-25 NL	Tix	18-DIP	NMOS	0...+70	<385		<200		TTL-TS

2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 40L45-30	Tix	18-DIP	NMOS	0...+70	<385		<300		TTL-TS
TMS 4045-30 JL	Tix	18-DIC	NMOS	0...+70	<440		<300		TTL-TS
TMS 4045-30 NL	Tix	18-DIP	NMOS	0...+70	<440		<300		TTL-TS
TMS 40L45-45	Tix	18-DIP	NMOS	0...+70	<385		<450		TTL-TS
TMS 4045-45 JL	Tix	18-DIC	NMOS	0...+70	<440		<450		TTL-TS
TMS 4045-45 NL	Tix	18-DIP	NMOS	0...+70	<440		<450		TTL-TS
2114	Int	18-DIP	NMOS	0...+70	<630		<450		TTL-TS
2114-2	Int	18-DIP	NMOS	0...+70	<630		<200		TTL-TS
2114-3	Int	18-DIP	NMOS	0...+70	<630		<300		TTL-TS
2114 A-4	Int	18-DIP	NMOS	0...+70	<385		<200		TTL-TS
2114 A-5	Int	18-DIP	NMOS	0...+70	<385		<250		TTL-TS
2114 AL-1	Int	18-DIP	NMOS	0...+70	<220		<100		TTL-TS
2114 AL-2	Int	18-DIP	NMOS	0...+70	<220		<120		TTL-TS
2114 AL-3	Int	18-DIP	NMOS	0...+70	<220		<150		TTL-TS
2114 AL-4	Int	18-DIP	NMOS	0...+70	<220		<200		TTL-TS
2114 L	Int	18-DIP	NMOS	0...+70	<341		<450		TTL-TS
2114 L-3	Int	18-DIP	NMOS	0...+70	<341		<300		TTL-TS
93475 DC	Fch	18-DIC	TTL	0...+75	700		35		TTL-TS
93475 DM	Fch	18-DIC	TTL	-55...+125	700		35		TTL-TS
93475 FC	Fch	18-FLAT	TTL	0...+75	700		35		TTL-TS
93475 PC	Fch	18-DIP	TTL	0...+75	700		35		TTL-TS
µPD 444 C	Nip	18-DIP	CMOS	-40...+85	<220	<0,275	<450		TTL-TS
µPD 444 C-1	Nip	18-DIP	CMOS	-40...+85	<220	<0,275	<300		TTL-TS
µPD 444 C-2	Nip	18-DIP	CMOS	-40...+85	<220	<0,275	<250		TTL-TS
µPD 444 C-3	Nip	18-DIP	CMOS	-40...+85	<220	<0,275	<200		TTL-TS
µPD 444 C-L	Nip	18-DIP	CMOS	-20...+70	<220	<0,055	<2000		TTL-TS
µPD 2114 LC	Nip	18-DIP	NMOS	0...+70	<357		<450		TTL-TS
µPD 2114 LC-1	Nip	18-DIP	NMOS	0...+70	<357		<300		TTL-TS
µPD 2114 LC-2	Nip	18-DIP	NMOS	0...+70	<357		<250		TTL-TS
µPD 2114 LC-3	Nip	18-DIP	NMOS	0...+70	<357		<200		TTL-TS
µPD 2114 LC-5	Nip	18-DIP	NMOS	0...+70	<357		<150		TTL-TS
µPD 2114 LD	Nip	18-DIC	NMOS	0...+70	<357		<450		TTL-TS
µPD 2114 LD-1	Nip	18-DIC	NMOS	0...+70	<357		<300		TTL-TS
µPD 2114 LD-2	Nip	18-DIC	NMOS	0...+70	<357		<250		TTL-TS
µPD 2114 LD-3	Nip	18-DIC	NMOS	0...+70	<357		<200		TTL-TS
µPD 2114 LD-5	Nip	18-DIC	NMOS	0...+70	<357		<150		TTL-TS

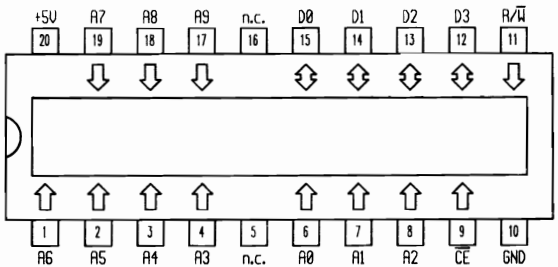
2114 — 1024x4-Bit static RAM



$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCD 5114 D	Val	18-DIC	CMOS	-25...+70	<110	<27,5µ	<200		TTL-TS
PCD 5114 P	Val	18-DIP	CMOS	-25...+70	<110	<27,5µ	<200		TTL-TS

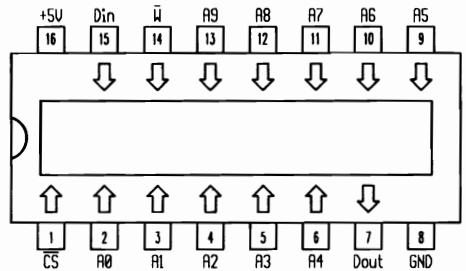
2114 — 1024x4-Bit static RAM



$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

2114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCD 5114 T	Val	20-FLAT	CMOS	-25...+70	<110	<27,5µ	<200		TTL-S

2115 — 1024x1-Bit static RAM

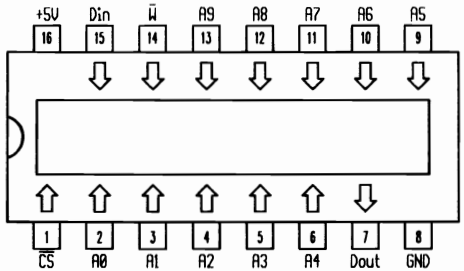


$\overline{CS}$	$\overline{W}$	D_{In}	D_{out}	Mode
H	X	X	H	not selected
L	L	L	H	write 0
L	L	H	H	write 1
L	H	X	data out	read

2115 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MB 8115 E	Fui	16-DIP	NMOS	0...+75	<341		<95		TTL-OC
MB 8115 H	Fui	16-DIP	NMOS	0...+75	<525		<70		TTL-OC
MB 8115 N	Fui	16-DIP	NMOS	0...+75	<341		<120		TTL-OC
MB 8115 Y	Fui	16-DIP	NMOS	0...+75	<656		<45		TTL-OC
MCM 2115 AC-45	Mot	16-DIC	NMOS	0...+70	<625		<45		TTL-OC
MCM 2115 AC-55	Mot	16-DIC	NMOS	0...+70	<625		<55		TTL-OC
MCM 2115 AC-70	Mot	16-DIC	NMOS	0...+70	<625		<70		TTL-OC
MCM 2115 HC-20	Mot	16-DIC	NMOS				<20		TTL-OC

2115 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 2115 HC-25	Mot	16-DIC	NMOS				<25		TTL-OC
MCM 2115 HC-30	Mot	16-DIC	NMOS				<30		TTL-OC
MCM 2115 HC-35	Mot	16-DIC	NMOS				<35		TTL-OC
MCM 21L15 A-45	Mot	16-DIC	NMOS	0...+70	<375		<45		TTL-OC
MCM 21L15 A-55	Mot	16-DIC	NMOS	0...+70	<375		<55		TTL-OC
MCM 21L15 A-70	Mot	16-DIC	NMOS	0...+70	<375		<70		TTL-OC
N 2115 F	Sig	16-DIC	NMOS	0...+70	<525		<45		TTL-OC
N 2115L F	Sig	16-DIC	NMOS	0...+70	<314		<50		TTL-OC
N 2115 I	Sig	16-DIC	NMOS	0...+70	<525		<45		TTL-OC
N 2115L I	Sig	16-DIC	NMOS	0...+70	<314		<50		TTL-OC
N 2115 N	Sig	16-DIP	NMOS	0...+70	<525		<45		TTL-OC
N 2115L N	Sig	16-DIP	NMOS	0...+70	<314		<50		TTL-OC
2115	Int	16-DIP	NMOS	0...+75	<525		<95		TTL-OC
2115-2	Int	16-DIP	NMOS	0...+75	<656		<70		TTL-OC
2115 A	Int	16-DIP	NMOS	0...+75	<656		<45		TTL-OC
2115 A-2	Int	16-DIP	NMOS	0...+75	<656		<70		TTL-OC
2115 AL	Int	16-DIP	NMOS	0...+75	<394		<45		TTL-OC
2115 AL-2	Int	16-DIP	NMOS	0...+75	<394		<70		TTL-OC
2115 H-1	Int	16-DIP	NMOS	0...+75	<656		<20		TTL-OC
2115 H-2	Int	16-DIP	NMOS	0...+75	<656		<25		TTL-OC
2115 H-3	Int	16-DIP	NMOS	0...+75	<525		<30		TTL-OC
2115 H-4	Int	16-DIP	NMOS	0...+75	<656		<35		TTL-OC
2115 L	Int	16-DIP	NMOS	0...+75	<341		<95		TTL-OC

2125 — 1024x1-Bit static RAM

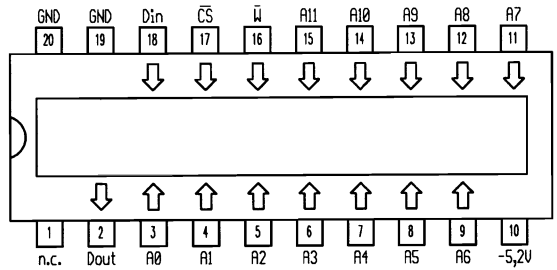


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

2125 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MB 8125 E	Fui	16-DIP	NMOS	0...+75	<341		<95		TTL-TS
MB 8125 H	Fui	16-DIP	NMOS	0...+75	<525		<70		TTL-TS
MB 8125 N	Fui	16-DIP	NMOS	0...+75	<341		<120		TTL-TS
MB 8125 Y	Fui	16-DIP	NMOS	0...+75	<656		<45		TTL-TS
MCM 2125 AC-45	Mot	16-DIC	NMOS	0...+70	<625		<45		TTL-TS
MCM 2125 AC-55	Mot	16-DIC	NMOS	0...+70	<625		<55		TTL-TS
MCM 2125 AC-70	Mot	16-DIC	NMOS	0...+70	<625		<70		TTL-TS
MCM 2125 HC-20	Mot	16-DIC	NMOS				<20		TTL-TS

2125 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 2125 HC-25	Mot	16-DIC	NMOS				<25		TTL-TS
MCM 2125 HC-30	Mot	16-DIC	NMOS				<30		TTL-TS
MCM 2125 HC-35	Mot	16-DIC	NMOS				<35		TTL-TS
MCM 21L25 AC-45	Mot	16-DIC	NMOS	0...+70	<375		<45		TTL-TS
MCM 21L25 AC-55	Mot	16-DIC	NMOS	0...+70	<375		<55		TTL-TS
MCM 21L25 AC-70	Mot	16-DIC	NMOS	0...+70	<375		<70		TTL-TS
MCM 93425 DC-35	Mot	16-DIC	TTL	0...+75	$0,5		35		TTL-TS
MCM 93425 DM-35	Mot	16-DIC	TTL	-55...+125	$0,5		35		TTL-TS
MCM 93425 FM-35	Mot	16-FLAT	TTL	-55...+125	$0,5		35		TTL-TS
MCM 93425 PC-35	Mot	16-DIP	TTL	0...+75	$0,5		35		TTL-TS
N 2125 F	Sig	16-DIC	NMOS	0...+70	<525		<45		TTL-TS
N 2125L F	Sig	16-DIC	NMOS	0...+70	<314		<50		TTL-TS
N 2125 I	Sig	16-DIC	NMOS	0...+70	<525		<45		TTL-TS
N 2125L I	Sig	16-DIC	NMOS	0...+70	<314		<50		TTL-TS
N 2125 N	Sig	16-DIP	NMOS	0...+70	<525		<45		TTL-TS
N 2125L N	Sig	16-DIP	NMOS	0...+70	<314		<50		TTL-TS
N 93425A F	Sig	16-DIC	TTL	0...+75	<814		<45		TTL-TS
N 93425A N	Sig	16-DIP	TTL	0...+75	<814		<45		TTL-TS
2125	Int	16-DIP	NMOS	0...+75	<525		<95		TTL-TS
2125-2	Int	16-DIP	NMOS	0...+75	<656		<70		TTL-TS
2125 A	Int	16-DIP	NMOS	0...+75	<656		<45		TTL-TS
2125 A-2	Int	16-DIP	NMOS	0...+75	<656		<70		TTL-TS
2125 AL	Int	16-DIP	NMOS	0...+75	<394		<45		TTL-TS
2125 AL-2	Int	16-DIP	NMOS	0...+75	<394		<70		TTL-TS
2125 H-1	Int	16-DIP	NMOS	0...+75	<788		<20		TTL-TS
2125 H-2	Int	16-DIP	NMOS	0...+75	<788		<25		TTL-TS
2125 H-3	Int	16-DIP	NMOS	0...+75	<788		<30		TTL-TS
2125 H-4	Int	16-DIP	NMOS	0...+75	<788		<35		TTL-TS
2125 L	Int	16-DIP	NMOS	0...+75	<341		<95		TTL-TS

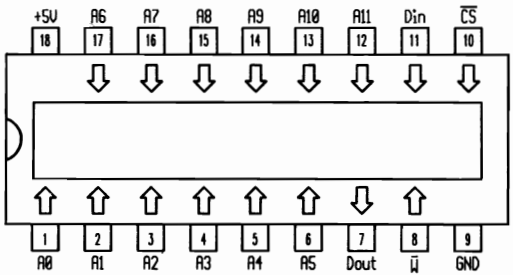
2142 — 4096x1-Bit ECL RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

2142 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 2142	Hit	20-DIC	ECL	0...+75	$0,3		<10		ECL

2147 — 4096x1-Bit static RAM



CS	W	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2147-35	Amd	18-DIP	NMOS	0...+70	<990		<35		TTL-TS
Am 2147-45	Amd	18-DIP	NMOS	0...+70	<990		<45		TTL-TS
Am 2147-55	Amd	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
Am 2147-70	Amd	18-DIP	NMOS	0...+70	<880		<70		TTL-TS
Am 21L47-12	Amd	18-DIP	NMOS	0...+70	<302		<120		TTL-TS
Am 21L47-15	Amd	18-DIP	NMOS	0...+70	<220		<150		TTL-TS
Am 21L47-20	Amd	18-DIP	NMOS	0...+70	<220		<200		TTL-TS
Am 21L47-25	Amd	18-DIP	NMOS	0...+70	<220		<250		TTL-TS

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 21L47-45	Amd	18-DIP	NMOS	0...+70	<687		<45		TTL-TS
Am 21L47-55	Amd	18-DIP	NMOS	0...+70	<687		<55		TTL-TS
Am 9044 B	Amd	18-DIP	NMOS	0...+70	<440		<450		TTL-TS
Am 9044 C	Amd	18-DIP	NMOS	0...+70	<440		<300		TTL-TS
Am 9044 D	Amd	18-DIP	NMOS	0...+70	<440		<250		TTL-TS
Am 9044 E	Amd	18-DIP	NMOS	0...+70	<440		<200		TTL-TS
Am 90L44 B	Amd	18-DIP	NMOS	0...+70	<330		<450		TTL-TS
Am 90L44 C	Amd	18-DIP	NMOS	0...+70	<330		<300		TTL-TS
Am 90L44 D	Amd	18-DIP	NMOS	0...+70	<330		<250		TTL-TS
Am 90L44 E	Amd	18-DIP	NMOS	0...+70	<330		<200		TTL-TS
C 2147 A	Int	18-DIP	NMOS	0...+70	<275		<70		TTL-TS
C 2147 A-3	Int	18-DIP	NMOS	0...+70	<275		<55		TTL-TS
C 2147 AL	Int	18-DIP	NMOS	0...+70	<192		<70		TTL-TS
C 2147 AL-3	Int	18-DIP	NMOS	0...+70	<192		<55		TTL-TS
C 2147 H-2	Int	18-DIP	NMOS	0...+70	<990		<45		TTL-TS
C 2147 H-3	Int	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
ET 2147 HJ-1	Tho	18-DIC	NMOS	0...+70	<990	<165	<35		TTL-TS
ET 2147 HJ-2	Tho	18-DIC	NMOS	0...+70	<990	<165	<45		TTL-TS
ET 2147 HJ-3	Tho	18-DIC	NMOS	0...+70	<990	<165	<55		TTL-TS
ETL 2147 HJ-3	Tho	18-DIC	NMOS	0...+70	<687,5	<110	<55		TTL-TS
HN 4847	Hit	18-DIC	NMOS	0...+70	<840		<70		TTL-TS
HN 4847-2	Hit	18-DIC	NMOS	0...+70	<945		<45		TTL-TS
HN 4847-3	Hit	18-DIC	NMOS	0...+70	<892		<55		TTL-TS
HM 6147	Hit	18-DIC	CMOS	0...+70	75	100µ	<70		TTL-TS
HM 6147-3	Hit	18-DIC	CMOS	0...+70	75	100µ	<55		TTL-TS
HM 6147 H-35	Hit	18-DIC	CMOS	0...+70	150	0,1	<35		TTL-TS
HM 6147 H-45	Hit	18-DIC	CMOS	0...+70	150	0,1	<45		TTL-TS
HM 6147 HLP-35	Hit	18-DIP	CMOS	0...+70	150	5µ	<35		TTL-TS
HM 6147 HLP-45	Hit	18-DIP	CMOS	0...+70	150	5µ	<45		TTL-TS
HM 6147 HLP-55	Hit	18-DIP	CMOS	0...+70	<440	<0,55	<55		TTL-TS
HM 6147 HP-35	Hit	18-DIP	CMOS	0...+70	150	0,1	<35		TTL-TS
HM 6147 HP-45	Hit	18-DIP	CMOS	0...+70	150	0,1	<45		TTL-TS
HM 6147 HP-55	Hit	18-DIP	CMOS	0...+70	<440	<5,5	<55		TTL-TS
HM 6147 LP	Hit	18-DIP	CMOS	0...+70	75	5µ	<70		TTL-TS
HM 6147 LP-3	Hit	18-DIP	CMOS	0...+70	75	5µ	<55		TTL-TS
HM 6147 P	Hit	18-DIP	CMOS	0...+70	75	100µ	<70		TTL-TS
HM 6147 P-3	Hit	18-DIP	CMOS	0...+70	75	100µ	<55		TTL-TS

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IM 2147	Isi	18-DIP	NMOS	0...+70	<880		<70		TTL-TS
IM 2147-3	Isi	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
IM 2147 L	Isi	18-DIP	NMOS	0...+70	<770		<70		TTL-TS
IM 7141 2CDN	Isi	18-DIC	NMOS	0...+70	<262		<200		TTL-TS
IM 7141 2CPN	Isi	18-DIP	NMOS	0...+70	<262		<200		TTL-TS
IM 7141 3CDN	Isi	18-DIC	NMOS	0...+70	<262		<300		TTL-TS
IM 7141 3CPN	Isi	18-DIP	NMOS	0...+70	<262		<300		TTL-TS
IM 7141 CDN	Isi	18-DIC	NMOS	0...+70	<262		<450		TTL-TS
IM 7141 CPN	Isi	18-DIP	NMOS	0...+70	<262		<450		TTL-TS
IM 7141 L2CDN	Isi	18-DIC	NMOS	0...+70	<367		<200		TTL-TS
IM 7141 L3CDN	Isi	18-DIC	NMOS	0...+70	<367		<300		TTL-TS
IM 7141 L2CPN	Isi	18-DIP	NMOS	0...+70	<367		<200		TTL-TS
IM 7141 L3CPN	Isi	18-DIP	NMOS	0...+70	<367		<300		TTL-TS
IM 7141 LCDN	Isi	18-DIC	NMOS	0...+70	<367		<450		TTL-TS
IM 7141 LCPN	Isi	18-DIP	NMOS	0...+70	<367		<450		TTL-TS
IMS 1203 P-25	Inm	18-DIP	CMOS	0...+70	<440	<82,5	<25		TTL-TS
IMS 1203 P-35	Inm	18-DIP	CMOS	0...+70	<440	<82,5	<35		TTL-TS
IMS 1203 P-45	Inm	18-DIP	CMOS	0...+70	<440	<82,5	<45		TTL-TS
IMS 1203 S-25	Inm	18-DIC	CMOS	0...+70	<440	<82,5	<25		TTL-TS
IMS 1203 S-25M	Inm	18-DIC	CMOS	-55...+125	<440	<82,5	<25		TTL-TS
IMS 1203 S-35	Inm	18-DIC	CMOS	0...+70	<440	<82,5	<35		TTL-TS
IMS 1203 S-35M	Inm	18-DIC	CMOS	-55...+125	<440	<82,5	<35		TTL-TS
IMS 1203 S-45	Inm	18-DIC	CMOS	0...+70	<440	<82,5	<45		TTL-TS
IMS 1203 S-45M	Inm	18-DIC	CMOS	-55...+125	<440	<82,5	<45		TTL-TS
M5T4044 P-20	Mit	18-DIP	NMOS	0...+70	<357		<200		TTL-TS
M5T4044 P-30	Mit	18-DIP	NMOS	0...+70	<357		<300		TTL-TS
M5T4044 P-45	Mit	18-DIP	NMOS	0...+70	<357		<450		TTL-TS
M5T4044 S-20	Mit	18-DIC	NMOS	0...+70	<357		<200		TTL-TS
M5T4044 S-30	Mit	18-DIC	NMOS	0...+70	<357		<300		TTL-TS
M5T4044 S-45	Mit	18-DIC	NMOS	0...+70	<357		<450		TTL-TS
MB 8144 E	Fui	18-DIP	NMOS	0...+70	<495		<200		TTL-TS
MB 8144 EL	Fui	18-DIC	NMOS	0...+70	<495		<200		TTL-TS
MB 8144 N	Fui	18-DIP	NMOS	0...+70	<385		<300		TTL-TS
MB 8144 NL	Fui	18-DIC	NMOS	0...+70	<385		<300		TTL-TS
MB 8147 E	Fui	18-DIP	NMOS	0...+70	<880		<70		TTL-TS
MB 8147 F-35	Fui	18-DIP	NMOS	0...+70	<990		<35		TTL-TS
MB 8147 F-45	Fui	18-DIP	NMOS	0...+70	<990		<45		TTL-TS

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MB 8147 H	Fui	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
MB 8147 N	Fui	18-DIP	NMOS	0...+70	<880		<95		TTL-TS
MCM 2147 C-100	Mot	18-DIC	NMOS	0...+70	<550	<100	<100		TTL-TS
MCM 2147 C-55	Mot	18-DIC	NMOS	0...+70	<850	<150	<55		TTL-TS
MCM 2147 C-70	Mot	18-DIC	NMOS	0...+70	<750	<100	<70		TTL-TS
MCM 2147 C-85	Mot	18-DIC	NMOS	0...+70	<650	<125	<85		TTL-TS
MCM 2147 HC-35	Mot	18-DIC	NMOS				<35		TTL-TS
MCM 2147 HC-45	Mot	18-DIC	NMOS				<45		TTL-TS
MCM 2147 HC-55	Mot	18-DIC	NMOS				<55		TTL-TS
MCM 2147 P-100	Mot	18-DIP	NMOS	0...+70	<550	<100	<100		TTL-TS
MCM 2147 P-55	Mot	18-DIP	NMOS	0...+70	<850	<150	<55		TTL-TS
MCM 2147 P-70	Mot	18-DIP	NMOS	0...+70	<750	<100	<70		TTL-TS
MCM 2147 P-85	Mot	18-DIP	NMOS	0...+70	<650	<125	<85		TTL-TS
MCM 6641 C-20	Mot	18-DIC	NMOS	0...+70	<550	<125	<200		TTL-TS
MCM 6641 C-25	Mot	18-DIC	NMOS	0...+70	<550	<125	<250		TTL-TS
MCM 6641 C-30	Mot	18-DIC	NMOS	0...+70	<550	<125	<300		TTL-TS
MCM 6641 C-45	Mot	18-DIC	NMOS	0...+70	<550	<125	<450		TTL-TS
MCM 66L41 C-20	Mot	18-DIC	NMOS	0...+70	<385	<125	<200		TTL-TS
MCM 66L41 C-25	Mot	18-DIC	NMOS	0...+70	<385	<125	<250		TTL-TS
MCM 66L41 C-30	Mot	18-DIC	NMOS	0...+70	<385	<125	<300		TTL-TS
MCM 66L41 C-45	Mot	18-DIC	NMOS	0...+70	<385	<125	<450		TTL-TS
MCM 66L41 P-20	Mot	18-DIP	NMOS	0...+70	<385	<125	<200		TTL-TS
MCM 66L41 P-25	Mot	18-DIP	NMOS	0...+70	<385	<125	<250		TTL-TS
MCM 66L41 P-30	Mot	18-DIP	NMOS	0...+70	<385	<125	<300		TTL-TS
MCM 66L41 P-45	Mot	18-DIP	NMOS	0...+70	<385	<125	<450		TTL-TS
MCM 6641 P-20	Mot	18-DIP	NMOS	0...+70	<550	<125	<200		TTL-TS
MCM 6641 P-25	Mot	18-DIP	NMOS	0...+70	<550	<125	<250		TTL-TS
MCM 6641 P-30	Mot	18-DIP	NMOS	0...+70	<550	<125	<300		TTL-TS
MCM 6641 P-45	Mot	18-DIP	NMOS	0...+70	<550	<125	<450		TTL-TS
MCM 65147 C-55	Mot	18-DIC	CMOS	0...+70	75	0,5	<55		TTL-TS
MCM 65147 C-70	Mot	18-DIC	CMOS	0...+70	75	0,5	<70		TTL-TS
MCM 65147 L-55	Mot	18-DIC	CMOS	0...+70	75	0,5	<55		TTL-TS
MCM 65147 L-70	Mot	18-DIC	CMOS	0...+70	75	0,5	<70		TTL-TS
MK 2147 J-55	Mos	18-DIC	NMOS	0...+70	<990	<165	<55		TTL-TS
MK 2147 J-70	Mos	18-DIC	NMOS	0...+70	<880	<110	<70		TTL-TS
MK 2147 J-90	Mos	18-DIC	NMOS	0...+70	<880	<110	<90		TTL-TS
MK 2147 N-55	Mos	18-DIP	NMOS	0...+70	<990	<165	<55		TTL-TS

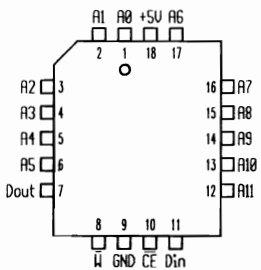
2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 2147 N-70	Mos	18-DIP	NMOS	0...+70	<880	<110	<70		TTL-TS
MK 2147 N-90	Mos	18-DIP	NMOS	0...+70	<880	<110	<90		TTL-TS
MK 4104 J-3	Mos	18-DIC	NMOS	0...+70	<150	<28	<200		TTL-TS
MK 4104 J-4	Mos	18-DIC	NMOS	0...+70	<150	<28	<250		TTL-TS
MK 4104 J-5	Mos	18-DIC	NMOS	0...+70	<150	<28	<300		TTL-TS
MK 4104 N-3	Mos	18-DIP	NMOS	0...+70	<150	<28	<200		TTL-TS
MK 4104 N-33	Mos	18-DIP	NMOS	0...+70	<150	<28	<200		TTL-TS
MK 4104 N-34	Mos	18-DIP	NMOS	0...+70	<150	<28	<250		TTL-TS
MK 4104 N-35	Mos	18-DIP	NMOS	0...+70	<150	<28	<300		TTL-TS
MK 4104 N-4	Mos	18-DIP	NMOS	0...+70	<150	<28	<250		TTL-TS
MK 4104 N-5	Mos	18-DIP	NMOS	0...+70	<150	<28	<300		TTL-TS
MK 4104 N-6	Mos	18-DIP	NMOS	0...+70	<150	<28	<350		TTL-TS
MKB 4104 J-3	Mos	18-DIC	NMOS	0...+70	<148	<27,5	<200		TTL-TS
MKB 4104 J-33	Mos	18-DIC	NMOS	0...+70	<148	<27,5	<200		TTL-TS
MKB 4104 J-34	Mos	18-DIC	NMOS	0...+70	<148	<27,5	<250		TTL-TS
MKB 4104 J-35	Mos	18-DIC	NMOS	0...+70	<148	<27,5	<300		TTL-TS
MKB 4104 J-4	Mos	18-DIC	NMOS	0...+70	<148	<27,5	<250		TTL-TS
MKB 4104 J-5	Mos	18-DIC	NMOS	0...+70	<148	<27,5	<300		TTL-TS
MKB 4104 J-6	Mos	18-DIC	NMOS	0...+70	<148	<27,5	<350		TTL-TS
MKB 4104 J-85	Mos	18-DIC	NMOS	-55...+85	<148	<53	<300		TTL-TS
MKB 4104 J-86	Mos	18-DIC	NMOS	-55...+85	<148	<53	<350		TTL-TS
MKB 4104 P-85	Mos	18-DIP	NMOS	-55...+85	<148	<53	<300		TTL-TS
MKB 4104 P-86	Mos	18-DIP	NMOS	-55...+85	<148	<53	<350		TTL-TS
MM 2147-3J	Nsc	18-DIC	NMOS	0...+70	<385		<55		TTL-TS
MM 2147-3N	Nsc	18-DIP	NMOS	0...+70	<385		<55		TTL-TS
MM 2147 J	Nsc	18-DIC	NMOS	0...+70	<275		<70		TTL-TS
MM 2147 L-1J	Nsc	18-DIC	NMOS	0...+70	<165		<90		TTL-TS
MM 2147 L-1N	Nsc	18-DIP	NMOS	0...+70	<165		<90		TTL-TS
MM 2147 LJ	Nsc	18-DIC	NMOS	0...+70	<165		<70		TTL-TS
MM 2147 LN	Nsc	18-DIP	NMOS	0...+70	<165		<70		TTL-TS
MM 2147 N	Nsc	18-DIP	NMOS	0...+70	<275		<70		TTL-TS
MM 5247-25 J	Nsc	18-DIC	NMOS	0...+70	<472		<250		TTL-TS
MM 5247-25 LJ	Nsc	18-DIC	NMOS	0...+70	<341		<250		TTL-TS
MM 5247-2 J	Nsc	18-DIC	NMOS	0...+70	<472		<200		TTL-TS
MM 5247-2 LJ	Nsc	18-DIC	NMOS	0...+70	<341		<200		TTL-TS
MM 5247-3 J	Nsc	18-DIC	NMOS	0...+70	<472		<300		TTL-TS
MM 5247-3 LJ	Nsc	18-DIC	NMOS	0...+70	<341		<300		TTL-TS

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MM 5247 J	Nsc	18-DIC	NMOS	0...+70	<472		<450		TTL-TS
MM 5247 LJ	Nsc	18-DIC	NMOS	0...+70	<341		<450		TTL-TS
MM 5257-25 N	Nsc	18-DIP	NMOS	0...+70	<472		<250		TTL-TS
MM 5257-2 N	Nsc	18-DIP	NMOS	0...+70	<472		<200		TTL-TS
MM 5257-3 N	Nsc	18-DIP	NMOS	0...+70	<472		<300		TTL-TS
MM 5257-25 LN	Nsc	18-DIP	NMOS	0...+70	<341		<250		TTL-TS
MM 5257-2 LN	Nsc	18-DIP	NMOS	0...+70	<341		<200		TTL-TS
MM 5257-3 LN	Nsc	18-DIP	NMOS	0...+70	<341		<300		TTL-TS
MM 5257 LN	Nsc	18-DIP	NMOS	0...+70	<341		<450		TTL-TS
MM 5257 N	Nsc	18-DIP	NMOS	0...+70	<472		<450		TTL-TS
MN 2147 H-5	Mat	18-DIP	NMOS	0...+70	<945		<55		TTL-TS
MN 2147 H-7	Mat	18-DIP	NMOS	0...+70	<840		<70		TTL-TS
MN 2147 H-8	Mat	18-DIP	NMOS	0...+70	<840		<85		TTL-TS
NMC 2141 J	Nsc	18-DIC	NMOS	0...+70	<550		<120		TTL-TS
NMC 2141 N	Nsc	18-DIP	NMOS	0...+70	<550		<120		TTL-TS
NMC 2147 HJ	Nsc	18-DIC	NMOS	0...+70	<880	<110	<70		TTL-TS
NMC 2147 HJ-1	Nsc	18-DIC	NMOS	0...+70	<990	<165	<35		TTL-TS
NMC 2147 HJ-2	Nsc	18-DIC	NMOS	0...+70	<990	<165	<45		TTL-TS
NMC 2147 HJ-3	Nsc	18-DIC	NMOS	0...+70	<990	<165	<55		TTL-TS
NMC 2147 HJ-3L	Nsc	18-DIC	NMOS	0...+70	<688	<110	<55		TTL-TS
NMC 2147 HN	Nsc	18-DIP	NMOS	0...+70	<880	<110	<70		TTL-TS
NMC 2147 HN-1	Nsc	18-DIP	NMOS	0...+70	<990	<165	<35		TTL-TS
NMC 2147 HN-2	Nsc	18-DIP	NMOS	0...+70	<990	<165	<45		TTL-TS
NMC 2147 HN-3	Nsc	18-DIP	NMOS	0...+70	<990	<165	<55		TTL-TS
NMC 2147 HN-3L	Nsc	18-DIP	NMOS	0...+70	<688	<110	<55		TTL-TS
NMC 5257 AJ	Nsc	18-DIC	NMOS	0...+70	<550		<120		TTL-TS
NMC 5257 AN	Nsc	18-DIP	NMOS	0...+70	<550		<120		TTL-TS
TMM 315 D	Tos	18-DIC	NMOS	0...+70	<105		<70		TTL-TS
TMM 315 D-1	Tos	18-DIC	NMOS	0...+70	<157		<55		TTL-TS
TMS 2147 H-3 JL	Tix	18-DIC	NMOS	0...+70	<660	<165	<35		TTL-TS
TMS 2147 H-3 NL	Tix	18-DIP	NMOS	0...+70	<660	<165	<35		TTL-TS
TMS 2147 H-4 JL	Tix	18-DIC	NMOS	0...+70	<660	<165	<45		TTL-TS
TMS 2147 H-4 NL	Tix	18-DIP	NMOS	0...+70	<660	<165	<45		TTL-TS
TMS 2147 H-5 JL	Tix	18-DIC	NMOS	0...+70	<660	<165	<55		TTL-TS
TMS 2147 H-5 NL	Tix	18-DIP	NMOS	0...+70	<660	<165	<55		TTL-TS
TMS 2147 H-7 JL	Tix	18-DIC	NMOS	0...+70	<660	<165	<70		TTL-TS
TMS 2147 H-7 NL	Tix	18-DIP	NMOS	0...+70	<660	<165	<70		TTL-TS

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 21L47-7	Tix	18-DIP	NMOS	0...+70	<770		<70		TTL-TS
TMS 4044-12 NL	Tix	18-DIP	NMOS	0...+70	<303	<84	<120		TTL-TS
TMS 4044-15 JL	Tix	18-DIC	NMOS	0...+70	<649		<150		TTL-TS
TMS 4044-15 NL	Tix	18-DIP	NMOS	0...+70	<649		<150		TTL-TS
TMS 4044-20 JL	Tix	18-DIC	NMOS	0...+70	<303	<84	<200		TTL-TS
TMS 4044-20 NL	Tix	18-DIP	NMOS	0...+70	<303	<84	<200		TTL-TS
TMS 4044-25 JL	Tix	18-DIC	NMOS	0...+70	<303	<84	<250		TTL-TS
TMS 4044-25 NL	Tix	18-DIP	NMOS	0...+70	<303	<84	<250		TTL-TS
TMS 4044-30 JL	Tix	18-DIC	NMOS	0...+70	<495		<300		TTL-TS
TMS 4044-30 NL	Tix	18-DIP	NMOS	0...+70	<495		<300		TTL-TS
TMS 4044-45 JL	Tix	18-DIC	NMOS	0...+70	<303	<84	<450		TTL-TS
TMS 4044-45 NL	Tix	18-DIP	NMOS	0...+70	<303	<84	<450		TTL-TS
TMS 40L44-12 NL	Tix	18-DIP	NMOS	0...+70	<220	<60	<120		TTL-TS
TMS 40L44-15	Tix	18-DIP	NMOS	0...+70	<275		<150		TTL-TS
TMS 40L44-20 NL	Tix	18-DIP	NMOS	0...+70	<220	<60	<200		TTL-TS
TMS 40L44-25 NL	Tix	18-DIP	NMOS	0...+70	<220	<60	<250		TTL-TS
TMS 40L44-45 NL	Tix	18-DIP	NMOS	0...+70	<220	<60	<450		TTL-TS
2141-2	Int	18-DIP	NMOS	0...+70	<385		<120		TTL-TS
2141-3	Int	18-DIP	NMOS	0...+70	<385		<150		TTL-TS
2141-4	Int	18-DIP	NMOS	0...+70	<302		<200		TTL-TS
2141-5	Int	18-DIP	NMOS	0...+70	<302		<250		TTL-TS
2141 L-3	Int	18-DIP	NMOS	0...+70	<220		<150		TTL-TS
2141 L-4	Int	18-DIP	NMOS	0...+70	<220		<200		TTL-TS
2141 L-5	Int	18-DIP	NMOS	0...+70	<220		<250		TTL-TS
2147	Int	18-DIP	NMOS	0...+70	<880		<85		TTL-TS
2147	Isi	18-DIC	NMOS	0...+70	<990		<70		TTL-TS
2147-3	Isi	18-DIC	NMOS	0...+70	<990		<55		TTL-TS
2147-6	Int	18-DIP	NMOS	0...+70	<770		<70		TTL-TS
2147 H	Int	18-DIP	NMOS	0...+70	<880		<70		TTL-TS
2147 H-1	Int	18-DIP	NMOS	0...+70	<990		<35		TTL-TS
2147 H-2	Int	18-DIP	NMOS	0...+70	<990		<45		TTL-TS
2147 H-3	Int	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
2147 H-4	Int	18-DIP	NMOS	0...+70	<687		<55		TTL-TS
2147 HL	Int	18-DIP	NMOS	0...+70	<770		<70		TTL-TS
2147 HL-3	Int	18-DIP	NMOS	0...+70	<687		<55		TTL-TS
µPD 2147 AD-25	Nip	18-DIC	NMOS	0...+70	<825	<275	<25		TTL-TS
µPD 2147 AD-35	Nip	18-DIC	NMOS	0...+70	<825	<275	<35		TTL-TS

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 2147 AD-45	Nip	18-DIC	NMOS	0...+70	<825	<275	<45		TTL-TS
µPD 2147 D-2	Nip	18-DIC	NMOS	0...+70	<825	<275	<70		TTL-TS
µPD 2147 D-3	Nip	18-DIC	NMOS	0...+70	<825	<275	<55		TTL-TS
µPD 2147 D-5	Nip	18-DIC	NMOS	0...+70	<825	<275	<45		TTL-TS

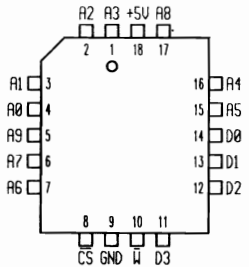
2147 — 4096x1-Bit static RAM



$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 2147 H-3 FPL	Tix	18-PLCC	NMOS	0...+70	<660	<165	<35		TTL-TS
TMS 2147 H-4 FPL	Tix	18-PLCC	NMOS	0...+70	<660	<165	<45		TTL-TS
TMS 2147 H-5 FPL	Tix	18-PLCC	NMOS	0...+70	<660	<165	<55		TTL-TS
TMS 2147 H-7 FPL	Tix	18-PLCC	NMOS	0...+70	<660	<165	<70		TTL-TS

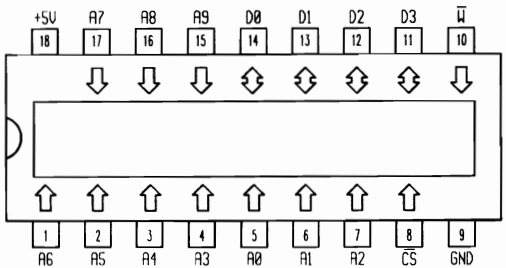
2147 — 4096x1-Bit static RAM



$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

2147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1203 A-25M	Inm	18-FLAT	CMOS	-55...+125	<440	<82,5	<25		TTL-TS
IMS 1203 A-35M	Inm	18-FLAT	CMOS	-55...+125	<440	<82,5	<35		TTL-TS
IMS 1203 A-45M	Inm	18-FLAT	CMOS	-55...+125	<440	<82,5	<45		TTL-TS

2148 — 1024x4-Bit static RAM



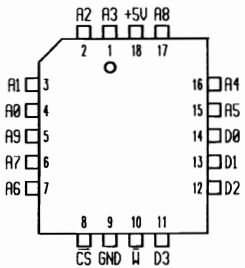
$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

2148 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6148	Hit	18-DIC	CMOS	0...+70	200	0,1	<70		TTL-TS
HM 6148-6	Hit	18-DIC	CMOS	0...+70	200	0,1	<85		TTL-TS
HM 6148 HLP-35	Hit	18-DIP	CMOS	0...+70	<440	<0,275	<35		TTL-TS
HM 6148 HLP-45	Hit	18-DIP	CMOS	0...+70	<440	<0,275	<45		TTL-TS
HM 6148 HLP-55	Hit	18-DIP	CMOS	0...+70	<440	<0,275	<55		TTL-TS
HM 6148 HP-35	Hit	18-DIP	CMOS	0...+70	<440	<4,4	<35		TTL-TS
HM 6148 HP-45	Hit	18-DIP	CMOS	0...+70	<440	<4,4	<45		TTL-TS
HM 6148 HP-55	Hit	18-DIP	CMOS	0...+70	<440	<4,4	<55		TTL-TS

2148 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6148 LP	Hit	18-DIP	CMOS	0...+70	200	5µ	<70		TTL-TS
HM 6148 LP-6	Hit	18-DIP	CMOS	0...+70	200	5µ	<85		TTL-TS
HM 6148 P	Hit	18-DIP	CMOS	0...+70	200	0,1	<70		TTL-TS
HM 6148 P-6	Hit	18-DIP	CMOS	0...+70	200	0,1	<85		TTL-TS
IM 2148	Isi	18-DIP	NMOS	0...+70	<770		<70		TTL-TS
IM 2148-3	Isi	18-DIP	NMOS	0...+70	<770		<55		TTL-TS
IMS 1223 P-25	Inm	18-DIP	CMOS	0...+70	<550	<82,5	<25		TTL-TS
IMS 1223 P-35	Inm	18-DIP	CMOS	0...+70	<550	<82,5	<35		TTL-TS
IMS 1223 P-45	Inm	18-DIP	CMOS	0...+70	<550	<82,5	<45		TTL-TS
IMS 1223 S-25	Inm	18-DIC	CMOS	0...+70	<550	<82,5	<25		TTL-TS
IMS 1223 S-25M	Inm	18-DIC	CMOS	-55...+125	<550	<82,5	<25		TTL-TS
IMS 1223 S-35	Inm	18-DIC	CMOS	0...+70	<550	<82,5	<35		TTL-TS
IMS 1223 S-35M	Inm	18-DIC	CMOS	-55...+125	<550	<82,5	<35		TTL-TS
IMS 1223 S-45	Inm	18-DIC	CMOS	0...+70	<550	<82,5	<45		TTL-TS
IMS 1223 S-45M	Inm	18-DIC	CMOS	-55...+125	<550	<82,5	<45		TTL-TS
MB 8148-55	Fui	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
MB 8148-70	Fui	18-DIP	NMOS	0...+70	<990		<70		TTL-TS
MB 8148 L-55	Fui	18-DIP	NMOS	0...+70	<687		<55		TTL-TS
MB 8148 L-70	Fui	18-DIP	NMOS	0...+70	<687		<70		TTL-TS
MB 8149-45	Fui	18-DIP	NMOS	0...+70	<990		<45		TTL-TS
MB 8149-55	Fui	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
MB 8149-70	Fui	18-DIP	NMOS	0...+70	<990		<70		TTL-TS
MB 8149 L-55	Fui	18-DIP	NMOS	0...+70	<687		<55		TTL-TS
MB 8149 L-70	Fui	18-DIP	NMOS	0...+70	<687		<70		TTL-TS
MCM 2148 C-70	Mot	18-DIC	NMOS	0...+70	<742	<165	<70		TTL-TS
MCM 2148 C-85	Mot	18-DIC	NMOS	0...+70	<742	<165	<85		TTL-TS
MCM 2148 L-70	Mot	18-DIC	NMOS	0...+70	<742	<165	<70		TTL-TS
MCM 2148 L-85	Mot	18-DIC	NMOS	0...+70	<742	<165	<85		TTL-TS
MCM 2149 C-70	Mot	18-DIC	NMOS	0...+70	<742	<165	<70		TTL-TS
MCM 2149 C-85	Mot	18-DIC	NMOS	0...+70	<742	<165	<85		TTL-TS
MCM 2149 L-70	Mot	18-DIC	NMOS	0...+70	<742	<165	<70		TTL-TS
MCM 2149 L-85	Mot	18-DIC	NMOS	0...+70	<742	<165	<85		TTL-TS
MCM 65148 C-70	Mot	18-DIC	CMOS	0...+70	200	0,1	<70		TTL-TS
MCM 65148 C-85	Mot	18-DIC	CMOS	0...+70	200	0,1	<85		TTL-TS
MCM 65148 L-70	Mot	18-DIC	CMOS	0...+70	200	0,1	<70		TTL-TS
MCM 65148 L-85	Mot	18-DIC	CMOS	0...+70	200	0,1	<85		TTL-TS
MK 2148 J-55	Mos	18-DIC	NMOS	0...+70	<687	<165	<55		TTL-TS

2148 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 2148 J-70	Mos	18-DIC	NMOS	0...+70	<687	<165	<70		TTL-TS
MK 2148 J-85	Mos	18-DIC	NMOS	0...+70	<687	<165	<85		TTL-TS
MN 2148 H-5	Mat	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
NMC 2148 HJ	Nsc	18-DIC	NMOS	0...+70	<990	<165	<70		TTL-TS
NMC 2148 HJ-2	Nsc	18-DIC	NMOS	0...+70	<990	<165	<45		TTL-TS
NMC 2148 HJ-3	Nsc	18-DIC	NMOS	0...+70	<990	<165	<55		TTL-TS
NMC 2148 HJ-3L	Nsc	18-DIC	NMOS	0...+70	<688	<110	<55		TTL-TS
NMC 2148 HJ-L	Nsc	18-DIC	NMOS	0...+70	<688	<110	<70		TTL-TS
NMC 2148 HN	Nsc	18-DIP	NMOS	0...+70	<990	<165	<70		TTL-TS
NMC 2148 HN-2	Nsc	18-DIP	NMOS	0...+70	<990	<165	<45		TTL-TS
NMC 2148 HN-3	Nsc	18-DIP	NMOS	0...+70	<990	<165	<55		TTL-TS
NMC 2148 HN-3L	Nsc	18-DIP	NMOS	0...+70	<688	<110	<55		TTL-TS
NMC 2148 HN-L	Nsc	18-DIP	NMOS	0...+70	<688	<110	<70		TTL-TS
TMS 2149-3 JL	Tix	18-DIC	NMOS	0...+70	<660		<35		TTL-TS
TMS 2149-3 NL	Tix	18-DIP	NMOS	0...+70	<660		<35		TTL-TS
TMS 2149-4 JL	Tix	18-DIC	NMOS	0...+70	<660		<45		TTL-TS
TMS 2149-4 NL	Tix	18-DIP	NMOS	0...+70	<660		<45		TTL-TS
TMS 2149-5 JL	Tix	18-DIC	NMOS	0...+70	<660		<55		TTL-TS
TMS 2149-5 NL	Tix	18-DIP	NMOS	0...+70	<660		<55		TTL-TS
TMS 2149-7 JL	Tix	18-DIC	NMOS	0...+70	<660		<70		TTL-TS
TMS 2149-7 NL	Tix	18-DIP	NMOS	0...+70	<660		<70		TTL-TS
2148 H	Int	18-DIP	NMOS	0...+70	<990		<70		TTL-TS
2148 H-2	Int	18-DIP	NMOS	0...+70	<660		<45		TTL-TS
2148 H-3	Int	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
2148 HL	Int	18-DIP	NMOS	0...+70	<687		<70		TTL-TS
2148 HL-3	Int	18-DIP	NMOS	0...+70	<687		<55		TTL-TS
2149 H	Int	18-DIP	NMOS	0...+70	<990		<70		TTL-TS
2149 H-2	Int	18-DIP	NMOS	0...+70	<990		<45		TTL-TS
2149 H-3	Int	18-DIP	NMOS	0...+70	<990		<55		TTL-TS
2149 HL	Int	18-DIP	NMOS	0...+70	<687		<70		TTL-TS
2149 HL-3	Int	18-DIP	NMOS	0...+70	<687		<55		TTL-TS
µPD 2149 D	Nip	18-DIC	NMOS	0...+70	<990	<110	<55		TTL-TS
µPD 2149 D-1	Nip	18-DIC	NMOS	0...+70	<990	<110	<45		TTL-TS
µPD 2149 D-2	Nip	18-DIC	NMOS	0...+70	<990	<110	<35		TTL-TS

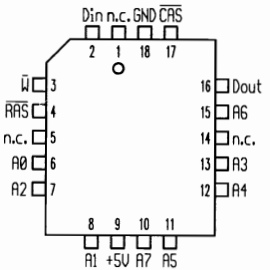
2148 — 1024x4-Bit static RAM



$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

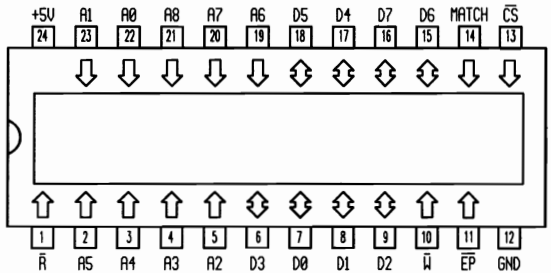
2148 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 2149-3 FPL	Tix	18-PLCC	NMOS	0...+70	<660		<35		TTL-TS
TMS 2149-4 FPL	Tix	18-PLCC	NMOS	0...+70	<660		<45		TTL-TS
TMS 2149-5 FPL	Tix	18-PLCC	NMOS	0...+70	<660		<55		TTL-TS
TMS 2149-7 FPL	Tix	18-PLCC	NMOS	0...+70	<660		<70		TTL-TS

2148 — 1024x4-Bit static RAM



CS	W	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

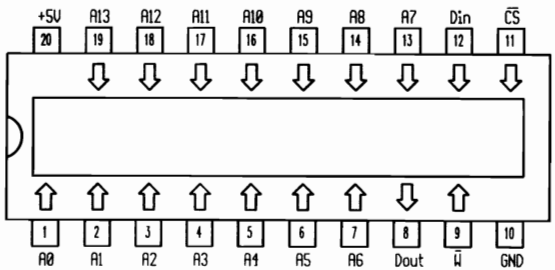
2150 — 512x8-Bit Cache Address Comparator



2148 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1223 A-25M	Inm	18-FLAT	CMOS	-55...+125	<550	<82,5	<25		TTL-TS
IMS 1223 A-35M	Inm	18-FLAT	CMOS	-55...+125	<550	<82,5	<35		TTL-TS
IMS 1223 A-45M	Inm	18-FLAT	CMOS	-55...+125	<550	<82,5	<45		TTL-TS

2150 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TACT 2150-20 DW	Tix	24-FLAT	CMOS	0...+70	<523		<20		MATCH
TACT 2150-20 JD	Tix	24-DIC	CMOS	0...+70	<523		<20		MATCH
TACT 2150-20 NT	Tix	24-TDIP	CMOS	0...+70	<523		<20		MATCH
TACT 2150-30 DW	Tix	24-FLAT	CMOS	0...+70	<523		<30		MATCH
TACT 2150-30 JD	Tix	24-DIC	CMOS	0...+70	<523		<30		MATCH
TACT 2150-30 NT	Tix	24-TDIP	CMOS	0...+70	<523		<30		MATCH

2167 — 16384x1-Bit static RAM

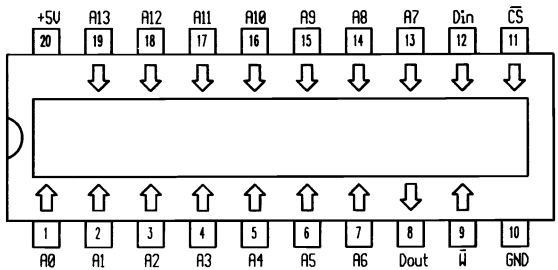


$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

2167 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6167	Hit	20-DIC	CMOS	0...+70	<330	<110	<70		TTL-TS
HM 6167-6	Hit	20-DIC	CMOS	0...+70	<330	<110	<85		TTL-TS
HM 6167-8	Hit	20-DIC	CMOS	0...+70	<330	<110	<100		TTL-TS
HM 6167 H-45	Hit	20-DIC	CMOS	0...+70	<440	<11	<45		TTL-TS
HM 6167 H-55	Hit	20-DIC	CMOS	0...+70	<440	<11	<55		TTL-TS
HM 6167 HLP-45	Hit	20-DIP	CMOS	0...+70	<440	<55µ	<45		TTL-TS
HM 6167 HLP-55	Hit	20-DIP	CMOS	0...+70	<440	<55µ	<55		TTL-TS
HM 6167 HLP-70	Hit	20-DIP	CMOS	0...+70	<440	<55µ	<70		TTL-TS

2167 Type	Man	Case	Techn	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6167 HP-45	Hit	20-DIP	CMOS	0...+70	<440	<11	<45		TTL-TS
HM 6167 HP-55	Hit	20-DIP	CMOS	0...+70	<440	<11	<55		TTL-TS
HM 6167 HP-70	Hit	20-DIP	CMOS	0...+70	<330	<11	<70		TTL-TS
HM 6167 LP	Hit	20-DIP	CMOS	0...+70	<330	<0,275	<70		TTL-TS
HM 6167 LP-6	Hit	20-DIP	CMOS	0...+70	<330	<0,275	<85		TTL-TS
HM 6167 LP-8	Hit	20-DIP	CMOS	0...+70	<330	<0,275	<100		TTL-TS
HM 6167 P	Hit	20-DIP	CMOS	0...+70	150	25	<70		TTL-TS
HM 6167 P-6	Hit	20-DIP	CMOS	0...+70	150	25	<85		TTL-TS
HM 6167 P-8	Hit	20-DIP	CMOS	0...+70	150	25	<100		TTL-TS
HM 6267 LP-35	Hit	20-DIP	CMOS	0...+70	<550	<0,275	<35		TTL-TS
HM 6267 LP-45	Hit	20-DIP	CMOS	0...+70	<440	<0,275	<45		TTL-TS
HM 6267 P-35	Hit	20-DIP	CMOS	0...+70	<550	<11	<35		TTL-TS
HM 6267 P-45	Hit	20-DIP	CMOS	0...+70	<440	<11	<45		TTL-TS
MK 41H66 N-20	Tho	20-DIP	CMOS	0...+70	<550		<20		TTL-TS
MK 41H66 N-25	Tho	20-DIP	CMOS	0...+70	<550		<25		TTL-TS
MK 41H66 N-35	Tho	20-DIP	CMOS	0...+70	<550		<35		TTL-TS
MK 41H66 P-20	Tho	20-DIC	CMOS	0...+70	<550		<20		TTL-TS
MK 41H66 P-25	Tho	20-DIC	CMOS	0...+70	<550		<25		TTL-TS
MK 41H66 P-35	Tho	20-DIC	CMOS	0...+70	<550		<35		TTL-TS

2167 — 16384x1-Bit static RAM



$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

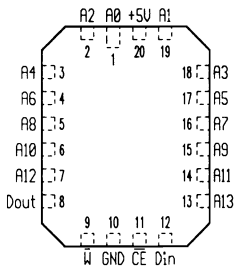
2167 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2167-45	Amd	20-DIP	NMOS	0...+70	<660		<45		TTL-TS
Am 2167-55	Amd	20-DIP	NMOS	0...+70	<660		<55		TTL-TS
Am 2167-70	Amd	20-DIP	NMOS	0...+70	<660		<70		TTL-TS
F 3567-55	Fch	20-DIP	NMOS	0...+70	625		<55		TTL-TS
HM1 65262 -2	Mhs	20-DIC	CMOS	-55...+125	<275	<27,5	<85		TTL-TS
HM1 65262 -5	Mhs	20-DIC	CMOS	0...+70	<275	<11	<70		TTL-TS
HM1 65262 -9	Mhs	20-DIC	CMOS	-40...+85	<275	<16,5	<85		TTL-TS
HM1 65262 B-2	Mhs	20-DIC	CMOS	-55...+125	<275	<27,5	<70		TTL-TS

2167 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65262 B-5	Mhs	20-DIC	CMOS	0...+70	<275	<11	<55		TTL-TS
HM1 65262 B-9	Mhs	20-DIC	CMOS	-40...+85	<275	<16,5	<70		TTL-TS
HM1 65262 C-2	Mhs	20-DIC	CMOS	-55...+125	<275	<27,5	<85		TTL-TS
HM1 65262 C-5	Mhs	20-DIC	CMOS	0...+70	<275	<11	<70		TTL-TS
HM1 65262 C-9	Mhs	20-DIC	CMOS	-40...+85	<275	<16,5	<85		TTL-TS
HM1 65767 E-5	Mhs	20-DIC	CMOS	0...+70	<385	<55	<15		TTL-TS
HM1 65767 F-5	Mhs	20-DIC	CMOS	0...+70	<385	<55	<20		TTL-TS
HM1 65767 H-2	Mhs	20-DIC	CMOS	-55...+125	<440	<110	<25		TTL-TS
HM1 65767 H-5	Mhs	20-DIC	CMOS	0...+70	<385	<110	<25		TTL-TS
HM1 65767 K-2	Mhs	20-DIC	CMOS	-55...+125	<385	<110	<35		TTL-TS
HM1 65767 K-5	Mhs	20-DIC	CMOS	0...+70	<385	<110	<35		TTL-TS
HM1 65767 M-2	Mhs	20-DIC	CMOS	-55...+125	<275	<110	<45		TTL-TS
HM1 65767 M-5	Mhs	20-DIC	CMOS	0...+70	<275	<82,5	<45		TTL-TS
HM1 65767 N-2	Mhs	20-DIC	CMOS	-55...+125	<385	<110	<55		TTL-TS
HM1 65767 N-5	Mhs	20-DIC	CMOS	0...+70	<495	<165	<55		TTL-TS
HM3 65262 -2	Mhs	20-TDIP	CMOS	-55...+125	<275	<27,5	<85		TTL-TS
HM3 65262 -5	Mhs	20-TDIP	CMOS	0...+70	<275	<11	<70		TTL-TS
HM3 65262 -9	Mhs	20-TDIP	CMOS	-40...+85	<275	<16,5	<85		TTL-TS
HM3 65262 B-2	Mhs	20-TDIP	CMOS	-55...+125	<275	<27,5	<70		TTL-TS
HM3 65262 B-5	Mhs	20-TDIP	CMOS	0...+70	<275	<11	<55		TTL-TS
HM3 65262 B-9	Mhs	20-TDIP	CMOS	-40...+85	<275	<16,5	<70		TTL-TS
HM3 65262 C-2	Mhs	20-TDIP	CMOS	-55...+125	<275	<27,5	<85		TTL-TS
HM3 65262 C-5	Mhs	20-TDIP	CMOS	0...+70	<275	<11	<70		TTL-TS
HM3 65262 C-9	Mhs	20-TDIP	CMOS	-40...+85	<275	<16,5	<85		TTL-TS
HM3 65767 E-5	Mhs	20-DIP	CMOS	0...+70	<385	<55	<15		TTL-TS
HM3 65767 F-5	Mhs	20-DIP	CMOS	0...+70	<385	<55	<20		TTL-TS
HM3 65767 H-2	Mhs	20-DIP	CMOS	-55...+125	<440	<110	<25		TTL-TS
HM3 65767 H-5	Mhs	20-DIP	CMOS	0...+70	<385	<110	<25		TTL-TS
HM3 65767 K-2	Mhs	20-DIP	CMOS	-55...+125	<385	<110	<35		TTL-TS
HM3 65767 K-5	Mhs	20-DIP	CMOS	0...+70	<385	<110	<35		TTL-TS
HM3 65767 M-2	Mhs	20-DIP	CMOS	-55...+125	<275	<110	<45		TTL-TS
HM3 65767 M-5	Mhs	20-DIP	CMOS	0...+70	<275	<82,5	<45		TTL-TS
HM3 65767 N-2	Mhs	20-DIP	CMOS	-55...+125	<385	<110	<55		TTL-TS
HM3 65767 N-5	Mhs	20-DIP	CMOS	0...+70	<495	<165	<55		TTL-TS
HMT 65767 E-5	Mhs	20-FLAT	CMOS	0...+70	<385	<55	<15		TTL-TS
HMT 65767 F-5	Mhs	20-FLAT	CMOS	0...+70	<385	<55	<20		TTL-TS
HMT 65767 H-2	Mhs	20-FLAT	CMOS	-55...+125	<440	<110	<25		TTL-TS

2167 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HMT 65767 H-5	Mhs	20-FLAT	CMOS	0...+70	<385	<110	<25		TTL-TS
HMT 65767 K-2	Mhs	20-FLAT	CMOS	-55...+125	<385	<110	<35		TTL-TS
HMT 65767 K-5	Mhs	20-FLAT	CMOS	0...+70	<385	<110	<35		TTL-TS
HMT 65767 M-2	Mhs	20-FLAT	CMOS	-55...+125	<275	<110	<45		TTL-TS
HMT 65767 M-5	Mhs	20-FLAT	CMOS	0...+70	<275	<82,5	<45		TTL-TS
HMT 65767 N-2	Mhs	20-FLAT	CMOS	-55...+125	<385	<110	<55		TTL-TS
HMT 65767 N-5	Mhs	20-FLAT	CMOS	0...+70	<495	<165	<55		TTL-TS
IMS 1400 S-45M	Inm	20-DIC	CMOS	-55...+125	<660	<165	<45		TTL-TS
IMS 1400 S-55M	Inm	20-DIC	CMOS	-55...+125	<660	<165	<55		TTL-TS
IMS 1400 S-70M	Inm	20-DIC	CMOS	-55...+125	<660	<165	<70		TTL-TS
IMS 1403 LS-35M	Inm	20-DIC	CMOS	-55...+125	<412,5	<82,5	<35		TTL-TS
IMS 1403 LS-45M	Inm	20-DIC	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
IMS 1403 LS-55M	Inm	20-DIC	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
IMS 1403 P-25	Inm	20-DIP	CMOS	0...+70	<412,5	<82,5	<25		TTL-TS
IMS 1403 P-35	Inm	20-DIP	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
IMS 1403 P-45	Inm	20-DIP	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS
IMS 1403 P-55	Inm	20-DIP	CMOS	0...+70	<412,5	<82,5	<55		TTL-TS
IMS 1403 S-25	Inm	20-DIC	CMOS	0...+70	<412,5	<82,5	<25		TTL-TS
IMS 1403 S-35	Inm	20-DIC	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
IMS 1403 S-35M	Inm	20-DIC	CMOS	-55...+125	<412,5	<82,5	<35		TTL-TS
IMS 1403 S-45	Inm	20-DIC	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS
IMS 1403 S-45M	Inm	20-DIC	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
IMS 1403 S-55	Inm	20-DIC	CMOS	0...+70	<412,5	<82,5	<55		TTL-TS
IMS 1403 S-55M	Inm	20-DIC	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
M5M2167 S-55	Mit	20-DIP	NMOS	0...+70	600		<55		TTL-TS
M5M2167 S-70	Mit	20-DIP	NMOS	0...+70	600		<70		TTL-TS
M5M 21C67 P-45	Mit	20-DIP	CMOS	0...+70	<275	<110	<45		TTL-TS
M5M 21C67 P-55	Mit	20-DIP	CMOS	0...+70	<275	<110	<55		TTL-TS
MB 8167-45	Fui	20-DIP	NMOS	0...+70	<660		<45		TTL-TS
MB 8167-55	Fui	20-DIP	NMOS	0...+70	<660		<55		TTL-TS
MB 8167-70	Fui	20-DIP	NMOS	0...+70	<660		<70		TTL-TS
MCM 2167 L-55	Mot	20-DIC	NMOS				<55		TTL-TS
MCM 2167 L-70	Mot	20-DIC	NMOS				<70		TTL-TS
MCM 2167 L-85	Mot	20-DIC	NMOS				<85		TTL-TS
MCM 2167 L-100	Mot	20-DIC	NMOS				<100		TTL-TS
MK 41H67 N-20	Tho	20-DIP	CMOS	0...+70	<550	<55	<20		TTL-TS
MK 41H67 N-25	Tho	20-DIP	CMOS	0...+70	<550	<55	<25		TTL-TS

2167 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 41H67 N-35	Tho	20-DIP	CMOS	0...+70	<550	<55	<35		TTL-TS
MK 41H67 P-20	Tho	20-DIC	CMOS	0...+70	<550	<55	<20		TTL-TS
MK 41H67 P-25	Tho	20-DIC	CMOS	0...+70	<550	<55	<25		TTL-TS
MK 41H67 P-35	Tho	20-DIC	CMOS	0...+70	<550	<55	<35		TTL-TS
TMS 2167-4 JL	Tix	20-DIC	NMOS	0...+70	<660	<110	<45		TTL-TS
TMS 2167-4 NL	Tix	20-DIP	NMOS	0...+70	<660	<110	<45		TTL-TS
TMS 2167-5 JL	Tix	20-DIC	NMOS	0...+70	<660	<110	<55		TTL-TS
TMS 2167-5 NL	Tix	20-DIP	NMOS	0...+70	<660	<110	<55		TTL-TS
TMS 2167-7 JL	Tix	20-DIC	NMOS	0...+70	<660	<110	<70		TTL-TS
TMS 2167-7 NL	Tix	20-DIP	NMOS	0...+70	<660	<110	<70		TTL-TS
TS 6167 N-45	Tho	20-DIP	CMOS	0...+70	<440	<11	<45		TTL-TS
TS 6167 N-55	Tho	20-DIP	CMOS	0...+70	<440	<11	<55		TTL-TS
TS 6167 N-70	Tho	20-DIP	CMOS	0...+70	<440	<11	<70		TTL-TS
TS 6167 P-45	Tho	20-DIC	CMOS	0...+70	<440	<11	<45		TTL-TS
TS 6167 P-55	Tho	20-DIC	CMOS	0...+70	<440	<11	<55		TTL-TS
TS 6167 P-70	Tho	20-DIC	CMOS	0...+70	<440	<11	<70		TTL-TS
2167-55	Int	20-DIP	NMOS	0...+70	<385		<55		TTL-TS
2167-70	Int	20-DIP	NMOS	0...+70	<385		<70		TTL-TS
2167 L-10	Int	20-DIP	NMOS	0...+70	<275		<100		TTL-TS
2167 L-70	Int	20-DIP	NMOS	0...+70	<275		<70		TTL-TS
µPD 2167 D-2	Nip	20-DIC	NMOS	0...+70	<990	<110	<70		TTL-TS
µPD 2167 D-3	Nip	20-DIC	NMOS	0...+70	<990	<110	<55		TTL-TS

2167 — 16384x1-Bit static RAM

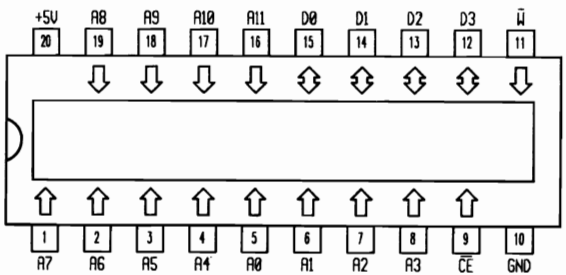


$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

2167 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6267 CG-35	Hit	20-LCC	CMOS	0...+70	<550	<11	<35		TTL-TS
HM 6267 CG-45	Hit	20-LCC	CMOS	0...+70	<440	<11	<45		TTL-TS
HM4 65262 -2	Mhs	20-LCC	CMOS	-55...+125	<275	<27,5	<85		TTL-TS
HM4 65262 -5	Mhs	20-LCC	CMOS	0...+70	<275	<11	<70		TTL-TS
HM4 65262 -9	Mhs	20-LCC	CMOS	-40...+85	<275	<16,5	<85		TTL-TS
HM4 65262 B-2	Mhs	20-LCC	CMOS	-55...+125	<275	<27,5	<70		TTL-TS
HM4 65262 B-5	Mhs	20-LCC	CMOS	0...+70	<275	<11	<55		TTL-TS
HM4 65262 B-9	Mhs	20-LCC	CMOS	-40...+85	<275	<16,5	<70		TTL-TS

2167 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65262 C-2	Mhs	20-LCC	CMOS	-55...+125	<275	<27,5	<85		TTL-TS
HM4 65262 C-5	Mhs	20-LCC	CMOS	0...+70	<275	<11	<70		TTL-TS
HM4 65262 C-9	Mhs	20-LCC	CMOS	-40...+85	<275	<16,5	<85		TTL-TS
HM4 65767 E-5	Mhs	20-LCC	CMOS	0...+70	<385	<55	<15		TTL-TS
HM4 65767 F-5	Mhs	20-LCC	CMOS	0...+70	<385	<55	<20		TTL-TS
HM4 65767 H-2	Mhs	20-LCC	CMOS	-55...+125	<440	<110	<25		TTL-TS
HM4 65767 H-5	Mhs	20-LCC	CMOS	0...+70	<385	<110	<25		TTL-TS
HM4 65767 K-2	Mhs	20-LCC	CMOS	-55...+125	<385	<110	<35		TTL-TS
HM4 65767 K-5	Mhs	20-LCC	CMOS	0...+70	<385	<110	<35		TTL-TS
HM4 65767 M-2	Mhs	20-LCC	CMOS	-55...+125	<275	<110	<45		TTL-TS
HM4 65767 M-5	Mhs	20-LCC	CMOS	0...+70	<275	<82,5	<45		TTL-TS
HM4 65767 N-2	Mhs	20-LCC	CMOS	-55...+125	<385	<110	<55		TTL-TS
HM4 65767 N-5	Mhs	20-LCC	CMOS	0...+70	<495	<165	<55		TTL-TS
IMS 1400 N-45M	Inm	20-LCC	CMOS	-55...+125	<660	<165	<45		TTL-TS
IMS 1400 N-55M	Inm	20-LCC	CMOS	-55...+125	<660	<165	<55		TTL-TS
IMS 1400 N-70M	Inm	20-LCC	CMOS	-55...+125	<660	<165	<70		TTL-TS
IMS 1403 LN-35M	Inm	20-LCC	CMOS	-55...+125	<412,5	<82,5	<35		TTL-TS
IMS 1403 LN-45M	Inm	20-LCC	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
IMS 1403 LN-55M	Inm	20-LCC	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
IMS 1403 N-35M	Inm	20-LCC	CMOS	-55...+125	<412,5	<82,5	<35		TTL-TS
IMS 1403 N-45M	Inm	20-LCC	CMOS	-55...+125	<412,5	<82,5	<45		TTL-TS
IMS 1403 N-55M	Inm	20-LCC	CMOS	-55...+125	<412,5	<82,5	<55		TTL-TS
IMS 1403 W-25	Inm	20-LCC	CMOS	0...+70	<412,5	<82,5	<25		TTL-TS
IMS 1403 W-35	Inm	20-LCC	CMOS	0...+70	<412,5	<82,5	<35		TTL-TS
IMS 1403 W-45	Inm	20-LCC	CMOS	0...+70	<412,5	<82,5	<45		TTL-TS
IMS 1403 W-55	Inm	20-LCC	CMOS	0...+70	<412,5	<82,5	<55		TTL-TS
MK 41H66 E-20	Tho	20-LCC	CMOS	0...+70	<550		<20		TTL-TS
MK 41H66 E-25	Tho	20-LCC	CMOS	0...+70	<550		<25		TTL-TS
MK 41H66 E-35	Tho	20-LCC	CMOS	0...+70	<550		<35		TTL-TS
MK 41H67 E-20	Tho	20-LCC	CMOS	0...+70	<550	<55	<20		TTL-TS
MK 41H67 E-25	Tho	20-LCC	CMOS	0...+70	<550	<55	<25		TTL-TS
MK 41H67 E-35	Tho	20-LCC	CMOS	0...+70	<550	<55	<35		TTL-TS
TS 6167 E-45	Tho	20-LCC	CMOS	0...+70	<440	<11	<45		TTL-TS
TS 6167 E-55	Tho	20-LCC	CMOS	0...+70	<440	<11	<55		TTL-TS
TS 6167 E-70	Tho	20-LCC	CMOS	0...+70	<440	<11	<70		TTL-TS

2168 — 4096x4-Bit static RAM



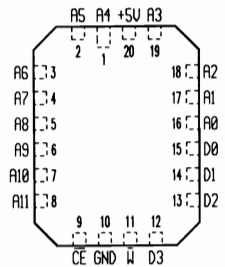
$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

2168 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1420 S-55M	Inm	20-DIC	CMOS	-55...+125	<660	<165	<55		TTL-TS
IMS 1420 S-70M	Inm	20-DIC	CMOS	-55...+125	<660	<165	<70		TTL-TS
IMS 1423 P-25	Inm	20-DIP	CMOS	0...+70	<577,5	<82,5	<25		TTL-TS
IMS 1423 P-35	Inm	20-DIP	CMOS	0...+70	<550	<82,5	<35		TTL-TS
IMS 1423 P-45	Inm	20-DIP	CMOS	0...+70	<550	<82,5	<45		TTL-TS
IMS 1423 P-55	Inm	20-DIP	CMOS	0...+70	<550	<82,5	<55		TTL-TS
IMS 1423 S-25	Inm	20-DIC	CMOS	0...+70	<577,5	<82,5	<25		TTL-TS
IMS 1423 S-35	Inm	20-DIC	CMOS	0...+70	<550	<82,5	<35		TTL-TS

2168 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1423 S-35M	Inm	20-DIC	CMOS	-55...+125	<715	<110	<35		TTL-TS
IMS 1423 S-45	Inm	20-DIC	CMOS	0...+70	<550	<82,5	<45		TTL-TS
IMS 1423 S-45M	Inm	20-DIC	CMOS	-55...+125	<660	<110	<45		TTL-TS
IMS 1423 S-55	Inm	20-DIC	CMOS	0...+70	<550	<82,5	<55		TTL-TS
IMS 1423 S-55M	Inm	20-DIC	CMOS	-55...+125	<605	<110	<55		TTL-TS
M5M 21C68 P-45	Mit	20-DIP	CMOS	0...+70	<275	<110	<45		TTL-TS
M5M 21C68 P-55	Mit	20-DIP	CMOS	0...+70	<275	<110	<55		TTL-TS
MCM 1423 P-45	Mot	20-DIP	CMOS	0...+70	<440	<11	<45		TTL-TS
MCM 6168 P-45	Mot	20-DIP	CMOS	0...+70	<440	<11	<45		TTL-TS
MCM 6168 P-55	Mot	20-DIP	CMOS	0...+70	<440	<11	<55		TTL-TS
MCM 6168 P-70	Mot	20-DIP	CMOS	0...+70	<440	<11	<70		TTL-TS
MCM 6268 P-25	Mot	20-DIP	CMOS	0...+70	<660	<110	<25		TTL-TS
MCM 6268 P-35	Mot	20-DIP	CMOS	0...+70	<605	<110	<35		TTL-TS
MK 41H68 N-20	Tho	20-DIP	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H68 N-25	Tho	20-DIP	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H68 N-35	Tho	20-DIP	CMOS	0...+70	<550	<44	<35		TTL-TS
MK 41H68 P-20	Tho	20-DIC	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H68 P-25	Tho	20-DIC	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H68 P-35	Tho	20-DIC	CMOS	0...+70	<550	<44	<35		TTL-TS
MKB 41H68 P-825	Tho	20-DIP	CMOS	-55...+125	<550	<33	<25		TTL-TS
MKB 41H68 P-835	Tho	20-DIP	CMOS	-55...+125	<550	<33	<35		TTL-TS
MKB 41H68 P-845	Tho	20-DIP	CMOS	-55...+125	<550	<33	<45		TTL-TS
TMS 2168-4 JL	Tix	20-DIC	NMOS	0...+70			<45		TTL-TS
TMS 2168-4 NL	Tix	20-DIP	NMOS	0...+70			<45		TTL-TS
TMS 2168-5 JL	Tix	20-DIC	NMOS	0...+70			<55		TTL-TS
TMS 2168-5 NL	Tix	20-DIP	NMOS	0...+70			<55		TTL-TS
TMS 2168-7 JL	Tix	20-DIC	NMOS	0...+70			<70		TTL-TS
TMS 2168-7 NL	Tix	20-DIP	NMOS	0...+70			<70		TTL-TS
TS 6168 N-45	Tho	20-DIP	CMOS	0...+70	<495	<11	<45		TTL-TS
TS 6168 N-55	Tho	20-DIP	CMOS	0...+70	<495	<11	<55		TTL-TS
TS 6168 N-70	Tho	20-DIP	CMOS	0...+70	<495	<11	<70		TTL-TS
TS 6168 P-45	Tho	20-DIC	CMOS	0...+70	<495	<11	<45		TTL-TS
TS 6168 P-55	Tho	20-DIC	CMOS	0...+70	<495	<11	<55		TTL-TS
TS 6168 P-70	Tho	20-DIC	CMOS	0...+70	<495	<11	<70		TTL-TS
6168-55 BRAJC	Mot	20-DIC	CMOS	-55...+125	<495	<110	<55		TTL-TS
6168-55 BYAJC	Mot	20-FLAT	CMOS	-55...+125	<495	<110	<55		TTL-TS
6168-70 BRAJC	Mot	20-DIC	CMOS	-55...+125	<495	<110	<70		TTL-TS

2168 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
6168-70 BYAJC	Mot	20-FLAT	CMOS	-55...+125	<495	<110	<70		TTL-TS
6268-35 BRAJC	Mot	20-DIC	CMOS	-55...+125	<660	<27,5	<35		TTL-TS
6268-35 BYAJC	Mot	20-FLAT	CMOS	-55...+125	<660	<27,5	<35		TTL-TS
6268-45 BRAJC	Mot	20-DIC	CMOS	-55...+125	<660	<27,5	<45		TTL-TS
6268-45 BYAJC	Mot	20-FLAT	CMOS	-55...+125	<660	<27,5	<45		TTL-TS

2168 — 4096x4-Bit static RAM

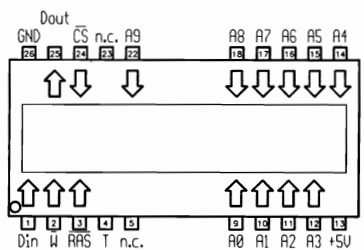


$\overline{CE}$	$\overline{W}$	D_{out}	Power	Mode
H	X	Hi-Z	standby	not selected
L	L	Hi-Z	active	write
L	H	data out	active	read

2168 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1420 N-55M	Inm	20-LCC	CMOS	-55...+125	<660	<165	<55		TTL-TS
IMS 1420 N-70M	Inm	20-LCC	CMOS	-55...+125	<660	<165	<70		TTL-TS
IMS 1423 N-35M	Inm	20-LCC	CMOS	-55...+125	<715	<110	<35		TTL-TS
IMS 1423 N-45M	Inm	20-LCC	CMOS	-55...+125	<660	<110	<45		TTL-TS
IMS 1423 N-55M	Inm	20-LCC	CMOS	-55...+125	<605	<110	<55		TTL-TS
IMS 1423 W-25	Inm	20-LCC	CMOS	0...+70	<577,5	<82,5	<25		TTL-TS
IMS 1423 W-35	Inm	20-LCC	CMOS	0...+70	<550	<82,5	<35		TTL-TS
IMS 1423 W-45	Inm	20-LCC	CMOS	0...+70	<550	<82,5	<45		TTL-TS

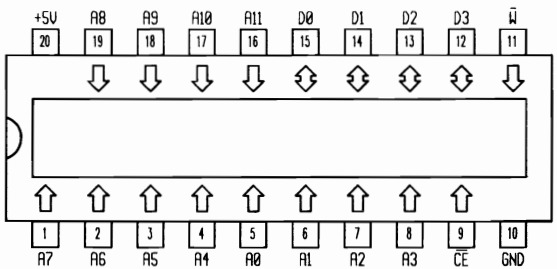
2168 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1423 W-55	Inm	20-LCC	CMOS	0...+70	<550	<82,5	<55		TTL-TS
MK 41H68 E-20	Tho	20-LCC	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H68 E-25	Tho	20-LCC	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H68 E-35	Tho	20-LCC	CMOS	0...+70	<550	<44	<35		TTL-TS
MKB 41H68 E-825	Tho	20-LCC	CMOS	-55...+125	<550	<33	<25		TTL-TS
MKB 41H68 E-835	Tho	20-LCC	CMOS	-55...+125	<550	<33	<35		TTL-TS
MKB 41H68 E-845	Tho	20-LCC	CMOS	-55...+125	<550	<33	<45		TTL-TS
TS 6168 E-45	Tho	20-LCC	CMOS	0...+70	<495	<11	<45		TTL-TS
TS 6168 E-55	Tho	20-LCC	CMOS	0...+70	<495	<11	<55		TTL-TS
TS 6168 E-70	Tho	20-LCC	CMOS	0...+70	<495	<11	<70		TTL-TS
6168-55 BUAJC	Mot	20-LCC	CMOS	-55...+125	<495	<110	<55		TTL-TS
6168-70 BUAJC	Mot	20-LCC	CMOS	-55...+125	<495	<110	<70		TTL-TS
6268-35 BUAJC	Mot	20-LCC	CMOS	-55...+125	<660	<27,5	<35		TTL-TS
6268-45 BUAJC	Mot	20-LCC	CMOS	-55...+125	<660	<27,5	<45		TTL-TS

2168 — 4096x4-Bit static RAM

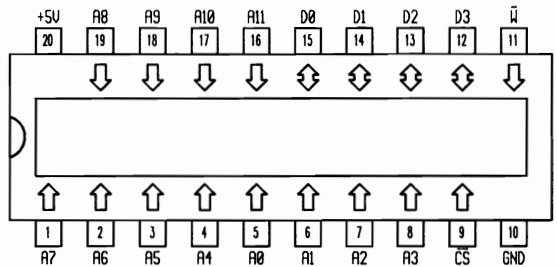


2168 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1423 E-25	Inm	20-FLAT	CMOS	0...+70	<577,5	<82,5	<25		TTL-TS
IMS 1423 E-35	Inm	20-FLAT	CMOS	0...+70	<550	<82,5	<35		TTL-TS
IMS 1423 E-45	Inm	20-FLAT	CMOS	0...+70	<550	<82,5	<45		TTL-TS
IMS 1423 E-55	Inm	20-FLAT	CMOS	0...+70	<550	<82,5	<55		TTL-TS

2168 — 4096x4-Bit static RAM



2169 — 4096x4-Bit static RAM



$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

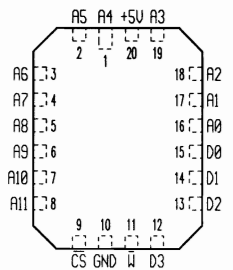
2168 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1423 Y-35M	Inm	20-FLAT	CMOS	-55...+125	<715	<110	<35		TTL-TS
IMS 1423 Y-45M	Inm	20-FLAT	CMOS	-55...+125	<660	<110	<45		TTL-TS
IMS 1423 Y-55M	Inm	20-FLAT	CMOS	-55...+125	<605	<110	<55		TTL-TS

2169 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6168 HLP-45	Hit	20-DIP	CMOS	0...+70	<495	<0,275	<45		TTL-TS
HM 6168 HLP-55	Hit	20-DIP	CMOS	0...+70	<495	<0,275	<55		TTL-TS
HM 6168 HLP-70	Hit	20-DIP	CMOS	0...+70	<495	<0,275	<70		TTL-TS
HM 6168 HP-45	Hit	20-DIP	CMOS	0...+70	<495	<11	<45		TTL-TS
HM 6168 HP-55	Hit	20-DIP	CMOS	0...+70	<495	<11	<55		TTL-TS
HM 6168 HP-70	Hit	20-DIP	CMOS	0...+70	<495	<11	<70		TTL-TS
HM 6268 LP-25	Hit	20-DIP	CMOS	0...+70	<495	<0,275	<25		TTL-TS
HM 6268 LP-35	Hit	20-DIP	CMOS	0...+70	<495	<0,275	<35		TTL-TS

2169 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6268 P-25	Hit	20-DIP	CMOS	0...+70	<495	<5,5	<25		TTL-TS
HM 6268 P-35	Hit	20-DIP	CMOS	0...+70	<495	<5,5	<35		TTL-TS
HM1 65768 E-5	Mhs	20-DIC	CMOS	0...+70	<385	<27,5	<15		TTL-TS
HM1 65768 F-5	Mhs	20-DIC	CMOS	0...+70	<385	<27,5	<20		TTL-TS
HM1 65768 H-2	Mhs	20-DIC	CMOS	-55...+125	<660	<82,5	<25		TTL-TS
HM1 65768 H-5	Mhs	20-DIC	CMOS	0...+70	<385	<82,5	<25		TTL-TS
HM1 65768 K-2	Mhs	20-DIC	CMOS	-55...+125	<495	<110	<35		TTL-TS
HM1 65768 K-5	Mhs	20-DIC	CMOS	0...+70	<385	<82,5	<35		TTL-TS
HM1 65768 M-2	Mhs	20-DIC	CMOS	-55...+125	<385	<110	<40		TTL-TS
HM1 65768 M-5	Mhs	20-DIC	CMOS	0...+70	<385	<82,5	<40		TTL-TS
HM1 65768 N-2	Mhs	20-DIC	CMOS	-55...+125	<495	<110	<40		TTL-TS
HM1 65768 N-5	Mhs	20-DIC	CMOS	0...+70	<495	<165	<40		TTL-TS
HM3 65768 E-5	Mhs	20-DIP	CMOS	0...+70	<385	<27,5	<15		TTL-TS
HM3 65768 F-5	Mhs	20-DIP	CMOS	0...+70	<385	<27,5	<20		TTL-TS
HM3 65768 H-2	Mhs	20-DIP	CMOS	-55...+125	<660	<82,5	<25		TTL-TS
HM3 65768 H-5	Mhs	20-DIP	CMOS	0...+70	<385	<82,5	<25		TTL-TS
HM3 65768 K-2	Mhs	20-DIP	CMOS	-55...+125	<495	<110	<35		TTL-TS
HM3 65768 K-5	Mhs	20-DIP	CMOS	0...+70	<385	<82,5	<35		TTL-TS
HM3 65768 M-2	Mhs	20-DIP	CMOS	-55...+125	<385	<110	<40		TTL-TS
HM3 65768 M-5	Mhs	20-DIP	CMOS	0...+70	<385	<82,5	<40		TTL-TS
HM3 65768 N-2	Mhs	20-DIP	CMOS	-55...+125	<495	<110	<40		TTL-TS
HM3 65768 N-5	Mhs	20-DIP	CMOS	0...+70	<495	<165	<40		TTL-TS
HMT 65768 E-5	Mhs	20-FLAT	CMOS	0...+70	<385	<27,5	<15		TTL-TS
HMT 65768 F-5	Mhs	20-FLAT	CMOS	0...+70	<385	<27,5	<20		TTL-TS
HMT 65768 H-2	Mhs	20-FLAT	CMOS	-55...+125	<660	<82,5	<25		TTL-TS
HMT 65768 H-5	Mhs	20-FLAT	CMOS	0...+70	<385	<82,5	<25		TTL-TS
HMT 65768 K-2	Mhs	20-FLAT	CMOS	-55...+125	<495	<110	<35		TTL-TS
HMT 65768 K-5	Mhs	20-FLAT	CMOS	0...+70	<385	<82,5	<35		TTL-TS
HMT 65768 M-2	Mhs	20-FLAT	CMOS	-55...+125	<385	<110	<40		TTL-TS
HMT 65768 M-5	Mhs	20-FLAT	CMOS	0...+70	<385	<82,5	<40		TTL-TS
HMT 65768 N-2	Mhs	20-FLAT	CMOS	-55...+125	<495	<110	<40		TTL-TS
HMT 65768 N-5	Mhs	20-FLAT	CMOS	0...+70	<495	<165	<40		TTL-TS
MCM 6269 P-25	Mot	20-DIP	CMOS	0...+70	<660	<110	<25		TTL-TS
MCM 6269 P-35	Mot	20-DIP	CMOS	0...+70	<605	<110	<35		TTL-TS
MK 41H69 N-20	Tho	20-DIP	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H69 N-25	Tho	20-DIP	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H69 N-35	Tho	20-DIP	CMOS	0...+70	<550	<44	<35		TTL-TS

2169 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 41H69 P-20	Tho	20-DIC	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H69 P-25	Tho	20-DIC	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H69 P-35	Tho	20-DIC	CMOS	0...+70	<550	<44	<35		TTL-TS
TMM 2068 AP-25	Tos	20-TDIP	NMOS	0...+70	<135	<20	<25		TTL-TS
TMM 2068 AP-35	Tos	20-TDIP	NMOS	0...+70	<120	<20	<35		TTL-TS
TMM 2068 AP-45	Tos	20-TDIP	NMOS	0...+70	<120	<20	<45		TTL-TS
TMS 2169-4 JL	Tix	20-DIC	NMOS	0...+70			<45		TTL-TS
TMS 2169-4 NL	Tix	20-DIP	NMOS	0...+70			<45		TTL-TS
TMS 2169-5 JL	Tix	20-DIC	NMOS	0...+70			<55		TTL-TS
TMS 2169-5 NL	Tix	20-DIP	NMOS	0...+70			<55		TTL-TS
TMS 2169-7 JL	Tix	20-DIC	NMOS	0...+70			<70		TTL-TS
TMS 2169-7 NL	Tix	20-DIP	NMOS	0...+70			<70		TTL-TS

2169 — 4096x4-Bit static RAM

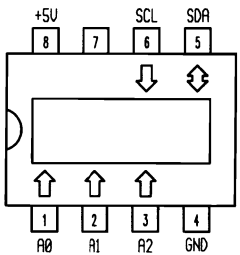


$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

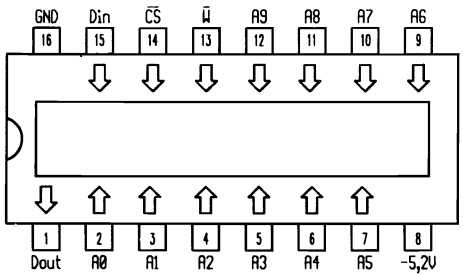
2169 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65768 E-5	Mhs	20-LCC	CMOS	0...+70	<385	<27,5	<15		TTL-TS
HM4 65768 F-5	Mhs	20-LCC	CMOS	0...+70	<385	<27,5	<20		TTL-TS
HM4 65768 H-2	Mhs	20-LCC	CMOS	-55...+125	<660	<82,5	<25		TTL-TS
HM4 65768 H-5	Mhs	20-LCC	CMOS	0...+70	<385	<82,5	<25		TTL-TS
HM4 65768 K-2	Mhs	20-LCC	CMOS	-55...+125	<495	<110	<35		TTL-TS
HM4 65768 K-5	Mhs	20-LCC	CMOS	0...+70	<385	<82,5	<35		TTL-TS
HM4 65768 M-2	Mhs	20-LCC	CMOS	-55...+125	<385	<110	<40		TTL-TS
HM4 65768 M-5	Mhs	20-LCC	CMOS	0...+70	<385	<82,5	<40		TTL-TS

2169 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65768 N-2	Mhs	20-LCC	CMOS	-55...+125	<495	<110	<40		TTL-TS
HM4 65768 N-5	Mhs	20-LCC	CMOS	0...+70	<495	<165	<40		TTL-TS
MK 41H69 E-20	Tho	20-LCC	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H69 E-25	Tho	20-LCC	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H69 E-35	Tho	20-LCC	CMOS	0...+70	<550	<44	<35		TTL-TS

2402 — 256x8-Bit serial EEPROM with IC-BUS



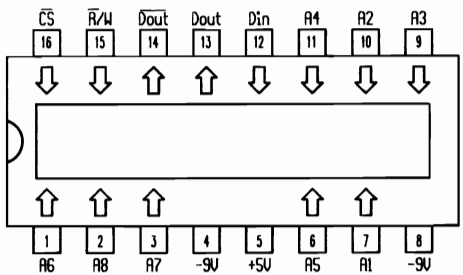
2501 — 256x1-Bit static RAM



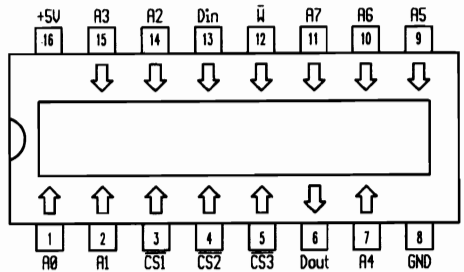
2402 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
ST 24C02 CP	Sgs	8-DIP	CMOS	0…+70	<16,5	<0,55	<3,5µ		IC-BUS
ST 24C02 VP	Sgs	8-DIP	CMOS	-40…+85	<16,5	<0,55	<3,5µ		IC-BUS

2501 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 25L01 I	Sig	16-DIC	PMOS	0…+70	$<1,7	$0,1	<1000		TTL-OC
N 25L01 N	Sig	16-DIP	PMOS	0…+70	$<1,7	$0,1	<1000		TTL-OC

2501 — 256x1-Bit static RAM



2504 — 256x1-Bit RAM (bipolar)



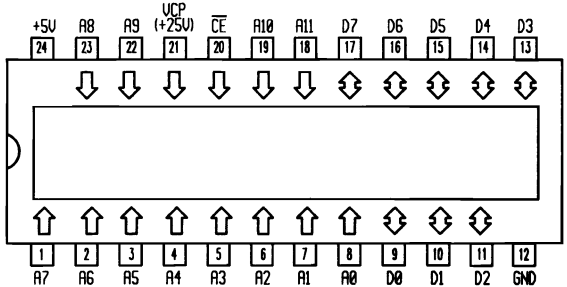
CS1...3	W	Din	Dout	Mode
one H	X	X	H	not selected
all L	L	L	H	write 0
all L	L	H	H	write 1
all L	H	X	data out*	read

* = data out inverted

2501 Type	Man	Case	Techn.	TU°C	Ptyp mW / $mW/bit	P standby mW / $mW/bit	taa ns	tref ms	Output
N 2501 I	Sig	16-DIC	PMOS	0...+70	$<1,6	$0,15	<1000		TTL-OC
N 2501 N	Sig	16-DIP	PMOS	0...+70	$<1,6	$0,15	<1000		TTL-OC

2504 Type	Man	Case	Techn.	TU°C	Ptyp mW / $mW/bit	P standby mW / $mW/bit	taa ns	tref ms	Output
HM 2504	Hit	16-DIC	TTL	0...+75	$1,8		<55		TTL-OC
HM 2504-1	Hit	16-DIC	TTL	0...+75	$1,8		<45		TTL-OC

2532 — 4096x8-Bit EPROM

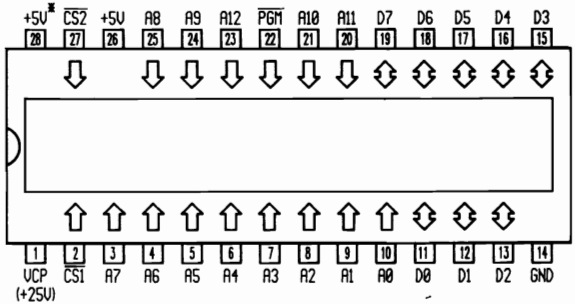


CE	VCP	D_{out}	Mode
L	+5V	data out	read
H	+5V	Hi-Z	standby
H⌐L*	+25V	data in	program
H	+25V	Hi-Z	program inhibit

* = one 50ms pulse
L = −0,1... +0,8V
H = +2..: +6V

2532 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 462532	Hit	24-DIC	NMOS	0...+70	<858	<201	<450		TTL-TS
HN 462532 G	Hit	24-DIC	NMOS	0...+70	<858	<201	<450		TTL-TS
HN 462532 G-2	Hit	24-DIC	NMOS	0...+70	<858	<201	<390		TTL-TS
HN 462532 GL	Hit	24-DIC	NMOS	0...+70	<543	<201	<450		TTL-TS
MCM 2532 C	Mot	24-DIC	NMOS	0...+70	<840		<450		TTL-TS
MCM 2532 C-25	Mot	24-DIC	NMOS	0...+70	<840		<250		TTL-TS
MCM 2532 C-35	Mot	24-DIC	NMOS	0...+70	<840		<350		TTL-TS
MCM 25L32 C	Mot	24-DIC	NMOS	0...+70	<50	<10	<450		TTL-TS
MCM 25L32 C-25	Mot	24-DIC	NMOS	0...+70	70	15	<250		TTL-TS
MCM 25L32 C-35	Mot	24-DIC	NMOS	0...+70	<50	<10	<350		TTL-TS
NMC 2532	Nsc	24-DIP	NMOS	0...+70	<840	<131	<450		TTL-TS
TMS 2532-30 JL	Tix	24-DIC	NMOS	0...+70	<840	<131	<300		TTL-TS
TMS 2532-30 JP4	Tix	24-DIC	NMOS	-10...+85	<656	<184	<300		TTL-TS
TMS 2532-35 JL	Tix	24-DIC	NMOS	0...+70	<840	<131	<350		TTL-TS
TMS 2532-35 JP4	Tix	24-DIC	NMOS	-10...+85	<656	<184	<350		TTL-TS
TMS 2532-45 JL	Tix	24-DIC	NMOS	0...+70	<840	<131	<450		TTL-TS
TMS 2532-45 JP4	Tix	24-DIC	NMOS	-10...+85	<656	<184	<450		TTL-TS
TMS 25L32-45 JL	Tix	24-DIC	NMOS	0...+70	<500	<131	<450		TTL-TS

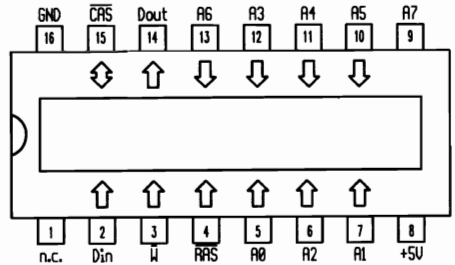
2564 — 8192x8-Bit EPROM



PD/$\overline{PGM}$	$\overline{CS1}$	$\overline{CS2}$	V_{pp}	D_n	Mode
L	L	L	+5V	data out	read
H	X	X	+5V	Hi-Z	power down
pulsed H⌐L	L	L	+25V	data in	start programming

* = Versorgung für 24-PIN ROM · Supply for 24 pin ROM
Alimentation d'une ROM à 24 broches · Alimentación per 24 pin ROM
Alimentación para una ROM de 24 pins

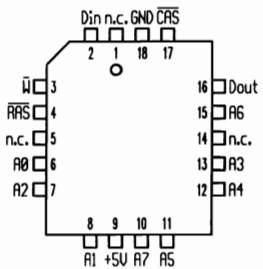
2600 — 65536x1-Bit static RAM



2564 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 2564-45 JL	Tix	28-DIC	NMOS	0...+70	<840	<157	<450		TTL-TS

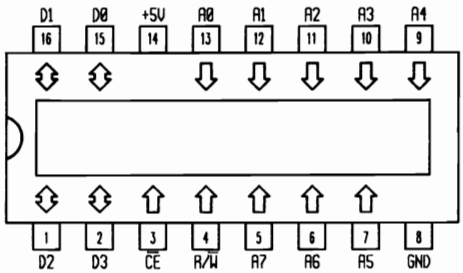
2600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 2600 S-100M	Inm	16-DIC	NMOS	-55...+110	<85	<20	<100		TTL-TS
IMS 2600 S-120M	Inm	16-DIC	NMOS	-55...+110	<85	<20	<120		TTL-TS
IMS 2600 S-150M	Inm	16-DIC	NMOS	-55...+110	<75	<20	<150		TTL-TS

2600 — 65536x1-Bit static RAM



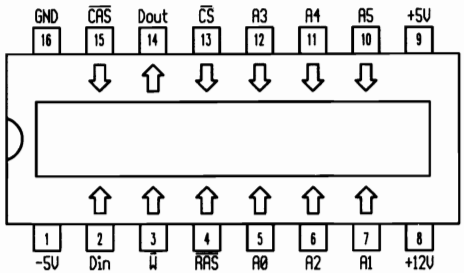
2600 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 2600 N-100M	Inm	18-LCC	NMOS	-55...+110	<85	<20	<100		TTL-TS
IMS 2600 N-120M	Inm	18-LCC	NMOS	-55...+110	<85	<20	<120		TTL-TS
IMS 2600 N-150M	Inm	18-LCC	NMOS	-55...+110	<75	<20	<150		TTL-TS

2606 — 256x4-Bit static RAM



2606 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 2606 F	Sig	16-DIC	NMOS	0...+70	<367		<750		TTL-TS
N 2606-1 F	Sig	16-DIC	NMOS	0...+70	<367		<500		TTL-TS
N 2606 I	Sig	16-DIC	NMOS	0...+70	<367		<750		TTL-TS
N 2606-1 I	Sig	16-DIC	NMOS	0...+70	<367		<500		TTL-TS
N 2606 N	Sig	16-DIP	NMOS	0...+70	<367		<750		TTL-TS
N 2606-1 N	Sig	16-DIP	NMOS	0...+70	<367		<500		TTL-TS

2660 — 4096x1-Bit dynamic RAM



RAS	CAS	CS	W	Mode
L	L	L	L	write cycle
L	L	L	H	read cycle
L	L	H	X	deselected – refresh
L	H	X	X	RAS only refresh
H	L	X	X	standby output disabled
H	H	X	X	standby output valid

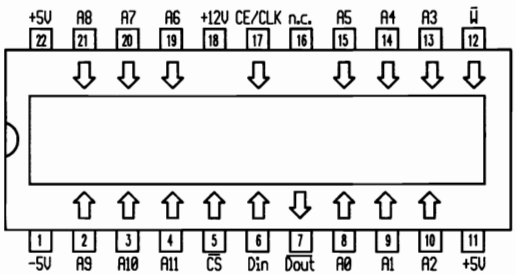
2660 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
HM 4704-2	Hit	16-DIC	NMOS	0...+70	<463	<27	<250	<2	TTL-TS
HM 4704 L-2	Hit	16-DIC	NMOS	0...+70	<464	<27	<150	<2	TTL-TS
HM 4704 L-3	Hit	16-DIC	NMOS	0...+70	<464	<27	<200	<2	TTL-TS
HM 4704 L-4	Hit	16-DIC	NMOS	0...+70	<464	<27	<250	<2	TTL-TS
HM 4704 L-6	Hit	16-DIC	NMOS	0...+70	<529	<33	<350	<1	TTL-TS
HM 4704 LP-2	Hit	16-DIP	NMOS	0...+70	<464	<27	<150	<2	TTL-TS
HM 4704 LP-3	Hit	16-DIP	NMOS	0...+70	<464	<27	<200	<2	TTL-TS
HM 4704 LP-4	Hit	16-DIP	NMOS	0...+70	<464	<27	<250	<2	TTL-TS

2660 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
HM 4704 P-2	Hit	16-DIP	NMOS	0...+70	<463	<27	<250	<2	TTL-TS
IM 7005-11 DE	Isi	16-DIC	NMOS	0...+70	<450	<27	<250	<2	TTL-TS
IM 7005-11 PE	Isi	16-DIP	NMOS	0...+70	<450	<27	<250	<2	TTL-TS
IM 7005-12 DE	Isi	16-DIC	NMOS	0...+70	<450	<27	<300	<2	TTL-TS
IM 7005-12 PE	Isi	16-DIP	NMOS	0...+70	<450	<27	<300	<2	TTL-TS
IM 7005-13 DE	Isi	16-DIC	NMOS	0...+70	<450	<27	<350	<2	TTL-TS
IM 7005-13 PE	Isi	16-DIP	NMOS	0...+70	<450	<27	<350	<2	TTL-TS
IM 7027-1	Isi	16-DIC	NMOS	0...+70	<464	<26,4	<120	<2	TTL-TS
IM 7027-2	Isi	16-DIC	NMOS	0...+70	<464	<26,4	<150	<2	TTL-TS
IM 7027-3	Isi	16-DIC	NMOS	0...+70	<464	<26,4	<200	<2	TTL-TS
IM 7027-4	Isi	16-DIC	NMOS	0...+70	<464	<26,4	<250	<2	TTL-TS
ITT 4027-2	Itt	16-DIP	NMOS	0...+70	<463	<26,4	<150	<2	TTL-TS
ITT 4027-3	Itt	16-DIP	NMOS	0...+70	<463	<26,4	<200	<2	TTL-TS
ITT 4027-4	Itt	16-DIP	NMOS	0...+70	<463	<26,4	<250	<2	TTL-TS
ITT 4027-6	Itt	16-DIP	NMOS	0...+70	<463	<26,4	<350	<2	TTL-TS
LH 4027-2	Sha	16-DIP	NMOS				<150		TTL-TS
LH 4027-3	Sha	16-DIP	NMOS				<200		TTL-TS
LH 4027-4	Sha	16-DIP	NMOS				<250		TTL-TS
M 58756 K	Mit	16-DIC	NMOS	0...+70	<740	<27	<300	<2	TTL-TS
M 58756 S	Mit	16-DIC	NMOS	0...+70	<740	<27	<300	<2	TTL-TS
MB 8224 E	Fui	16-DIP	NMOS	0...+70	<441	<19	<230	<2	TTL-TS
MB 8224 N	Fui	16-DIC	NMOS	0...+70	<441	<19	<280	<2	TTL-TS
MB 8227 E	Fui	16-DIP	NMOS	0...+70	<464	<26,4	<200	<2	TTL-TS
MB 8227 H	Fui	16-DIP	NMOS	0...+70	<464	<26,4	<150	<2	TTL-TS
MB 8227 N	Fui	16-DIP	NMOS	0...+70	<464	<26,4	<250	<2	TTL-TS
MCM 4027 AC 1	Mot	16-DIC	NMOS	0...+70	<470	<27	<120	<2	TTL-TS
MCM 4027 AC 2	Mot	16-DIC	NMOS	0...+70	<470	<27	<150	<2	TTL-TS
MCM 4027 AC 3	Mot	16-DIC	NMOS	0...+70	<470	<27	<200	<2	TTL-TS
MCM 4027 AC 4	Mot	16-DIC	NMOS	0...+70	<470	<27	<250	<2	TTL-TS
MCM 4096-11 C	Mot	16-DIP	NMOS	0...+70	<462	<20	<350	<2	TTL-TS
MCM 4096-11 L	Mot	16-DIC	NMOS	0...+70	<462	<20	<350	<2	TTL-TS
MCM 4096-16 C	Mot	16-DIP	NMOS	0...+70	<462	<20	<300	<2	TTL-TS
MCM 4096-16 L	Mot	16-DIC	NMOS	0...+70	<462	<20	<300	<2	TTL-TS
MCM 4096-6 C	Mot	16-DIP	NMOS	0...+70	<462	<20	<250	<2	TTL-TS
MCM 4096-6 L	Mot	16-DIC	NMOS	0...+70	<462	<20	<250	<2	TTL-TS
MCM 6604 L	Mot	16-DIC	NMOS	0...+70	<555	<24	<350	<2	TTL-TS
MCM 6604 L2	Mot	16-DIC	NMOS	0...+70	<555	<24	<250	<2	TTL-TS

2660 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6604 L4	Mot	16-DIC	NMOS	0...+70	<555	<24	<300	<2	TTL-TS
MCM 6604 P	Mot	16-DIP	NMOS	0...+70	<555	<24	<350	<2	TTL-TS
MCM 6604 P2	Mot	16-DIP	NMOS	0...+70	<555	<24	<250	<2	TTL-TS
MCM 6604 P4	Mot	16-DIP	NMOS	0...+70	<555	<24	<300	<2	TTL-TS
MK 4027 J-1	Mos	16-DIC	NMOS	0...+70	<462	<27	<120	<2	TTL-TS
MK 4027 J-2	Mos	16-DIC	NMOS	0...+70	<462	<27	<150	<2	TTL-TS
MK 4027 J-3	Mos	16-DIC	NMOS	0...+70	<462	<27	<200	<2	TTL-TS
MK 4027 J-4	Mos	16-DIC	NMOS	0...+70	<462	<27	<250	<2	TTL-TS
MK 4027 N-1	Mos	16-DIP	NMOS	0...+70	<462	<27	<120	<2	TTL-TS
MK 4027 N-2	Mos	16-DIP	NMOS	0...+70	<462	<27	<150	<2	TTL-TS
MK 4027 N-3	Mos	16-DIP	NMOS	0...+70	<462	<27	<200	<2	TTL-TS
MK 4027 N-4	Mos	16-DIP	NMOS	0...+70	<462	<27	<250	<2	TTL-TS
MK 4096 K-11	Mos	16-TDIC	NMOS	0...+70	<320	<19	<350	<2	TTL-TS
MK 4096 K-16	Mos	16-TDIC	NMOS	0...+70	<385	<19	<300	<2	TTL-TS
MK 4096 K-6	Mos	16-TDIC	NMOS	0...+70	<450	<19	<250	<2	TTL-TS
MK 4096 N-11	Mos	16-DIP	NMOS	0...+70	<320	<19	<350	<2	TTL-TS
MK 4096 N-16	Mos	16-DIP	NMOS	0...+70	<385	<19	<300	<2	TTL-TS
MK 4096 N-6	Mos	16-DIP	NMOS	0...+70	<450	<19	<250	<2	TTL-TS
MK 4200 K-11	Mos	16-TDIC	NMOS	0...+70	<300	<0,6	<350	<2	TTL-TS
MK 4200 K-16	Mos	16-TDIC	NMOS	0...+70	<380	<0,6	<300	<2	TTL-TS
MK 4200 N-11	Mos	16-DIP	NMOS	0...+70	<300	<0,6	<350	<2	TTL-TS
MK 4200 N-16	Mos	16-DIP	NMOS	0...+70	<380	<0,6	<300	<2	TTL-TS
MKB 4027 J-2	Mos	16-DIC	NMOS	0...+70	<462	<27	<150	<2	TTL-TS
MKB 4027 J-3	Mos	16-DIC	NMOS	0...+70	<462	<27	<200	<2	TTL-TS
MKB 4027 J-4	Mos	16-DIC	NMOS	0...+70	<462	<27	<250	<2	TTL-TS
MKB 4027 J-83	Mos	16-DIC	NMOS	-55...+85	<467	<40	<200	<2	TTL-TS
MKB 4027 J-84	Mos	16-DIC	NMOS	-55...+85	<467	<40	<250	<2	TTL-TS
MW 4104 D	Rca	16-DIP	NMOS		<380		<350		TTL-TS
N 2660 F	Sig	16-DIC	NMOS	0...+70	<380	<24	<250	<2	TTL-TS
N 2660-1 F	Sig	16-DIC	NMOS	0...+70	<380	<24	<300	<2	TTL-TS
N 2660-2 F	Sig	16-DIC	NMOS	0...+70	<380	<24	<350	<2	TTL-TS
N 2660-3 F	Sig	16-DIC	NMOS	0...+70	<380	<24	<250	<2	TTL-TS
N 2660 I	Sig	16-DIC	NMOS	0...+70	<380	<24	<250	<2	TTL-TS
N 2660-1 I	Sig	16-DIC	NMOS	0...+70	<380	<24	<300	<2	TTL-TS
N 2660-2 I	Sig	16-DIC	NMOS	0...+70	<380	<24	<350	<2	TTL-TS
N 2660-3 I	Sig	16-DIC	NMOS	0...+70	<380	<24	<250	<2	TTL-TS
N 2660 N	Sig	16-DIP	NMOS	0...+70	<380	<24	<250	<2	TTL-TS

2660 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 2660-1 N	Sig	16-DIP	NMOS	0...+70	<380	<24	<300	<2	TTL-TS
N 2660-2 N	Sig	16-DIP	NMOS	0...+70	<380	<24	<350	<2	TTL-TS
N 2660-3 N	Sig	16-DIP	NMOS	0...+70	<380	<24	<250	<2	TTL-TS
N 4027-2	Sig	16-DIP	NMOS	0...+70	<463	<26,4	<150	<2	TTL-TS
N 4027-3	Sig	16-DIP	NMOS	0...+70	<463	<26,4	<200	<2	TTL-TS
N 4027-4	Sig	16-DIP	NMOS	0...+70	<463	<26,4	<250	<2	TTL-TS
TMM 415 P-3	Tos	16-DIP	NMOS	0...+70	<463	<26,4	<200	<2	TTL-TS
TMM 415 P-4	Tos	16-DIP	NMOS	0...+70	<463	<26,4	<250	<2	TTL-TS
TMS 4027-15JL	Tix	16-DIC	NMOS	0...+70	<300	<10	<150		TTL-TS
TMS 4027-15NL	Tix	16-DIP	NMOS	0...+70	<300	<10	<150		TTL-TS
TMS 4027-20JL	Tix	16-DIC	NMOS	0...+70	<300	<10	<200		TTL-TS
TMS 4027-20NL	Tix	16-DIP	NMOS	0...+70	<300	<10	<200		TTL-TS
TMS 4027-25JL	Tix	16-DIC	NMOS	0...+70	<300	<10	<250		TTL-TS
TMS 4027-25NL	Tix	16-DIP	NMOS	0...+70	<300	<10	<250		TTL-TS
2104 A-1	Int	16-DIP	NMOS	0...+70	<464	<27	<150	<2	TTL-TS
2104 A-2	Int	16-DIP	NMOS	0...+70	<464	<27	<200	<2	TTL-TS
2104 A-3	Int	16-DIP	NMOS	0...+70	<464	<27	<250	<2	TTL-TS
2104 A-4	Int	16-DIP	NMOS	0...+70	<464	<27	<300	<2	TTL-TS
µPD 414 D	Nip	16-DIC	NMOS	0...+70	<630	<38	<300	<2	TTL-TS
µPD 414 D-1	Nip	16-DIC	NMOS	0...+70	<630	<38	<250	<2	TTL-TS
µPD 414 D-E	Nip	16-DIC	NMOS	0...+70	<630	<38	<350	<2	TTL-TS

2680 — 4096x1-Bit dynamic RAM

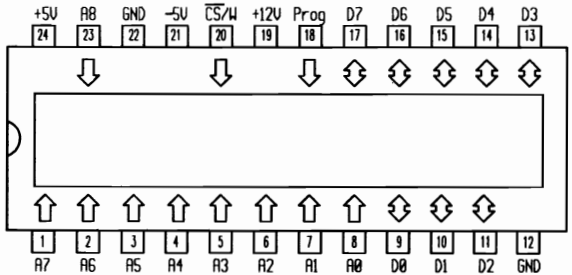


2680 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9060-CDC	Amd	22-DIC	NMOS	0...+70	<757	<2,52	<280	<2	TTL-TS
Am 9060-CPC	Amd	22-DIP	NMOS	0...+70	<757	<2,52	<280	<2	TTL-TS
Am 9060-DDC	Amd	22-DIC	NMOS	0...+70	<757	<2,52	<230	<2	TTL-TS
Am 9060-DPC	Amd	22-DIP	NMOS	0...+70	<757	<2,52	<230	<2	TTL-TS
Am 9060-EDC	Amd	22-DIC	NMOS	0...+70	<757	<2,52	<180	<2	TTL-TS
Am 9060-EPC	Amd	22-DIP	NMOS	0...+70	<757	<2,52	<180	<2	TTL-TS
HM 4710	Hit	22-DIC	NMOS	0...+70	<757	<2,52	<85	<3	TTL-TS
HM 4711-1	Hit	22-DIC	NMOS	0...+70	<757	<2,52	<110	<2	TTL-TS

2680 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 4711-2	Hit	22-DIC	NMOS	0...+70	<757	<2,52	<130	<2	TTL-TS
HM 4711-3	Hit	22-DIC	NMOS	0...+70	<757	<2,52	<180	<2	TTL-TS
IM 7280-11	Isi	22-DIC	NMOS	0...+70			<200	<2	TTL-TS
IM 7280-12	Isi	22-DIC	NMOS	0...+70			<270	<2	TTL-TS
IM 7280-14	Isi	22-DIC	NMOS	0...+70			<350	<1	TTL-TS
IM 7280-32	Isi	22-DIC	NMOS	0...+70			<270	<2	TTL-TS
M 58755 S-1	Mit	22-DIC	NMOS	0...+70	<595	<2,64	<180	<2	TTL-TS
M 58755 S-2	Mit	22-DIC	NMOS	0...+70	<595	<2,64	<250	<2	TTL-TS
M 58755 S-3	Mit	22-DIC	NMOS	0...+70	<595	<2,64	<130	<2	TTL-TS
M5L2107 BP	Mit	22-DIP	NMOS	0...+70	<529	<2,64	<180	<2	TTL-TS
M5L2107 BS	Mit	22-DIC	NMOS	0...+70	<529	<2,64	<180	<2	TTL-TS
MB 8107-E	Fui	22-DIP	NMOS	0...+70	<825	<2,52	<230	<2	TTL-TS
MB 8107-H	Fui	22-DIP	NMOS	0...+70	<825	<2,52	<180	<2	TTL-TS
MB 8107-N	Fui	22-DIP	NMOS	0...+70	<825	<2,52	<280	<2	TTL-TS
MB 8107-Y	Fui	22-DIP	NMOS	0...+70	<825	<2,52	<130	<2	TTL-TS
MM 4280 D	Nsc	22-DIC	NMOS	-55...+85	<883	<3,78	<250	<2	TTL-TS
MM 4280 J	Nsc	22-DIC	NMOS	-55...+85	<883	<3,78	<250	<2	TTL-TS
MM 5280-5 J	Nsc	22-DIC	NMOS	0...+70	<793	<3,78	<250	<2	TTL-TS
MM 5280-5 N	Nsc	22-DIP	NMOS	0...+70	<793	<3,78	<250	<2	TTL-TS
MM 5280 A-1D	Nsc	22-DIC	NMOS	0...+70	630	1,3	<90	<2	TTL-TS
MM 5280 A-1J	Nsc	22-DIC	NMOS	0...+70	630	1,3	<90	<2	TTL-TS
MM 5280 A-1N	Nsc	22-DIP	NMOS	0...+70	630	1,3	<90	<2	TTL-TS
MM 5280 A-2D	Nsc	22-DIC	NMOS	0...+70	630	1,3	<115	<2	TTL-TS
MM 5280 A-2J	Nsc	22-DIC	NMOS	0...+70	630	1,3	<115	<2	TTL-TS
MM 5280 A-2N	Nsc	22-DIP	NMOS	0...+70	630	1,3	<115	<2	TTL-TS
MM 5280 AD	Nsc	22-DIC	NMOS	0...+70	630	1,3	<140	<2	TTL-TS
MM 5280 AJ	Nsc	22-DIC	NMOS	0...+70	630	1,3	<140	<2	TTL-TS
MM 5280 AN	Nsc	22-DIP	NMOS	0...+70	630	1,3	<140	<2	TTL-TS
MM 5280 J	Nsc	22-DIC	NMOS	0...+70	<793	<3,78	<180	<2	TTL-TS
MM 5280 N	Nsc	22-DIP	NMOS	0...+70	<793	<3,78	<180	<2	TTL-TS
MN 1001	Mat	22-DIP	NMOS	0...+70	<485	<2,52	<300	<2	TTL-TS
MN 1001-1	Mat	22-DIP	NMOS	0...+70	<485	<2,52	<250	<2	TTL-TS
MN 1001-2	Mat	22-DIP	NMOS	0...+70	<485	<2,52	<200	<2	TTL-TS
MN 1002 P	Mat	22-DIP	NMOS	0...+70	<485	<2,52	<180	<2	TTL-TS
MSM 3741-1 A	Oki	22-DIP	NMOS	+10...+55	<833	<5,88	<200	<2	TTL-TS
MSM 3741-2 A	Oki	22-DIP	NMOS	+10...+55	<833	<5,88	<380	<2	TTL-TS
MSM 3741 A	Oki	22-DIP	NMOS	+10...+55	<833	<5,88	<300	<2	TTL-TS

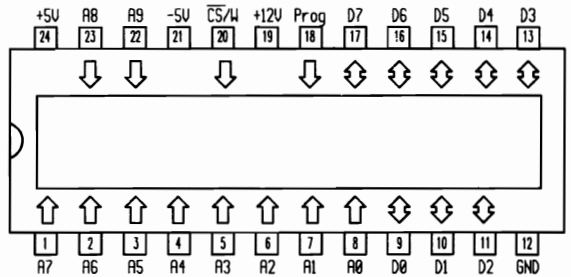
2680 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MSM 3743	Oki	22-DIP	NMOS	0...+70	<807	<2,52	<180	<2	TTL-TS
MW 4060 D	Rca	22-DIP	NMOS	0...+70			<300		TTL-TS
MW 4060 DV1	Rca	22-DIP	NMOS	0...+70			<250		TTL-TS
MW 4060 DV2	Rca	22-DIP	NMOS	0...+70			<200		TTL-TS
N 2680 F	Sig	22-DIC	NMOS	0...+70	<648		<200	<2	TTL-TS
N 2680-1 F	Sig	22-DIC	NMOS	0...+70	<648		<270	<2	TTL-TS
N 2680-2 F	Sig	22-DIC	NMOS	0...+70	<648		<350	<1	TTL-TS
N 2680 I	Sig	22-DIC	NMOS	0...+70	<648		<200	<2	TTL-TS
N 2680-1 I	Sig	22-DIC	NMOS	0...+70	<648		<270	<2	TTL-TS
N 2680-2 I	Sig	22-DIC	NMOS	0...+70	<648		<350	<1	TTL-TS
N 2680 N	Sig	22-DIP	NMOS	0...+70	<648		<200	<2	TTL-TS
N 2680-1 N	Sig	22-DIP	NMOS	0...+70	<648		<270	<2	TTL-TS
N 2680-2 N	Sig	22-DIP	NMOS	0...+70	<648		<350	<1	TTL-TS
TMS 4030-1 JL	Tix	22-DIC	NMOS	0...+70	<485	2,52	<230	<2	TTL-TS
TMS 4030-1 NL	Tix	22-DIP	NMOS	0...+70	<485	2,52	<230	<2	TTL-TS
TMS 4030-2 JL	Tix	22-DIC	NMOS	0...+70	<485	2,52	<180	<2	TTL-TS
TMS 4030-2 NL	Tix	22-DIP	NMOS	0...+70	<485	2,52	<180	<2	TTL-TS
TMS 4030 JL	Tix	22-DIC	NMOS	0...+70	<485	2,52	<280	<2	TTL-TS
TMS 4030 NL	Tix	22-DIP	NMOS	0...+70	<485	2,52	<280	<2	TTL-TS
TMS 4060-1 JL	Tix	22-DIC	NMOS	0...+70	<762	<2,52	<230	<2	TTL-TS
TMS 4060-1 PL	Tix	22-DIP	NMOS	0...+70	<762	<2,52	<230	<2	TTL-TS
TMS 4060-2 JL	Tix	22-DIC	NMOS	0...+70	<762	<2,52	<180	<2	TTL-TS
TMS 4060-2 PL	Tix	22-DIP	NMOS	0...+70	<762	<2,52	<180	<2	TTL-TS
TMS 4060-3 JL	Tix	22-DIC	NMOS	0...+70	<762	<2,52	<150	<2	TTL-TS
TMS 4060-3 PL	Tix	22-DIP	NMOS	0...+70	<762	<2,52	<150	<2	TTL-TS
TMS 4060 JL	Tix	22-DIC	NMOS	0...+70	<762	<2,52	<280	<2	TTL-TS
TMS 4060 PL	Tix	22-DIP	NMOS	0...+70	<762	<2,52	<280	<2	TTL-TS
2107 A	Int	22-DIP	NMOS	0...+70	<96	<1,26	<300	<2	TTL-TS
2107 A-1	Int	22-DIP	NMOS	0...+70	<96	<1,26	<280	<1	TTL-TS
2107 A-4	Int	22-DIP	NMOS	0...+70	<96	<1,26	<350	<2	TTL-TS
2107 A-5	Int	22-DIP	NMOS	0...+70	<96	<1,26	<420	<2	TTL-TS
2107 B	Int	22-DIP	NMOS	0...+70	<682	<2,52	<200	<2	TTL-TS
2107 B-4	Int	22-DIP	NMOS	0...+70	<682	<2,52	<270	<2	TTL-TS
2107 B-5	Int	22-DIP	NMOS	0...+70	<682	<2,52	<300	<1	TTL-TS
µPD 411 A	Nip	22-DIP	NMOS	0...+70	<630	<2,52	<300	<2	TTL-TS
µPD 411 A-1	Nip	22-DIP	NMOS	0...+70	<630	<2,52	<250	<2	TTL-TS
µPD 411 A-2	Nip	22-DIP	NMOS	0...+70	<630	<2,52	<200	<2	TTL-TS
µPD 411 A-E	Nip	22-DIP	NMOS	0...+70	<630	<2,52	<350	<1	TTL-TS
µPD 411 D	Nip	22-DIC	NMOS	0...+70	<720	0,3	<300	<2	TTL-TS
µPD 411 D-1	Nip	22-DIC	NMOS	0...+70	<720	0,3	<250	<2	TTL-TS
µPD 411 D-2	Nip	22-DIC	NMOS	0...+70	<720	0,3	<200	<2	TTL-TS
µPD 411 D-3	Nip	22-DIC	NMOS	0...+70	<780	0,3	<150	<2	TTL-TS
µPD 411 D-E	Nip	22-DIC	NMOS	0...+70	<780	0,3	<350	<1	TTL-TS

2704 — 512x8-Bit EPROM



2704 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MM 2704	Nsc	24-DIP	NMOS	0...+70	<1107		<450		TTL-TS
N 2704 I	Sig	24-DIC	NMOS	0...+70	<1107		<450		TTL-TS
TMM 321 C	Tos	24-DIP	NMOS	0...+70	<1207		<550		TTL-TS
2704	Int	24-DIP	NMOS	0...+70	<1107		<450		TTL-TS

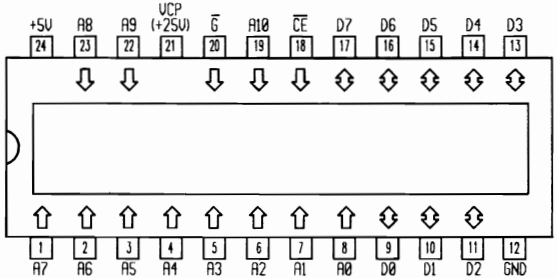
2708 — 1024x8-Bit EPROM



2708 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2708	Amd	24-DIP	NMOS	0...+70			<450		TTL-TS
F 2708	Fch	24-DIC	NMOS	0...+70	800		<450		TTL-TS
F 2708-1	Fch	24-DIC	NMOS	0...+70	800		<350		TTL-TS
HN 462708	Hit	24-DIC	NMOS	0...+70	<1087		<450		TTL-TS
IM 7708	Isi	24-DIP	NMOS	0...+70	<1108		<450		TTL-TS
M5L2708 K	Mit	24-DIC	NMOS	0...+70	<1108		<450		TTL-TS
M5L2708 K-65	Mit	24-DIC	NMOS	0...+70	<1108		<650		TTL-TS
M5L2708 S	Mit	24-DIC	NMOS	0...+70	<1108		<450		TTL-TS

2708 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5L2708 S-65	Mit	24-DIC	NMOS	0...+70	<1108		<650		TTL-TS
MCM 2708 C	Mot	24-DIC	NMOS	0...+70	<1108		<450		TTL-TS
MCM 2708 L	Mot	24-DIC	NMOS	0...+70	<1108		<450		TTL-TS
MCM 27A08 L	Mot	24-DIC	NMOS	0...+70	<1108		<300		TTL-TS
MCM 27A08 C	Mot	24-DIC	NMOS	0...+70	<1108		<300		TTL-TS
MCM 68708 C	Mot	24-DIC	NMOS	0...+70	<1055		<450		TTL-TS
MCM 68A708 C	Mot	24-DIC	NMOS	0...+70	<1055		<300		TTL-TS
MCM 68708 L	Mot	24-DIC	NMOS	0...+70	<1055		<450		TTL-TS
MCM 68A708 L	Mot	24-DIC	NMOS	0...+70	<1055		<300		TTL-TS
MM 2708	Nsc	24-DIP	NMOS	0...+70	<1108		<450		TTL-TS
MM 2708-1	Nsc	24-DIP	NMOS	0...+70	<1108		<350		TTL-TS
N 2708 I	Sig	24-DIC	NMOS	0...+70	<780		<450		TTL-TS
TMM 322 C	Tos	24-DIC	NMOS	0...+70	<1207		<550		TTL-TS
TMS 2708-35	Tix	24-DIC	NMOS	0...+70			<350		TTL-TS
TMS 2708-35 JL	Tix	24-DIC	NMOS	0...+70	<1108		<350		TTL-TS
TMS 2708-45 JL	Tix	24-DIC	NMOS	0...+70	<1108		<450		TTL-TS
TMS 27L08-45 JL	Tix	24-DIC	NMOS	0...+70	245		<450		TTL-TS
2708	Int	24-DIP	NMOS	0...+70	<1108		<450		TTL-TS
2708-1	Int	24-DIP	NMOS	0...+70	<1108		<350		TTL-TS
2708-6	Int	24-DIC	NMOS	0...+70	<1107		<550		TTL-TS
2708 L	Int	24-DIC	NMOS	0...+70	<469		<450		TTL-TS

2716 — 2048x8-Bit EPROM



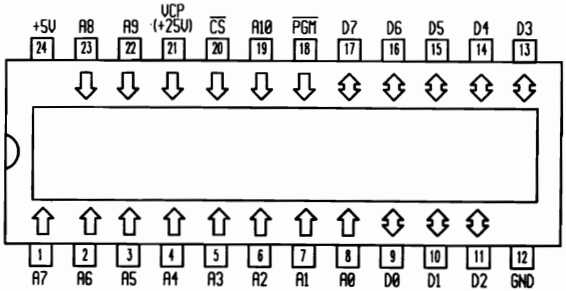
CS	G	VCP	D_n	Mode
L	L	+5V	data out	read
L⊓H*	H	+25V	data in	program
L	L	+25V	data out	program verify
H	X	+5V	Hi-Z	standby

* = 50ms pulse (active high)

2716 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
ET 2716 Q	Tho	24-DIC	NMOS	0...+70	<525	<132	<450		TTL-TS
ET 2716 Q-1	Tho	24-DIC	NMOS	0...+70	<525	<132	<350		TTL-TS
ETC 2716 Q	Tho	24-DIC	CMOS	0...+70	<55	<5,5	<450		TTL-TS
ETC 2716 Q-1	Tho	24-DIC	CMOS	0...+70	<55	<5,5	<350		TTL-TS
ETC 2716 Q-5	Tho	24-DIC	CMOS	0...+70	<55	<5,5	<550		TTL-TS
ETC 2716 QE	Tho	24-DIC	CMOS	-25...+70	<55	<5,5	<450		TTL-TS
ETC 2716 QE-1	Tho	24-DIC	CMOS	-25...+70	<55	<5,5	<350		TTL-TS
ETC 2716 QE-5	Tho	24-DIC	CMOS	-25...+70	<55	<5,5	<550		TTL-TS

2716 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
ETC 2716 QV	Tho	24-DIC	CMOS	-40...+85	<55	<5,5	<450		TTL-TS
ETC 2716 QV-1	Tho	24-DIC	CMOS	-40...+85	<55	<5,5	<350		TTL-TS
ETC 2716 QV-5	Tho	24-DIC	CMOS	-40...+85	<55	<5,5	<550		TTL-TS
HN 462716	Hit	24-DIC	NMOS	0...+70	555	213	<450		TTL-TS
HN 462716 G	Hit	24-DIC	NMOS	0...+70	555	213	<450		TTL-TS
HN 462716 G-1	Hit	24-DIC	NMOS	0...+70	555	161	<350		TTL-TS
HN 462716 G-2	Hit	24-DIC	NMOS	0...+70	555	161	<390		TTL-TS
M 2716-1 F1	Sgs	24-DIC	NMOS	0...+70	<550	<137	<350		TTL-TS
M 2716-1 F6	Sgs	24-DIC	NMOS	-40...+85	<550	<137	<350		TTL-TS
M 2716 F1	Sgs	24-DIC	NMOS	0...+70	<525	<131	<450		TTL-TS
M 2716 F6	Sgs	24-DIC	NMOS	-40...+85	<525	<131	<450		TTL-TS
M5L2716 K	Mit	24-DIC	NMOS	0...+70	<525	<131	<450		TTL-TS
M5L2716 K-65	Mit	24-DIC	NMOS	0...+70	<525	<131	<650		TTL-TS
MB 8516	Fui	24-DIP	NMOS	0...+70	<555	<213	<450		TTL-TS
MB 8516 H	Fui	24-DIP	NMOS	0...+70	<555	<213	<350		TTL-TS
MCM 2716 L	Mot	24-DIC	NMOS	0...+70	<550	<137	<450		TTL-TS
MCM 2716 L-25	Mot	24-DIC	NMOS	0...+70	<550	<137	<250		TTL-TS
MCM 2716 L-35	Mot	24-DIC	NMOS	0...+70	<550	<137	<350		TTL-TS
MCM 27L16 L	Mot	24-DIC	NMOS	0...+70	<50	<10	<450		TTL-TS
MCM 27L16 L-25	Mot	24-DIC	NMOS	0...+70	<70	<15	<250		TTL-TS
MCM 27L16 L-35	Mot	24-DIC	NMOS	0...+70	<50	<10	<350		TTL-TS
MK 2716 T-12	Mos	24-DIC	NMOS	0...+70	<525	<132	<650		TTL-TS
MK 2716 T-5	Mos	24-DIC	NMOS	0...+70	<525	<132	<300		TTL-TS
MK 2716 T-6	Mos	24-DIC	NMOS	0...+70	<525	<132	<350		TTL-TS
MK 2716 T-7	Mos	24-DIC	NMOS	0...+70	<525	<132	<390		TTL-TS
MK 2716 T-8	Mos	24-DIC	NMOS	0...+70	<525	<132	<450		TTL-TS
MKB 2716 T-12	Mos	24-DIC	NMOS	0...+70	<525	<132	<650		TTL-TS
MKB 2716 T-7	Mos	24-DIC	NMOS	0...+70	<525	<132	<390		TTL-TS
MKB 2716 T-78	Mos	24-DIC	NMOS	-40...+85	<603	<132	<450		TTL-TS
MKB 2716 T-8	Mos	24-DIC	NMOS	0...+70	<525	<132	<450		TTL-TS
MKB 2716 T-82	Mos	24-DIC	NMOS	-40...+85	<603	<132	<650		TTL-TS
MM 2716	Nsc	24-DIC	NMOS	0...+70	<525	<132	<450		TTL-TS
MM 2716-1	Nsc	24-DIC	NMOS	0...+70	<525	<132	<350		TTL-TS
MM 2716-2	Nsc	24-DIC	NMOS	0...+70	<525	<131	<390		TTL-TS
MM 2716 E	Nsc	24-DIC	NMOS	-40...+85	<525	<132	<450		TTL-TS
NMC 27C16-35	Nsc	24-DIC	CMOS	0...+70	<26,25	<0,53	<350		TTL-TS
NMC 27C16-45	Nsc	24-DIC	CMOS	0...+70	<26,25	<0,53	<450		TTL-TS
NMC 27C16E-45	Nsc	24-DIC	CMOS	-40...+85	<26,25	<0,53	<450		TTL-TS
NMC 27C16H-45	Nsc	24-DIC	CMOS	0...+70	<26,25	<0,53	<450		TTL-TS
TMM 323 D	Tos	24-DIP	NMOS	0...+70	<525	<131	<450		TTL-TS
TMM 323 D-1	Tos	24-DIP	NMOS	0...+70	<525	<131	<350		TTL-TS
TMS 2516-25 JL	Tix	24-DIC	NMOS	0...+70	<525	<131	<250		TTL-TS
TMS 2516-35 JL	Tix	24-DIC	NMOS	0...+70	<525	<131	<350		TTL-TS
TMS 2516-35 JP4	Tix	24-DIC	NMOS	-10...+85	<656	<184	<350		TTL-TS
TMS 2516-45 JL	Tix	24-DIC	NMOS	0...+70	<525	<131	<450		TTL-TS
TMS 2516-45 JP4	Tix	24-DIC	NMOS	-10...+85	<656	<184	<450		TTL-TS
2716-1	Int	24-DIP	NMOS	0...+70	<299		<350		TTL-TS
2716-2	Int	24-DIP	NMOS	0...+70	<525		<390		TTL-TS
2716-5	Int	24-DIP	NMOS	0...+70	<525		<450		TTL-TS
2716-6	Int	24-DIP	NMOS	0...+70	<525		<450		TTL-TS
µPD 2716 D	Nip	24-DIP	NMOS	-10...+80	<550	<137	<450		TTL-TS
µPD 2716 D-2	Nip	24-DIP	NMOS	-10...+80	<550	<137	<390		TTL-TS

2716 — 2048x8-Bit EEPROM

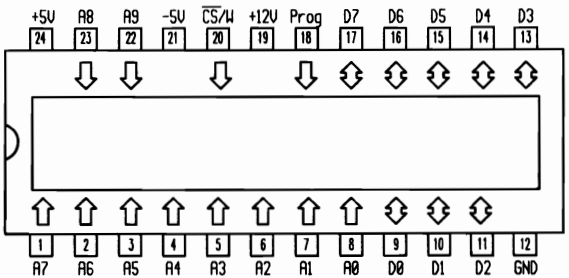


Prog	CS	VCP	D_{out}	Mode
L	L	+5V	data out	read
X	H	+5V	Hi-Z	not selected
L⎍H*	H	+25V	data in	program
L	L	+25V	data out	program verify
L	H	+25V	Hi-Z	program inhibit
L⎍H**	L	+25V	Hi-Z	erase

* = one 20ms pulse
** = one 200ms pulse
L = −0,1... +0,8V
H = +2... +6V

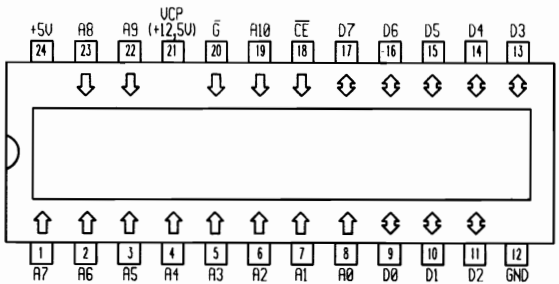
2716 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 48016 P	Hit	24-DIP	NMOS	0...+70	<300		<350		TTL-TS

2716 — 2048x8-Bit EPROM



2716 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 2716 C	Mot	24-DIC	NMOS	0...+70	<1065		<450		TTL-TS
TMS 27A16 C	Mot	24-DIC	NMOS	0...+70	<1065		<300		TTL-TS
TMS 2716 L	Mot	24-DIC	NMOS	0...+70	<1065		<300		TTL-TS
TMS 27A16 L	Mot	24-DIC	NMOS	0...+70	<1065		<300		TTL-TS

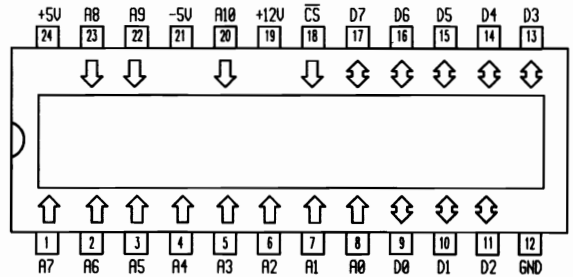
2716 — 2048x8-Bit EPROM



CE/PGM	G	V_{pp}	V_{cc}	D_{out}	Mode
L	L	+5V	+5V	data out	read
L	X	+5V	+5V	Hi-Z	standby
pulsed H⊓L	H	+13V	+6V	data in	program
H	L	+13V	+6V	data out	program verify
H	H	+13V	+6V	Hi-Z	program inhibit

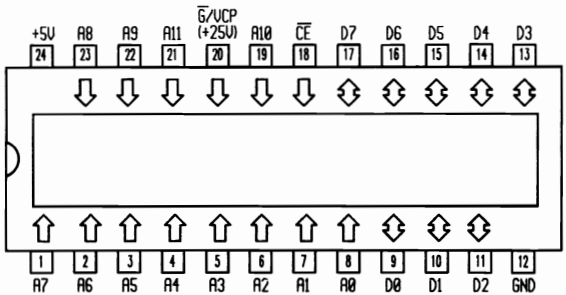
2716 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27C16 BQ35	Nsc	24-DIC	CMOS	0...+70	<26,25	<0,53	<350		TTL-TS
NMC 27C16 BQE35	Nsc	24-DIC	CMOS	-40...+85	<26,25	<0,53	<350		TTL-TS

2716 — 2048x8-Bit EPROM



2716 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 2716-30 JL	Tix	24-DIC	NMOS	0...+70	<595		<300		TTL-TS
TMS 2716-45 JL	Tix	24-DIC	NMOS	0...+70	<595		<450		TTL-TS

2732 — 4096x8-Bit EPROM



$\overline{CE}$	$\overline{G}$/VCP	D_{out}	Mode
L	L	data out	read
H	X	Hi-Z	standby
L	+25V	data in	program
L	L	data out	program verify
H	+25V	Hi-Z	program inhibit

L = −0,1... +0,8V
H = +2... +6V

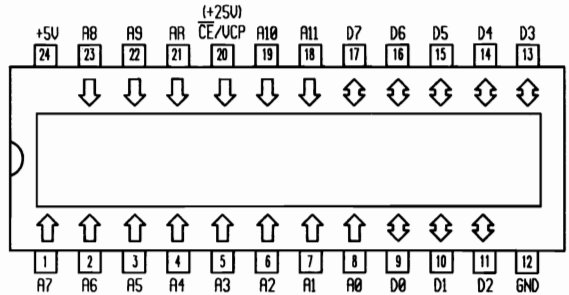
2732 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2732	Amd	24-DIP	NMOS	0...+70			<450		TTL-TS
Am 2732-1	Amd	24-DIP	NMOS	0...+70			<350		TTL-TS
Am 2732-2	Amd	24-DIP	NMOS	0...+70			<390		TTL-TS
Am 2732 A-20DC	Amd	24-DIC	NMOS	0...+70	<550	<137	<200		TTL-TS
Am 2732 A-25DC	Amd	24-DIC	NMOS	0...+70	<550	<137	<250		TTL-TS
Am 2732 A-2DC	Amd	24-DIC	NMOS	0...+70	<550	<137	<200		TTL-TS
Am 2732 A-30DC	Amd	24-DIC	NMOS	0...+70	<550	<137	<300		TTL-TS
Am 2732 A-3DC	Amd	24-DIC	NMOS	0...+70	<550	<137	<300		TTL-TS

2732 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2732 A-45DC	Amd	24-DIC	NMOS	0...+70	<550	<137	<450		TTL-TS
Am 2732 A-4DC	Amd	24-DIC	NMOS	0...+70	<550	<137	<450		TTL-TS
Am 2732 ADC	Amd	24-DIC	NMOS	0...+70	<550	<137	<250		TTL-TS
Am 2732 APC	Amd	24-DIP	NMOS	0...+70	<550	<137	<250		TTL-TS
C 2732	Int	24-DIC	NMOS	0...+70	<787	<157	<450		TTL-TS
C 2732-6	Int	24-DIC	NMOS	0...+70	<787	<157	<550		TTL-TS
C 2732 A	Int	24-DIC	NMOS	0...+70	<787	<184	<250		TTL-TS
C 2732 A-2	Int	24-DIC	NMOS	0...+70	<787	<184	<200		TTL-TS
C 2732 A-20	Int	24-DIC	NMOS	0...+70	<687	<192	<200		TTL-TS
C 2732 A-25	Int	24-DIC	NMOS	0...+70	<687	<192	<250		TTL-TS
C 2732 A-3	Int	24-DIC	NMOS	0...+70	<656	<184	<300		TTL-TS
C 2732 A-30	Int	24-DIC	NMOS	0...+70	<687	<192	<300		TTL-TS
C 2732 A-4	Int	24-DIC	NMOS	0...+70	<656	<184	<450		TTL-TS
ETC 2732 Q-3	Tho	24-DIC	CMOS	0...+70	<55	<5,5	<350		TTL-TS
ETC 2732 Q-35	Tho	24-DIC	CMOS	0...+70	<55	<5,5	<350		TTL-TS
ETC 2732 Q-45	Tho	24-DIC	CMOS	0...+70	<55	<5,5	<450		TTL-TS
ETC 2732 Q-55	Tho	24-DIC	CMOS	0...+70	<55	<5,5	<550		TTL-TS
ETC 2732 QD-35	Tho	24-DIC	CMOS	-20...+70	<55	<5,5	<350		TTL-TS
ETC 2732 QD-45	Tho	24-DIC	CMOS	-20...+70	<55	<5,5	<450		TTL-TS
ETC 2732 QD-55	Tho	24-DIC	CMOS	-20...+70	<55	<5,5	<550		TTL-TS
ETC 2732 QE-35	Tho	24-DIC	CMOS	-25...+70	<55	<5,5	<350		TTL-TS
ETC 2732 QE-45	Tho	24-DIC	CMOS	-25...+70	<55	<5,5	<450		TTL-TS
ETC 2732 QE-55	Tho	24-DIC	CMOS	-25...+70	<55	<5,5	<550		TTL-TS
ETC 2732 QV-35	Tho	24-DIC	CMOS	-40...+85	<55	<5,5	<350		TTL-TS
ETC 2732 QV-45	Tho	24-DIC	CMOS	-40...+85	<55	<5,5	<450		TTL-TS
ETC 2732 QV-55	Tho	24-DIC	CMOS	-40...+85	<55	<5,5	<550		TTL-TS
F 2732	Fch	24-DIC	NMOS		750	150	<450		TTL-TS
HN 462732	Hit	24-DIC	NMOS	0...+70	<150	<30	<450		TTL-TS
HN 462732 G	Hit	24-DIC	NMOS	0...+70	<150	<30	<450		TTL-TS
HN 462732 G-2	Hit	24-DIC	NMOS	0...+70	<150	<30	<390		TTL-TS
HN 482732 AG-20	Hit	24-DIC	NMOS	0...+70			<200		TTL-TS
HN 482732 AG-25	Hit	24-DIC	NMOS	0...+70			<250		TTL-TS
HN 482732 AG-30	Hit	24-DIC	NMOS	0...+70			<300		TTL-TS
M5L2732 K	Mit	24-DIC	NMOS	0...+70	750	325	<450		TTL-TS
M5L2732 K-6	Mit	24-DIC	NMOS	0...+70	750	325	<550		TTL-TS
MB 8532-35	Fui	24-DIP	NMOS	0...+70	<825	<165	<350		TTL-TS
MB 8532-45	Fui	24-DIP	NMOS	0...+70	<825	<165	<450		TTL-TS

2732 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MBM 2732 A-20	Fui	24-DIC	NMOS	0...+70	<787	<184	<200		TTL-TS
MBM 2732 A-25	Fui	24-DIC	NMOS	0...+70	<787	<184	<250		TTL-TS
MBM 2732 A-30	Fui	24-DIC	NMOS	0...+70	<787	<184	<300		TTL-TS
MBM 2732 A-35	Fui	24-DIC	NMOS	0...+70	<825	<165	<350		TTL-TS
NMC 27C32-35	Nsc	24-DIC	CMOS	0...+70	<26,25	<0,53	<350		TTL-TS
NMC 27C32-45	Nsc	24-DIC	CMOS	0...+70	<26,25	<0,53	<450		TTL-TS
NMC 27C32E-45	Nsc	24-DIC	CMOS	-40...+85	<26,25	<0,53	<450		TTL-TS
NMC 27C32H-45	Nsc	24-DIC	CMOS	0...+70	<26,25	<0,53	<450		TTL-TS
TMM 2732 D	Tos	24-DIC	NMOS	0...+70	<787	<131	<350		TTL-TS
TMM 2732 D-2	Tos	24-DIC	NMOS	0...+70	<787	<131	<350		TTL-TS
µPD 2732 AD	Nip	24-DIP	NMOS	-10...+80	<688	<165	<250		TTL-TS
µPD 2732 AD-2	Nip	24-DIP	NMOS	-10...+80	<688	<165	<200		TTL-TS
µPD 2732 AD-3	Nip	24-DIP	NMOS	-10...+80	<688	<165	<300		TTL-TS
µPD 2732 C	Nip	24-DIP	NMOS	-10...+80	<825	<165	<450		TTL-TS
µPD 2732 D	Nip	24-DIP	NMOS	-10...+80	<825	<165	<450		TTL-TS
µPD 2732 D-4	Nip	24-DIP	NMOS	-10...+80	<825	<165	<390		TTL-TS

2732

4096x8-Bit EPROM

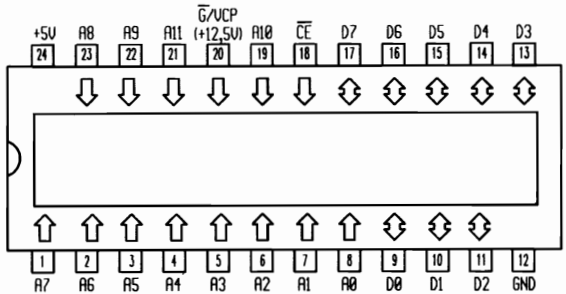


$\overline{CE}/V_{pp}$	D_{out}	Mode
L	data out	read
H	Hi-Z	output disable
H	Hi-Z	standby
pulsed $V_{iLP} \sqcap V_{iHP}$	data in	program

L = −0,1... + 0,8V
H = + 2... + 6V
V_{iLP} = + 2... + 6V
V_{iHP} = + 24... + 26V

2732 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 68732 C	Mot	24-DIC	NMOS	0...+70	<660	<131	<450		TTL-TS
MCM 68732 C-35	Mot	24-DIC	NMOS	0...+70	<880	<137	<350		TTL-TS
MCM 68L732 C	Mot	24-DIC	NMOS	0...+70	<315	<78	<450		TTL-TS
MCM 68L732 C-35	Mot	24-DIC	NMOS	0...+70	<550	<137	<350		TTL-TS

2732 — 4096x8-Bit EPROM

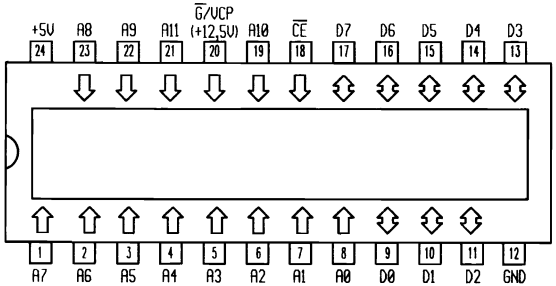


C̄E	Ḡ/V_{pp}	V_{cc}	D_{out}	Mode
L	L	+5V	data out	read
H	X	+5V	Hi-Z	standby
L	+13V	+6V	data in	program
L	L	+6V	data out	program verify
H	+13V	+6V	Hi-Z	program inhibit

2732 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27C32 BQ200	Nsc	24-DIC	CMOS	0...+70	<27,5	<0,55	<200		TTL-TS
NMC 27C32 BQ350	Nsc	24-DIC	CMOS	0...+70	<27,5	<0,55	<350		TTL-TS
NMC 27C32 BQE200	Nsc	24-DIC	CMOS	-40...+85	<27,5	<0,55	<200		TTL-TS
NMC 27C32 BQE350	Nsc	24-DIC	CMOS	-40...+85	<27,5	<0,55	<350		TTL-TS
TMS 27C32-100 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<100		TTL-TS
TMS 27C32-100 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<100		TTL-TS
TMS 27C32-100 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<100		TTL-TS
TMS 27C32-100 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<100		TTL-TS

2732 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27C32-10 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<100		TTL-TS
TMS 27C32-10 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<100		TTL-TS
TMS 27C32-10 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<100		TTL-TS
TMS 27C32-10 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<100		TTL-TS
TMS 27C32-120 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<120		TTL-TS
TMS 27C32-120 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<120		TTL-TS
TMS 27C32-120 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<120		TTL-TS
TMS 27C32-120 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<120		TTL-TS
TMS 27C32-12 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<120		TTL-TS
TMS 27C32-12 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<120		TTL-TS
TMS 27C32-12 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<120		TTL-TS
TMS 27C32-12 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<120		TTL-TS
TMS 27C32-150 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<150		TTL-TS
TMS 27C32-150 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<150		TTL-TS
TMS 27C32-150 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<150		TTL-TS
TMS 27C32-150 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<150		TTL-TS
TMS 27C32-15 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<150		TTL-TS
TMS 27C32-15 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<150		TTL-TS
TMS 27C32-15 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<150		TTL-TS
TMS 27C32-15 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<150		TTL-TS
TMS 27C32-20 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<200		TTL-TS
TMS 27C32-20 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<200		TTL-TS
TMS 27C32-20 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<200		TTL-TS
TMS 27C32-20 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<200		TTL-TS
TMS 27C32-25 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<250		TTL-TS
TMS 27C32-25 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<250		TTL-TS
TMS 27C32-25 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<250		TTL-TS
TMS 27C32-25 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<250		TTL-TS
TMS 27C32-2 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<200		TTL-TS
TMS 27C32-2 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<200		TTL-TS
TMS 27C32-2 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<200		TTL-TS
TMS 27C32-2 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<200		TTL-TS
TMS 27C32 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<250		TTL-TS
TMS 27C32 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<250		TTL-TS
TMS 27C32 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<250		TTL-TS
TMS 27C32 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<250		TTL-TS

2732 — 4096x8-Bit PROM

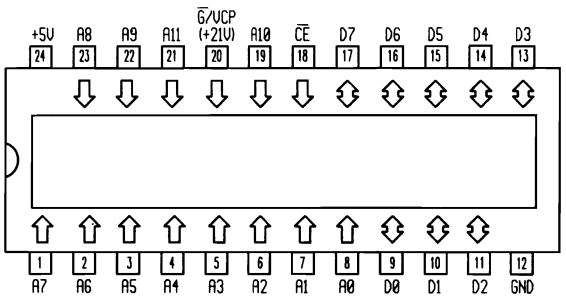


$\overline{CE}$	$\overline{G}/V_{pp}$	V_{cc}	D_{out}	Mode
L	L	+ 5V	data out	read
H	X	+ 5V	Hi-Z	standby
L	+ 13V	+ 6V	data in	program
L	L	+ 6V	data out	program verify
H	+ 13V	+ 6V	Hi-Z	program inhibit

2732 Type	Man	Case	Techn.	TU°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC32-120 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<120		TTL-TS
TMS 27PC32-120 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<120		TTL-TS
TMS 27PC32-120 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<120		TTL-TS
TMS 27PC32-120 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<120		TTL-TS
TMS 27PC32-12 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<120		TTL-TS
TMS 27PC32-12 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<120		TTL-TS
TMS 27PC32-12 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<120		TTL-TS
TMS 27PC32-12 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<120		TTL-TS

2732 Type	Man	Case	Techn.	TU°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC32-150 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<150		TTL-TS
TMS 27PC32-150 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<150		TTL-TS
TMS 27PC32-150 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<150		TTL-TS
TMS 27PC32-150 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<150		TTL-TS
TMS 27PC32-15 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<150		TTL-TS
TMS 27PC32-15 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<150		TTL-TS
TMS 27PC32-15 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<150		TTL-TS
TMS 27PC32-15 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<150		TTL-TS
TMS 27PC32-20 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<200		TTL-TS
TMS 27PC32-20 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<200		TTL-TS
TMS 27PC32-20 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<200		TTL-TS
TMS 27PC32-20 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<200		TTL-TS
TMS 27PC32-25 JE	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<250		TTL-TS
TMS 27PC32-25 JE4	Tix	24-DIC	CMOS	-40...+85	<137,5	<2,75	<250		TTL-TS
TMS 27PC32-25 JL	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<250		TTL-TS
TMS 27PC32-25 JL4	Tix	24-DIC	CMOS	0...+70	<137,5	<2,75	<250		TTL-TS
TMS 27PC32-2 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<200		TTL-TS
TMS 27PC32-2 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<200		TTL-TS
TMS 27PC32-2 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<200		TTL-TS
TMS 27PC32-2 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<200		TTL-TS
TMS 27PC32 JE	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<250		TTL-TS
TMS 27PC32 JE4	Tix	24-DIC	CMOS	-40...+85	<131	<2,62	<250		TTL-TS
TMS 27PC32 JL	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<250		TTL-TS
TMS 27PC32 JL4	Tix	24-DIC	CMOS	0...+70	<131	<2,62	<250		TTL-TS

2732 — 4096x8-Bit EPROM

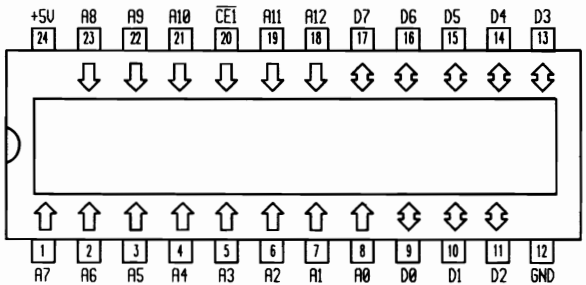


CE	G/VCP	D_{out}	Mode
L	L	data out	read
H	X	Hi-Z	standby
L	+21V	data in	program
L	L	data out	program verify
H	+21V	Hi-Z	program inhibit

L = −0,1... + 0,8V
H = + 2... + 6V

2732 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 2732 A-2F1	Sgs	24-DIC	NMOS	0...+70	<656	<184	<200		TTL-TS
M 2732 A-3F1	Sgs	24-DIC	NMOS	0...+70	<656	<184	<300		TTL-TS
M 2732 A-4F1	Sgs	24-DIC	NMOS	0...+70	<656	<184	<450		TTL-TS
M 2732 A-4F6	Sgs	24-DIC	NMOS	-40...+85	<656	<184	<450		TTL-TS
M 2732 AF1	Sgs	24-DIC	NMOS	0...+70	<656	<184	<250		TTL-TS
M 2732 AF6	Sgs	24-DIC	NMOS	-40...+85	<656	<184	<250		TTL-TS
TMS 2732 A-17 JL	Tix	24-DIC	NMOS	0...+70	<656	<157,5	<170		TTL-TS
TMS 2732 A-17 JP4	Tix	24-DIC	NMOS	-10...+85	<825	<192,5	<170		TTL-TS
TMS 2732 A-20 JL	Tix	24-DIC	NMOS	0...+70	<656	<157,5	<200		TTL-TS
TMS 2732 A-20 JP4	Tix	24-DIC	NMOS	-10...+85	<825	<192,5	<200		TTL-TS
TMS 2732 A-25 JL	Tix	24-DIC	NMOS	0...+70	<656	<157,5	<250		TTL-TS
TMS 2732 A-25 JP4	Tix	24-DIC	NMOS	-10...+85	<825	<192,5	<250		TTL-TS
TMS 2732 A-45 JL	Tix	24-DIC	NMOS	0...+70	<656	<157,5	<450		TTL-TS
TMS 2732 A-45 JP4	Tix	24-DIC	NMOS	-10...+85	<825	<192,5	<450		TTL-TS
TMS 27P32 A-25 NL	Tix	24-DIP	NMOS	0...+70	<656	<157,5	<250		TTL-TS
TMS 27P32 A-30 NL	Tix	24-DIP	NMOS	0...+70	<656	<157,5	<300		TTL-TS
TMS 27P32 A-45 NL	Tix	24-DIP	NMOS	0...+70	<656	<157,5	<450		TTL-TS

2749 — 8192x8-Bit EPROM

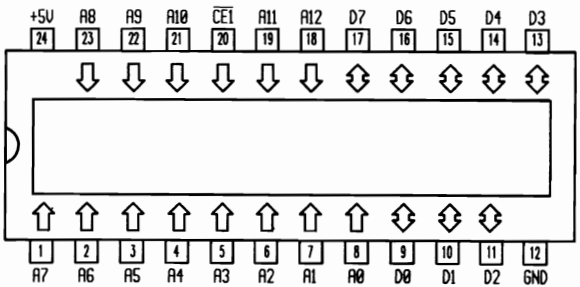


A12	A11	CE/PE	A10	A9	A8	Dn	Mode
x	x	L	x	x	x	data out	read
x	x	H	x	x	x	Hi-Z	output disable
L	+13,5V	L	latch	H	L	data out	program verify L-Level
H	+13,5V	L	latch	H	L	data out	program verify H-Level
L	+13,5V	H	latch	H	H	Hi-Z	program inhibit
L	+13,5V	L	latch	L	H	data in	program
L	L	+12V	latch	L	L	L-Level	blank check L-Level
L	H	+12V	latch	L	L	H-Level	blank check H-Level
x	x	L	x	+12V	x	code 97	signature
x	x	L	x	+12V	x	code F2	signature

2749 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27C49 Q45	Nsc	24-DIC	CMOS	0...+70	<360		<45		TTL-TS
NMC 27C49 Q55	Nsc	24-DIC	CMOS	0...+70	<360		<55		TTL-TS
NMC 27C49 Q70	Nsc	24-DIC	CMOS	0...+70	<360		<70		TTL-TS
TMS 27C49-45 JL	Tix	24-DIC	CMOS	0...+70	<495		<45		TTL-TS
TMS 27C49-45 JTL	Tix	24-TDIC	CMOS	0...+70	<495		<45		TTL-TS
TMS 27C49-4 JL	Tix	24-DIC	CMOS	0...+70	<472,5		<45		TTL-TS
TMS 27C49-4 JTL	Tix	24-TDIC	CMOS	0...+70	<472,5		<45		TTL-TS
TMS 27C49-55 JL	Tix	24-DIC	CMOS	0...+70	<495		<55		TTL-TS

2749 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27C49-55 JTL	Tix	24-TDIC	CMOS	0...+70	<495		<55		TTL-TS
TMS 27C49-5 JL	Tix	24-DIC	CMOS	0...+70	<472,5		<55		TTL-TS
TMS 27C49-5 JTL	Tix	24-TDIC	CMOS	0...+70	<472,5		<55		TTL-TS

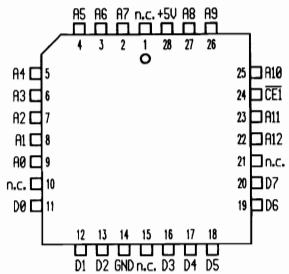
2749 — 8192x8-Bit PROM



A12	A11	CE/PE	A10	A9	A8	Dn	Mode
x	x	L	x	x	x	data out	read
x	x	H	x	x	x	Hi-Z	output disable
L	+13,5V	L	latch	H	L	data out	program verify L-Level
H	+13,5V	L	latch	H	L	data out	program verify H-Level
L	+13,5V	H	latch	H	H	Hi-Z	program inhibit
L	+13,5V	L	latch	L	H	data in	program
L	L	+12V	latch	L	L	L-Level	blank check L-Level
L	H	+12V	latch	L	L	H-Level	blank check H-Level
x	x	L	x	+12V	x	code 97	signature
x	x	L	x	+12V	x	code F2	signature

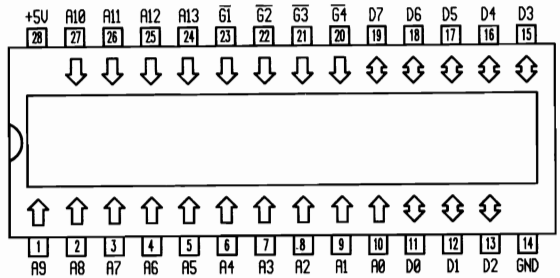
2749 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC49-45 NL	Tix	24-DIP	CMOS	0...+70	<495		<45		TTL-TS
TMS 27PC49-45 NTL	Tix	24-TDIP	CMOS	0...+70	<495		<45		TTL-TS
TMS 27PC49-4 NL	Tix	24-DIP	CMOS	0...+70	<472,5		<45		TTL-TS
TMS 27PC49-4 NTL	Tix	24-TDIP	CMOS	0...+70	<472,5		<45		TTL-TS
TMS 27PC49-55 NL	Tix	24-DIP	CMOS	0...+70	<495		<55		TTL-TS
TMS 27PC49-55 NTL	Tix	24-TDIP	CMOS	0...+70	<495		<55		TTL-TS
TMS 27PC49-5 NL	Tix	24-DIP	CMOS	0...+70	<472,5		<55		TTL-TS
TMS 27PC49-5 NTL	Tix	24-TDIP	CMOS	0...+70	<472,5		<55		TTL-TS

2749 — 8192x8-Bit PROM



A12	A11	CE/PE	A10	A9	A8	Dn	Mode
x	x	L	x	x	x	data out	read
x	x	H	x	x	x	Hi-Z	output disable
L	+13,5V	L	latch	H	L	data out	program verify L-Level
H	+13,5V	L	latch	H	L	data out	program verify H-Level
L	+13,5V	H	latch	H	H	Hi-Z	program inhibit
L	+13,5V	L	latch	L	H	data in	program
L	L	+12V	latch	L	L	L-Level	blank check L-Level
L	H	+12V	latch	L	L	H-Level	blank check H-Level
x	x	L	x	+12V	x	code 97	signature
x	x	L	x	+12V	x	code F2	signature

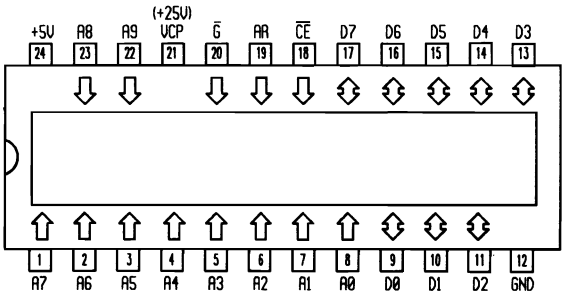
2751 — 16384x8-Bit EPROM



2749 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC49-45 FNL	Tix	28-PLCC	CMOS	0...+70	<495		<45		TTL-TS
TMS 27PC49-4 FNL	Tix	28-PLCC	CMOS	0...+70	<472,5		<45		TTL-TS
TMS 27PC49-55 FNL	Tix	28-PLCC	CMOS	0...+70	<495		<55		TTL-TS
TMS 27PC49-5 FNL	Tix	28-PLCC	CMOS	0...+70	<472,5		<55		TTL-TS

2751 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27C51 Q45	Nsc	28-DIC	CMOS	0...+70	<360		<45		TTL-TS
NMC 27C51 Q55	Nsc	28-DIC	CMOS	0...+70	<360		<55		TTL-TS
NMC 27C51 Q70	Nsc	28-DIC	CMOS	0...+70	<360		<70		TTL-TS

2758 — 1024x8-Bit EPROM

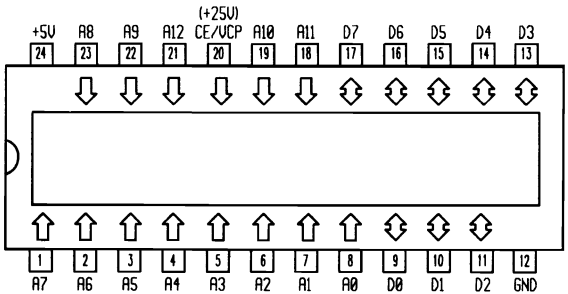


$\overline{CE}$	$\overline{G}$	VCP	D_n	Mode
L	L	+5V	data out	read
L⎍H*	H	+25V	data in	program
L	L	+25V	data out	program verify
H	X	+5V	Hi-Z	standby

* = one 50ms pulse (active high)

2758 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MM 2758 A	Nsc	24-DIC	NMOS	0...+70	<525	<132	<450		TTL-TS
MM 2758 B	Nsc	24-DIC	NMOS	0...+70	<525	<132	<450		TTL-TS
TMS 2508-25	Tix	24-DIC	NMOS	0...+70	<446	<131	<250		TTL-TS
TMS 2508-30	Tix	24-DIC	NMOS	0...+70	<446	<131	<300		TTL-TS
2758	Int	24-DIC	NMOS	0...+70	<551	<157	<450		TTL-TS

2764 — 8192x8-Bit EPROM



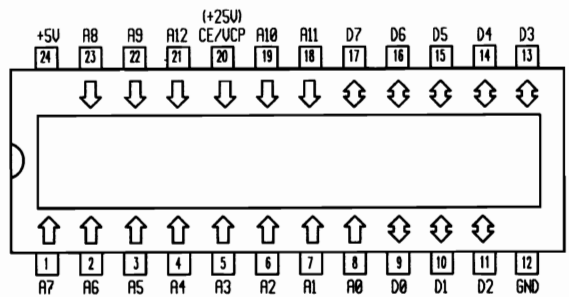
$\overline{CE}/V_{pp}$	D_{out}	Mode
L	data out	read
H	Hi-Z	output disable
H	Hi-Z	standby
pulsed V_{iLP} ⎍ V_{iHP}	data in	program

L = −0,1... +0,8V
H = +2... +6V
V_{iLP} = +2... +6V
V_{iHP} = +24... +26V

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 68764 C	Mot	24-DIC	NMOS	0...+70	<630	<131	<450		TTL-TS
MCM 68764 C-35	Mot	24-DIC	NMOS	0...+70	<880	<137	<350		TTL-TS
MCM 68L764 C	Mot	24-DIC	NMOS	0...+70	<315	<78	<450		TTL-TS

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 68L764 C-35	Mot	24-DIC	NMOS	0...+70	<550	<137	<350		TTL-TS
MCM 68764 L	Mot	24-DIC	NMOS	0...+70	<630	<131	<450		TTL-TS
MCM 68764 L-35	Mot	24-DIC	NMOS	0...+70	<880	<137	<350		TTL-TS
MCM 68L764 L	Mot	24-DIC	NMOS	0...+70	<315	<78	<450		TTL-TS
MCM 68L764 L-35	Mot	24-DIC	NMOS	0...+70	<550	<137	<350		TTL-TS

2764 — 8192x8-Bit EPROM



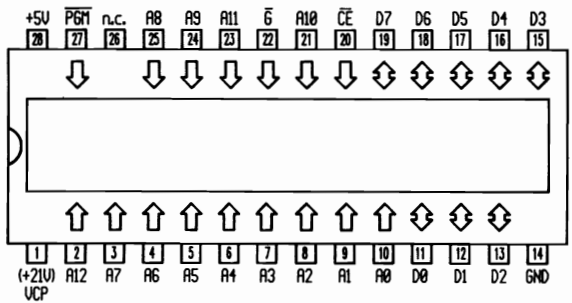
$\overline{CE}/V_{pp}$	D_{out}	Mode
L	data out	read
H	Hi-Z	output disable
pulsed V_{iLP} ⌐ V_{iHP}	data in	program

L = −0,1... +0,8V
H = +2... +6V
V_{iLP} = +2... +6V
V_{iHP} = +24... +26V

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 68766 C	Mot	24-DIC	NMOS	0...+70	<840		<450		TTL-TS
MCM 68766 C-35	Mot	24-DIC	NMOS	0...+70	<840		<350		TTL-TS
MCM 68766 L	Mot	24-DIC	NMOS	0...+70	<840		<450		TTL-TS
MCM 68766 L-35	Mot	24-DIC	NMOS	0...+70	<840		<350		TTL-TS

2764

8192x8-Bit EPROM



CE	G	PGM	VCP	D_{out}	Mode
L	L	H	+5V	data out	read
H	X	X	+5V	Hi-Z	standby
L	X	L	+21V	data in	program
L	L	H	+21V	data out	program verify
H	X	X	+21V	Hi-Z	program inhibit

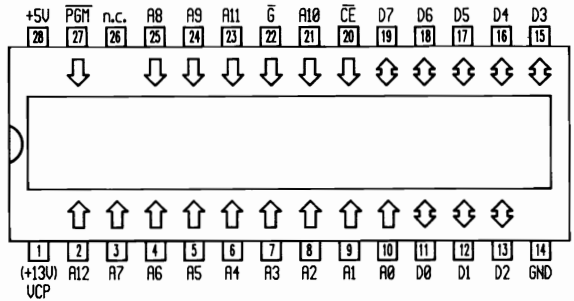
L = −0,1... +0,8V
H = +2... +6V

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2764 DC	Amd	28-DIC	NMOS	0...+70	<525	<105	<250		TTL-TS
Am 2764-2 DC	Amd	28-DIC	NMOS	0...+70	<525	<105	<200		TTL-TS
Am 2764-20 DC	Amd	28-DIC	NMOS	0...+70	<550	<110	<200		TTL-TS
Am 2764-25 DC	Amd	28-DIC	NMOS	0...+70	<550	<110	<250		TTL-TS
Am 2764-3 DC	Amd	28-DIC	NMOS	0...+70	<525	<105	<300		TTL-TS
Am 2764-30 DC	Amd	28-DIC	NMOS	0...+70	<550	<110	<300		TTL-TS
Am 2764-4 DC	Amd	28-DIC	NMOS	0...+70	<525	<105	<450		TTL-TS
Am 2764-45 DC	Amd	28-DIC	NMOS	0...+70	<550	<110	<450		TTL-TS

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 2764 PC	Amd	28-DIP	NMOS	0...+70	<525	<105	<250		TTL-TS
F 2764	Fch	28-DIP	NMOS	0...+70			<200		TTL-TS
HN 27C64 G-15	Hit	28-DIC	CMOS	0...+70	<165		<150		TTL-TS
HN 27C64 G-20	Hit	28-DIC	CMOS	0...+70	<165		<200		TTL-TS
HN 27C64 G-25	Hit	28-DIC	CMOS	0...+70	<165		<250		TTL-TS
HN 27C64 G-30	Hit	28-DIC	CMOS	0...+70	<165		<300		TTL-TS
HN 482764	Hit	28-DIC	NMOS	0...+70	555		<250		TTL-TS
HN 482764-3	Hit	28-DIC	NMOS	0...+70	555		<300		TTL-TS
HN 482764-4	Hit	28-DIC	NMOS	0...+70	555		<450		TTL-TS
HN 482764 G	Hit	28-DIC	NMOS	0...+70	555		<250		TTL-TS
HN 482764 G-2	Hit	28-DIC	NMOS	0...+70	<787	<184	<200		TTL-TS
HN 482764 G-3	Hit	28-DIC	NMOS	0...+70	555		<300		TTL-TS
HN 482764 G-4	Hit	28-DIC	NMOS	0...+70	555		<450		TTL-TS
M 2764 H-25F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<250		TTL-TS
M 2764 H-2F1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<200		TTL-TS
M 2764 H-30F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<300		TTL-TS
M 2764 H-3F1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<300		TTL-TS
M 2764 H-45F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<450		TTL-TS
M 2764 H-4F1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<450		TTL-TS
M 2764 H-4F6	Sgs	28-DIC	NMOS	-40...+85	<525	<210	<450		TTL-TS
M 2764 HF1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<250		TTL-TS
M 2764 HF6	Sgs	28-DIC	NMOS	-40...+85	<525	<210	<250		TTL-TS
M5L2764 K	Mit	28-DIP	NMOS				<250		TTL-TS
MBM 2764-20	Fui	28-DIC	NMOS	0...+70	<787	<184	<200		TTL-TS
MBM 2764-25	Fui	28-DIC	NMOS	0...+70	<787	<184	<250		TTL-TS
MBM 2764-30	Fui	28-DIC	NMOS	0...+70	<787	<184	<300		TTL-TS
MBM 27C64-25	Fui	28-DIC	CMOS	0...+70	<168		<250		TTL-TS
MBM 27C64-30	Fui	28-DIC	CMOS	0...+70	<168		<300		TTL-TS
MN 2764-20	Mat	28-DIC	NMOS	0...+70	<825	<27,5	<200		TTL-TS
MN 2764-25	Mat	28-DIC	NMOS	0...+70	<825	<27,5	<250		TTL-TS
TMM 2764 D	Tos	28-DIC	NMOS	0...+70	<630	<184	<250		TTL-TS
TMM 2764 D-2	Tos	28-DIC	NMOS	0...+70	<630	<184	<200		TTL-TS
TMS 2764-17 JL	Tix	28-DIC	NMOS	0...+70	<787	<184	<170		TTL-TS
TMS 2764-17 JP4	Tix	28-DIC	NMOS	-10...+85	<787	<220	<170		TTL-TS
TMS 2764-20 JL	Tix	28-DIC	NMOS	0...+70	<787	<184	<200		TTL-TS
TMS 2764-20 JP4	Tix	28-DIC	NMOS	-10...+85	<787	<220	<200		TTL-TS
TMS 2764-25 JL	Tix	28-DIC	NMOS	0...+70	<787	<184	<250		TTL-TS

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 2764-25 JP4	Tix	28-DIC	NMOS	-10...+85	<787	<220	<250		TTL-TS
TMS 2764-45 JL	Tix	28-DIC	NMOS	0...+70	<787	<184	<450		TTL-TS
TMS 2764-45 JP4	Tix	28-DIC	NMOS	-10...+85	<787	<220	<450		TTL-TS
TMS 27P64-25 NL	Tix	28-DIP	NMOS	0...+70	<787	<184	<250		TTL-TS
TMS 27P64-30 NL	Tix	28-DIP	NMOS	0...+70	<787	<184	<300		TTL-TS
TMS 27P64-45 NL	Tix	28-DIP	NMOS	0...+70	<787	<184	<450		TTL-TS
2764	Int	28-DIP	NMOS	0...+70	<525	<210	<250		TTL-TS
2764-2	Int	28-DIP	NMOS	0...+70	<525	<210	<200		TTL-TS
2764-25	Int	28-DIP	NMOS	0...+70	<550	<220	<250		TTL-TS
2764-3	Int	28-DIP	NMOS	0...+70	<525	<210	<300		TTL-TS
2764-30	Int	28-DIP	NMOS	0...+70	<550	<220	<300		TTL-TS
2764-4	Int	28-DIP	NMOS	0...+70	<525	<210	<450		TTL-TS
2764-45	Int	28-DIP	NMOS	0...+70	<550	<220	<450		TTL-TS
µPD 2764 D	Nip	28-DIP	NMOS	-10...+80	<440	<137	<250		TTL-TS
µPD 2764 D-2	Nip	28-DIP	NMOS	-10...+80	<440	<137	<200		TTL-TS
µPD 2764 D-3	Nip	28-DIP	NMOS	-10...+80	<440	<137	<300		TTL-TS
µPD 2764 D-4	Nip	28-DIP	NMOS	-10...+80	<440	<137	<450		TTL-TS

2764 — 8192x8-Bit EPROM



PGM	CE	G	V_{PP}	V_{CC}	D_n	Power	Mode
H	L	L	+5V	+5V	data out	active	read
X	X	H	+5V	+5V	Hi-Z	active	output deselect
X	H	X	+5V	+5V	Hi-Z	standby	standby
L	L	X	+12,5V	+6V	data in	active	program
X	H	X	+12,5V	+6V	Hi-Z	active	program inhibit
H	L	H	+12,5V	+6V	Hi-Z	active	program inhibit
H	L	L	+12,5V	+6V	data out	active	program verify

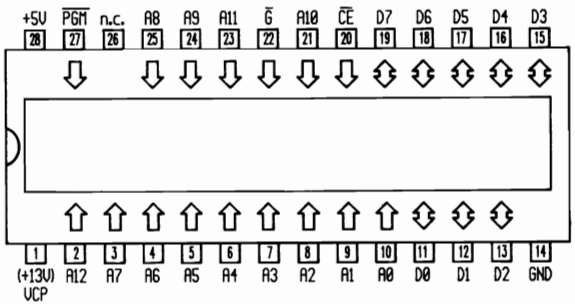
2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 2764 A-20F1	Sgs	28-DIC	NMOS	0...+70	<412	<192	<200		TTL-TS
M 2764 A-25F1	Sgs	28-DIC	NMOS	0...+70	<330	<110	<250		TTL-TS
M 2764 A-2F1	Sgs	28-DIC	NMOS	0...+70	<394	<184	<200		TTL-TS
M 2764 A-30F1	Sgs	28-DIC	NMOS	0...+70	<330	<110	<300		TTL-TS
M 2764 A-3F1	Sgs	28-DIC	NMOS	0...+70	<315	<105	<300		TTL-TS
M 2764 A-45F1	Sgs	28-DIC	NMOS	0...+70	<330	<110	<450		TTL-TS
M 2764 A-4F1	Sgs	28-DIC	NMOS	0...+70	<315	<105	<450		TTL-TS
M 2764 A-4F6	Sgs	28-DIC	NMOS	-40...+85	<315	<105	<450		TTL-TS

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 2764 AF1	Sgs	28-DIC	NMOS	0...+70	<315	<105	<250		TTL-TS
M 2764 AF6	Sgs	28-DIC	NMOS	-40...+85	<315	<105	<250		TTL-TS
NMC 27C64 Q15	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<150		TTL-TS
NMC 27C64 Q150	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<150		TTL-TS
NMC 27C64 Q200	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<200		TTL-TS
NMC 27C64 Q250	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<250		TTL-TS
NMC 27C64 Q300	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<300		TTL-TS
NMC 27C64 QE200	Nsc	28-DIC	CMOS	-40...+85	<55	<0,55	<200		TTL-TS
NMC 27C64 QM200	Nsc	28-DIC	CMOS	-55...+125	<55	<0,55	<200		TTL-TS
NMC 27C64 QM250	Nsc	28-DIC	CMOS	-55...+125	<55	<0,55	<250		TTL-TS
TMM 2764 AD-15	Tos	28-DIP	NMOS	0...+70	<550	<165	<150		TTL-TS
TMM 2764 AD-150	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<150		TTL-TS
TMM 2764 AD-20	Tos	28-DIP	NMOS	0...+70	<550	<165	<200		TTL-TS
TMM 2764 AD-200	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<200		TTL-TS
TMM 2764 ADI-15	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<150		TTL-TS
TMM 2764 ADI-20	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<200		TTL-TS
TMS 27C64-100 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<100		TTL-TS
TMS 27C64-100 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<100		TTL-TS
TMS 27C64-100 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<100		TTL-TS
TMS 27C64-100 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<100		TTL-TS
TMS 27C64-120 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<120		TTL-TS
TMS 27C64-120 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<120		TTL-TS
TMS 27C64-120 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<120		TTL-TS
TMS 27C64-120 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<120		TTL-TS
TMS 27C64-12 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<120		TTL-TS
TMS 27C64-12 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<120		TTL-TS
TMS 27C64-12 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<120		TTL-TS
TMS 27C64-12 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<120		TTL-TS
TMS 27C64-15 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27C64-15 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27C64-15 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27C64-15 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27C64-1 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27C64-1 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27C64-1 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27C64-1 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27C64-20 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27C64-20 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27C64-20 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27C64-20 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27C64-25 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27C64-25 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27C64-25 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27C64-25 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27C64-2 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27C64-2 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27C64-2 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27C64-2 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27C64 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27C64 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27C64 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS
TMS 27C64 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS
TS 27C64-15 CQ	Tho	28-DIC	CMOS	0...+70	<110	<5,5	<150		TTL-TS
TS 27C64-15 VQ	Tho	28-DIC	CMOS	-40...+85	<110	<5,5	<150		TTL-TS
TS 27C64-20 CQ	Tho	28-DIC	CMOS	0...+70	<110	<5,5	<200		TTL-TS
TS 27C64-20 VQ	Tho	28-DIC	CMOS	-40...+85	<110	<5,5	<200		TTL-TS
TS 27C64-25 CQ	Tho	28-DIC	CMOS	0...+70	<110	<5,5	<250		TTL-TS
TS 27C64-25 MQ	Tho	28-DIC	CMOS	-55...+125	<110	<5,5	<250		TTL-TS
TS 27C64-25 VQ	Tho	28-DIC	CMOS	-40...+85	<110	<5,5	<250		TTL-TS
TS 27C64-30 CQ	Tho	28-DIC	CMOS	0...+70	<110	<5,5	<300		TTL-TS
TS 27C64-30 MQ	Tho	28-DIC	CMOS	-55...+125	<110	<5,5	<300		TTL-TS
TS 27C64-30 VQ	Tho	28-DIC	CMOS	-40...+85	<110	<5,5	<300		TTL-TS
27C64 A-10 FA	Phi	28-DIC	CMOS	0...+70	<110	<5,5	<100		TTL-TS
27C64 A-12 FA	Phi	28-DIC	CMOS	0...+70	<110	<5,5	<120		TTL-TS
27C64 A-15 FA	Phi	28-DIC	CMOS	0...+70	<110	<5,5	<150		TTL-TS
27C64 A-20	Val	28-DIC	CMOS	0...+70	<165	<5,5	<200		TTL-TS
27C64 A-20 FA	Phi	28-DIC	CMOS	0...+70	<110	<5,5	<200		TTL-TS
27C64 A-25	Val	28-DIC	CMOS	0...+70	<110	<5,5	<250		TTL-TS
27C64 A-30	Val	28-DIC	CMOS	0...+70	<110	<5,5	<300		TTL-TS
27C64 AI15 FA	Phi	28-DIC	CMOS	-40...+85	<110	<5,5	<150		TTL-TS
27C64 AI15 N	Phi	28-DIP	CMOS	-40...+85	<110	<5,5	<150		TTL-TS
27C64 AI20 FA	Phi	28-DIC	CMOS	-40...+85	<110	<5,5	<200		TTL-TS
27C64 AI20 N	Phi	28-DIP	CMOS	-40...+85	<110	<5,5	<200		TTL-TS

2764

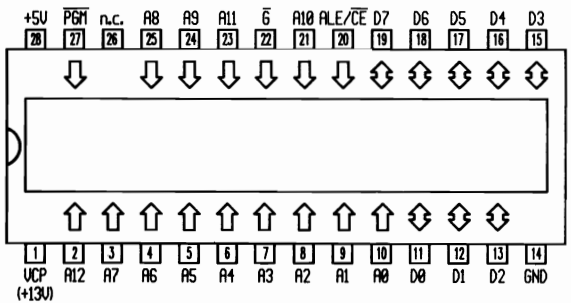
8192x8-Bit PROM



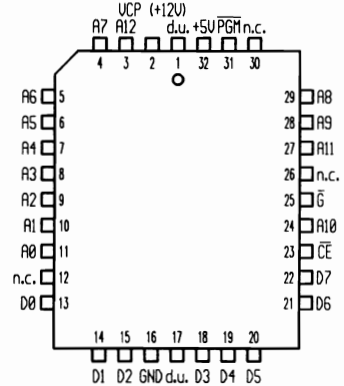
PGM	CE	G	V_{PP}	V_{CC}	D_n	Power	Mode
H	L	L	+5V	+5V	data out	active	read
X	X	H	+5V	+5V	Hi-Z	active	output deselect
X	H	X	+5V	+5V	Hi-Z	standby	standby
L	L	X	+12,5V	+6V	data in	active	program
X	H	X	+12,5V	+6V	Hi-Z	active	program inhibit
H	L	H	+12,5V	+6V	Hi-Z	active	program inhibit
H	L	L	+12,5V	+6V	data out	active	program verify

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC64-120 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<120		TTL-TS
TMS 27PC64-120 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<120		TTL-TS
TMS 27PC64-120 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<120		TTL-TS
TMS 27PC64-120 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<120		TTL-TS
TMS 27PC64-12 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<120		TTL-TS
TMS 27PC64-12 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<120		TTL-TS
TMS 27PC64-12 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<120		TTL-TS
TMS 27PC64-12 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<120		TTL-TS
TMS 27PC64-15 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27PC64-15 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27PC64-15 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27PC64-15 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27PC64-1 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27PC64-1 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27PC64-1 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27PC64-1 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27PC64-20 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC64-20 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC64-20 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC64-20 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC64-25 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC64-25 JE4	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC64-25 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27PC64-25 JL4	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27PC64-2 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27PC64-2 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27PC64-2 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC64-2 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC64 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC64 JE4	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC64 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS
TMS 27PC64 JL4	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS

2764 8192x8-Bit EPROM



CE/ALE	G	PGM	V_{pp}	V_{cc}	D_n	Mode
L	L	H	+5V	+5V	data out	read
L	X	X	+5V	+5V	Hi-Z	standby
L	H	pulsed H→L→H	+13V	+6V	data in	program
L	L	H	+13V	+6V	data out	program verify
H	X	X	+13V	+6V	Hi-Z	program inhibit

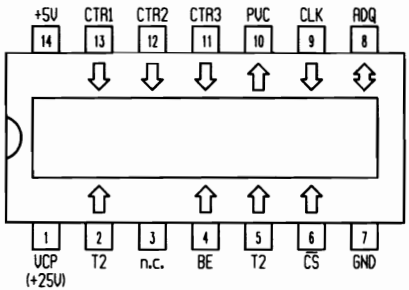


PGM	CE	G	V_{PP}	V_{CC}	D_n	Power	Mode
H	L	L	+5V	+5V	data out	active	read
X	X	H	+5V	+5V	Hi-Z	active	output deselect
X	H	X	+5V	+5V	Hi-Z	standby	standby
L	L	X	+12,5V	+6V	data in	active	program
X	H	X	+12,5V	+6V	Hi-Z	active	program inhibit
H	L	H	+12,5V	+6V	Hi-Z	active	program inhibit
H	L	L	+12,5V	+6V	data out	active	program verify

2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
87C64-20	Val	28-DIC	CMOS	0...+70	<165	<5,5	<200		TTL-TS
87C64-25	Val	28-DIC	CMOS	0...+70	<110	<5,5	<250		TTL-TS
87C64-30	Val	28-DIC	CMOS	0...+70	<110	<5,5	<300		TTL-TS

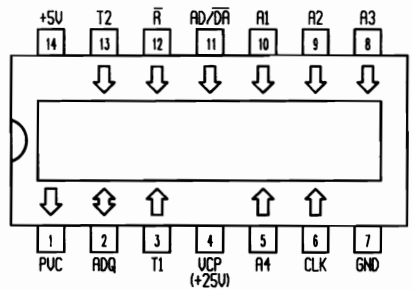
2764 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
27C64 AI15 A	Phi	32-LCC	CMOS	-40...+85	<110	<5,5	<150		TTL-TS
27C64 AI20 A	Phi	32-LCC	CMOS	-40...+85	<110	<5,5	<200		TTL-TS

2801 — 16x16-Bit EEPROM



V_{PP}	$\overline{CS}$	CTR3	CTR2	CTR1	Mode
GND or +5V	H	H	H	H	standby
+28V	L	H	L	L	word erase
+28V	L	H	H	L	write
GND or +5V	L	H	H	L	serial data out
GND or +5V	L	L	L	H	serial data in
GND or +5V	L	L	H	H	read
GND or +5V	H	L	L	L	standby

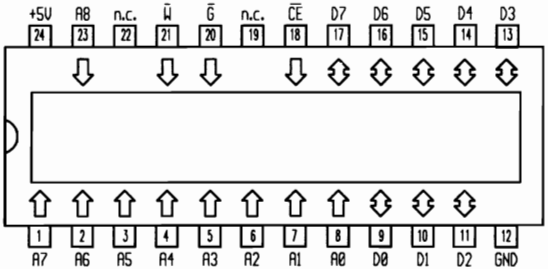
2802 — 32x32-Bit EEPROM



2801 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 2801	Mot	14-DIP	NMOS	0...+70	<165				

2802 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 2802 L	Mot	14-DIC	NMOS	-40...+85			10		

2804 — 512x8-Bit EEPROM



$\overline{CS}$	$\overline{G}$	$\overline{W}$	D_n	Power	Mode
L	L	H	data out	active	read
L	H	L	data in	active	write
H	X	X	Hi-Z	standby	standby + write inhibit
X	L	X	—	—	write inhibit
X	X	H	—	—	write inhibit

2814 — 256x8-Bit serial EEPROM

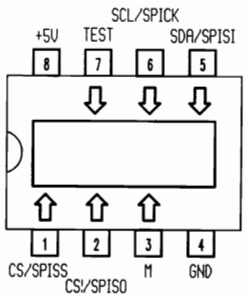
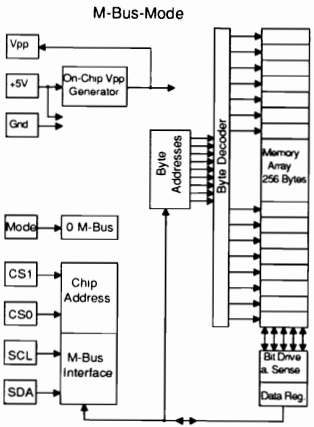


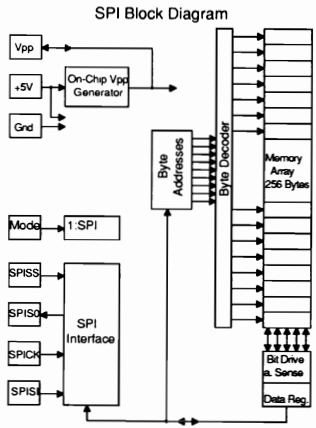
Tabelle siehe Seite 2-110

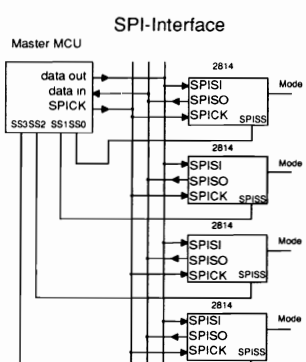
2804 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLS 2804 AP-250	Exl	24-DIP	NMOS	0...+70	<440	<220	<250		TTL
XLS 2804 AP-300	Exl	24-DIP	NMOS	0...+70	<440	<220	<300		TTL
XLS 2804 AP-350	Exl	24-DIP	NMOS	0...+70	<440	<220	<350		TTL
XLS 2804 AP-450	Exl	24-DIP	NMOS	0...+70	<440	<220	<450		TTL

2814 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 2814 P	Mot	8-DIP	CMOS	0...+70					

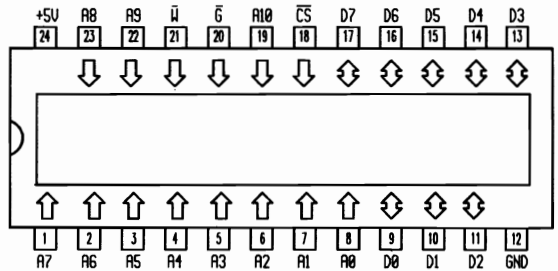
2814 — 256x8-Bit serial EEPROM







2816 — 2048x8-Bit EEPROM

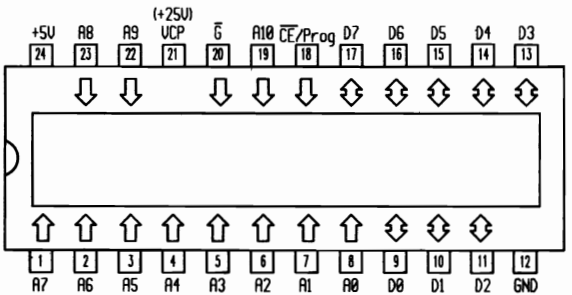


C̄S	Ḡ	W̄	D_n	Power	Mode
L	L	H	data out	active	read
L	H	L	data in	active	write
H	X	X	Hi-Z	standby	standby + write inhibit
X	L	X	—	—	write inhibit
X	X	H	—	—	write inhibit

2816 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 2816 A-25	Sam	24-DIP	NMOS	0...+70	<550	<275	<250		
KM 2816 A-30	Sam	24-DIP	NMOS	0...+70	<550	<275	<300		
KM 2816 A-35	Sam	24-DIP	NMOS	0...+70	<550	<275	<350		
XLM 2816 AC-300	Exl	24-DIC	NMOS	-55...+125	<660	<275	<300		TTL
XLM 2816 AC-350	Exl	24-DIC	NMOS	-55...+125	<660	<275	<350		TTL
XLM 2816 AC-450	Exl	24-DIC	NMOS	-55...+125	<660	<275	<450		TTL
XLS 2816 AC-250	Exl	24-DIC	NMOS	0...+70	<660	<220	<250		TTL
XLS 2816 AC-300	Exl	24-DIC	NMOS	0...+70	<660	<220	<300		TTL

2816 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLS 2816 AC-350	Exl	24-DIC	NMOS	0...+70	<660	<220	<350		TTL
XLS 2816 AC-450	Exl	24-DIC	NMOS	0...+70	<660	<220	<450		TTL
XLS 2816 AP-250	Exl	24-DIP	NMOS	0...+70	<660	<220	<250		TTL
XLS 2816 AP-300	Exl	24-DIP	NMOS	0...+70	<660	<220	<300		TTL
XLS 2816 AP-350	Exl	24-DIP	NMOS	0...+70	<660	<220	<350		TTL
XLS 2816 AP-450	Exl	24-DIP	NMOS	0...+70	<660	<220	<450		TTL

2816 — 2048x8-Bit EEPROM

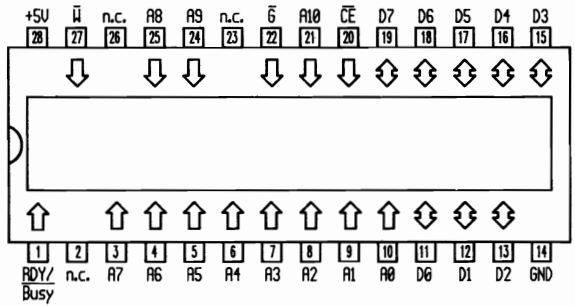


$\overline{CE}$	$\overline{G}$	V_{pp}	D_n	Mode
L	L	+5V	data out	read
H	X	+5V	Hi-Z	standby
L	H	+21V	data in = H	byte erase
L	H	+21V	data in	byte write
L	9V to 15V	+21V	data in = don't care	chip erase
H	X	+5V ⌐ +22V	Hi-Z	E/W inhibit

2816 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 2816 C	Mot	24-DIC	NMOS	0...+70			<450		
MCM 2816 C-35	Mot	24-DIC	NMOS	0...+70			<350		
MCM 2816 L	Mot	24-DIC	NMOS	0...+70			<450		
MCM 2816 L-35	Mot	24-DIC	NMOS	0...+70			<350		
NMC 2816-25 J	Nsc	24-DIC	NMOS	0...+70	<610	<295	<250		TTL-TS
NMC 2816-35 J	Nsc	24-DIC	NMOS	0...+70	<610	<295	<350		TTL-TS
NMC 2816-45 J	Nsc	24-DIC	NMOS	0...+70	<610	<295	<450		TTL-TS
NMC 2816M-25 J	Nsc	24-DIC	NMOS	-55...+125	<800	<360	<250		TTL-TS

2816 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 2816M-35 J	Nsc	24-DIC	NMOS	-55...+125	<800	<360	<350		TTL-TS
NMC 2816M-45 J	Nsc	24-DIC	NMOS	-55...+125	<800	<360	<450		TTL-TS
NMC 9716-25 J	Nsc	24-DIC	NMOS	0...+70	<610	<295	<250		TTL-TS
NMC 9716-35 J	Nsc	24-DIC	NMOS	0...+70	<610	<295	<350		TTL-TS
NMC 9716-45 J	Nsc	24-DIC	NMOS	0...+70	<610	<295	<450		TTL-TS
NMC 9716M-25 J	Nsc	24-DIC	NMOS	-55...+125	<800	<360	<250		TTL-TS
NMC 9716M-35 J	Nsc	24-DIC	NMOS	-55...+125	<800	<360	<350		TTL-TS
NMC 9716M-45 J	Nsc	24-DIC	NMOS	-55...+125	<800	<360	<450		TTL-TS

2817 — 2048x8-Bit EEPROM



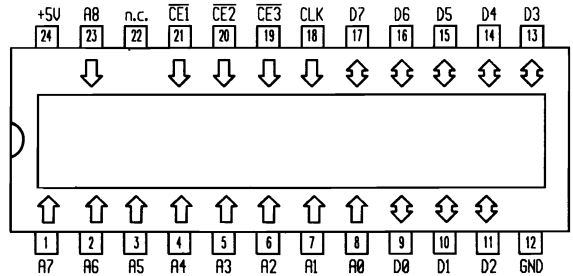
RDY/$\overline{Busy}$ = device ready/busy (open-drain output)

$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	RDY/$\overline{Busy}$	Mode
L	L	H	data out	Hi-Z	read
H	X	X	Hi-Z	Hi-Z	standby
L	H	⌐⌐	data in	L	write
X	X	X	Hi-Z	L	busy

2817 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 2817 A-25	Sam	28-DIP	NMOS	0...+70	<550	<275	<250		
KM 2817 A-30	Sam	28-DIP	NMOS	0...+70	<550	<275	<300		
KM 2817 A-35	Sam	28-DIP	NMOS	0...+70	<550	<275	<350		
NMC 9817-20 J	Nsc	28-DIC	NMOS	0...+75	<420	<131	<200		TTL-TS
NMC 9817-25 J	Nsc	28-DIC	NMOS	0...+75	<420	<131	<250		TTL-TS
NMC 9817-35 J	Nsc	28-DIC	NMOS	0...+75	<420	<131	<350		TTL-TS
TS 28C17 AP	Tho	28-DIC	CMOS	0...+70	<137,5	<5,5	<150		TTL-TS
XLM 2817 AC-300	Exl	28-DIC	NMOS	-55...+125	<660	<275	<300		TTL-TS

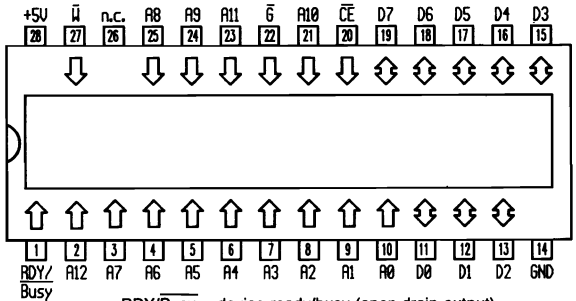
2817 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLM 2817 AC-350	Exl	28-DIC	NMOS	-55...+125	<660	<275	<350		TTL-TS
XLM 2817 AC-450	Exl	28-DIC	NMOS	-55...+125	<660	<275	<450		TTL-TS
XLS 2817 AC-300	Exl	28-DIC	NMOS	0,..+70	<660	<275	<300		TTL-TS
XLS 2817 AC-350	Exl	28-DIC	NMOS	0...+70	<660	<275	<350		TTL-TS
XLS 2817 AC-450	Exl	28-DIC	NMOS	0...+70	<660	<275	<450		TTL-TS

2845 — 512x8-Bit Register PROM



2845 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TBP 28R45 J	Tix	24-DIC	TTL	0...+70	<577		20		TTL-TS
TBP 28R45 MJ	Tix	24-DIC	TTL	-55...+125	<605		20		TTL-TS
TBP 28R45 N	Tix	24-DIP	TTL	0...+70	<577		20		TTL-TS

2864 — 8192x8-Bit EEPROM



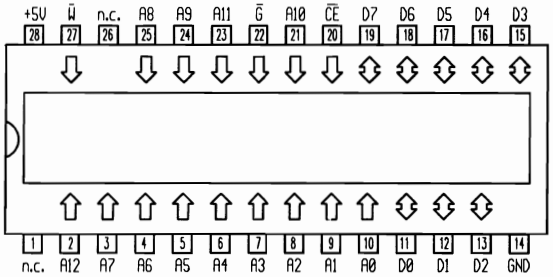
RDY/$\overline{Busy}$ = device ready/busy (open-drain output)

$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Ready/Busy	Power	Mode
L	L	L	data out	Hi-Z	active	read
L	H	⌐⌐	data in	L	active	write
H	X	X	Hi-Z	Hi-Z	standby	standby write inhibit
X	L	X	X	Hi-Z	—	write inhibit
X	X	H	X	Hi-Z	—	write inhibit
L	⌐+15V	L	data in = H	Hi-Z	active	chip erase
L	L	H	D7 = D_{in}7	0	active	data pulling
L	L	H	D7 = D_{in}7	1	active	data pulling

2864 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 58C65 P-20	Hit	28-DIP	CMOS	0...+70	<550	<165	<200		TTL-TS
HN 58C65 P-25	Hit	28-DIP	CMOS	0...+70	<550	<137,5	<250		TTL-TS
HN 58C65 P-30	Hit	28-DIP	CMOS	0...+70	<550	<110	<300		TTL-TS
NMC 98C64A J	Nsc	28-DIC	CMOS	0...+75	<55	<0,55	<250		TTL-TS
TMS 28C64-25 JL	Tix	28-DIC	CMOS	0...+70	<110	<17	<250		TTL-TS
TMS 28C64-25 NL	Tix	28-DIP	CMOS	0...+70	<110	<17	<250		TTL-TS
TMS 28C64-35 JL	Tix	28-DIC	CMOS	0...+70	<110	<17	<350		TTL-TS
TMS 28C64-35 NL	Tix	28-DIP	CMOS	0...+70	<110	<17	<350		TTL-TS

2864 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLM 2865 AC-300	Exl	28-DIC	NMOS	-55...+125	<660	<275	<300		TTL-TS
XLM 2865 AC-350	Exl	28-DIC	NMOS	-55...+125	<660	<275	<350		TTL-TS
XLM 2865 AC-450	Exl	28-DIC	NMOS	-55...+125	<660	<275	<450		TTL-TS
XLS 2865 AC-250	Exl	28-DIC	NMOS	0...+70	<660	<275	<250		TTL-TS
XLS 2865 AC-300	Exl	28-DIC	NMOS	0...+70	<660	<275	<300		TTL-TS
XLS 2865 AC-350	Exl	28-DIC	NMOS	0...+70	<660	<275	<350		TTL-TS
XLS 2865 AC-450	Exl	28-DIC	NMOS	0...+70	<660	<275	<450		TTL-TS
XLS 2865 AP-250	Exl	28-DIP	NMOS	0...+70	<660	<275	<250		TTL-TS
XLS 2865 AP-300	Exl	28-DIP	NMOS	0...+70	<660	<275	<300		TTL-TS
XLS 2865 AP-350	Exl	28-DIP	NMOS	0...+70	<660	<275	<350		TTL-TS
XLS 2865 AP-450	Exl	28-DIP	NMOS	0...+70	<660	<275	<450		TTL-TS

2864 — 8192x8-Bit EEPROM

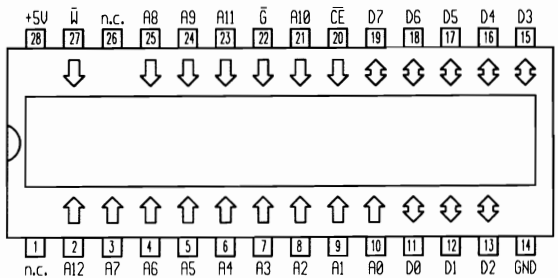


$\overline{W}$	$\overline{CS}$	$\overline{G}$	D_n	Mode
X	H	X	Hi-Z	standby
H	L	H	Hi-Z	output disabled
H	L	L	data out	read
L	L	X	data in	write

2864 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 58064 P-25	Hit	28-DIP	NMOS	0...+70	<550	<137,5	<250		TTL-TS
HN 58064 P-30	Hit	28-DIP	NMOS	0...+70	<550	<137,5	<300		TTL-TS
KM 2864 A-20	Sam	28-DIP	NMOS	0...+70	<660	<275	<200		TTL
KM 2864 A-25	Sam	28-DIP	NMOS	0...+70	<660	<275	<250		TTL
KM 2864 A-30	Sam	28-DIP	NMOS	0...+70	<660	<275	<300		TTL
KM 2864 AH-20	Sam	28-DIP	NMOS	0...+70	<660	<275	<200		TTL
KM 2864 AH-25	Sam	28-DIP	NMOS	0...+70	<660	<275	<250		TTL
KM 2864 AH-30	Sam	28-DIP	NMOS	0...+70	<660	<275	<300		TTL

2864 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 28C64-15	Sam	28-DIP	CMOS	0...+70	<165	<5,5	<150		TTL
KM 28C64-20	Sam	28-DIP	CMOS	0...+70	<165	<5,5	<200		TTL
KM 28C64-25	Sam	28-DIP	CMOS	0...+70	<165	<5,5	<250		TTL

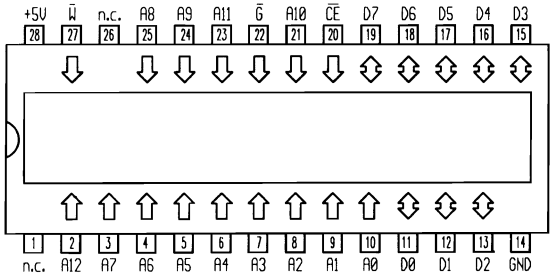
2864 — 8192x8-Bit EEPROM



CE	G	W	D_n	Power	Mode
H	X	X	Hi-Z	standby	standby
L	L	H	data out	active	read
L	H	⊓	data in	active	byte write (W controlled)
⊓	H	L	data in	active	byte write (CE controlled)
L	H	H	Hi-Z	active	read + write inhibit
L	+15V	⊓	D_{in} = H	active	chip erase

2864 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLM 2864 AC-300	Exl	28-DIC	NMOS	-55...+125	<660	<275	<300		TTL-TS
XLM 2864 AC-350	Exl	28-DIC	NMOS	-55...+125	<660	<275	<350		TTL-TS
XLM 2864 AC-450	Exl	28-DIC	NMOS	-55...+125	<660	<275	<450		TTL-TS
XLS 2864 AC-200	Exl	28-DIC	NMOS	0...+70	<660	<275	<200		TTL-TS
XLS 2864 AC-250	Exl	28-DIC	NMOS	0...+70	<660	<275	<250		TTL-TS
XLS 2864 AC-350	Exl	28-DIC	NMOS	0...+70	<660	<275	<350		TTL-TS
XLS 2864 AC-450	Exl	28-DIC	NMOS	0...+70	<660	<275	<450		TTL-TS
XLS 2864 AP-200	Exl	28-DIP	NMOS	0...+70	<660	<275	<200		TTL-TS
XLS 2864 AP-250	Exl	28-DIP	NMOS	0...+70	<660	<275	<250		TTL-TS
XLS 2864 AP-350	Exl	28-DIP	NMOS	0...+70	<660	<275	<350		TTL-TS
XLS 2864 AP-450	Exl	28-DIP	NMOS	0...+70	<660	<275	<450		TTL-TS

2864 — 8192x8-Bit EEPROM

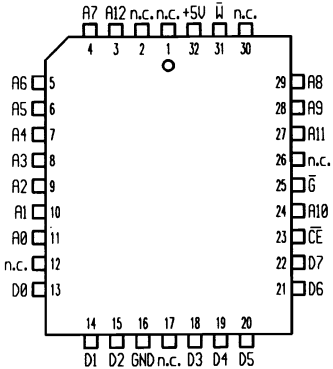


C̄E	Ḡ	W̄	A9	D_n	Mode
L	L	H	X	data out	read
L	X	L	X	data in	write
L	H	H	X	Hi-Z	output disable
H	X	X	X	Hi-Z	standby
L	+12V	L	X	D_{in} = X	chip erase
L	L	H	+12V	data out	electronic signature

2864 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLE 28C64 AC-110	Exl	28-DIC	CMOS	-40…+85	<165	<11	<110		TTL-TS
XLE 28C64 AC-70	Exl	28-DIC	CMOS	-40…+85	<165	<11	<70		TTL-TS
XLE 28C64 AC-90	Exl	28-DIC	CMOS	-40…+85	<165	<11	<90		TTL-TS
XLE 28C64 AP-110	Exl	28-DIP	CMOS	-40…+85	<165	<11	<110		TTL-TS
XLE 28C64 AP-70	Exl	28-DIP	CMOS	-40…+85	<165	<11	<70		TTL-TS
XLE 28C64 AP-90	Exl	28-DIP	CMOS	-40…+85	<165	<11	<90		TTL-TS
XLM 28C64 AC-110	Exl	28-DIC	CMOS	-55…+125	<165	<11	<110		TTL-TS
XLM 28C64 AC-130	Exl	28-DIC	CMOS	-55…+125	<165	<11	<130		TTL-TS

2864 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLM 28C64 AC-90	Exl	28-DIC	CMOS	-55…+125	<165	<11	<90		TTL-TS
XLS 28C64 AC-110	Exl	28-DIC	CMOS	0…+70	<165	<11	<110		TTL-TS
XLS 28C64 AC-70	Exl	28-DIC	CMOS	0…+70	<165	<11	<70		TTL-TS
XLS 28C64 AC-90	Exl	28-DIC	CMOS	0…+70	<165	<11	<90		TTL-TS
XLS 28C64 AP-110	Exl	28-DIP	CMOS	0…+70	<165	<11	<110		TTL-TS
XLS 28C64 AP-70	Exl	28-DIP	CMOS	0…+70	<165	<11	<70		TTL-TS
XLS 28C64 AP-90	Exl	28-DIP	CMOS	0…+70	<165	<11	<90		TTL-TS

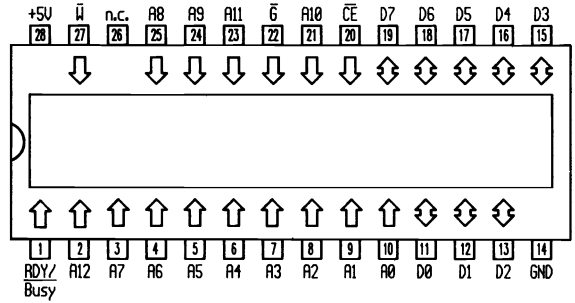
2864 — 8192x8-Bit EEPROM



$\overline{CE}$	$\overline{G}$	$\overline{W}$	A9	D_n	Mode
L	L	H	X	data out	read
L	X	L	X	data in	write
L	H	H	X	Hi-Z	output disable
H	X	X	X	Hi-Z	standby
L	+12V	L	X	D_{in} = X	chip erase
L	L	H	+12V	data out	electronic signature

2864 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLE 28C64 AD-110	Exl	32-PLCC	CMOS	-40…+85	<165	<11	<110		TTL-TS
XLE 28C64 AD-70	Exl	32-PLCC	CMOS	-40…+85	<165	<11	<70		TTL-TS
XLE 28C64 AD-90	Exl	32-PLCC	CMOS	-40…+85	<165	<11	<90		TTL-TS
XLS 28C64 AD-110	Exl	32-PLCC	CMOS	0…+70	<165	<11	<110		TTL-TS
XLS 28C64 AD-70	Exl	32-PLCC	CMOS	0…+70	<165	<11	<70		TTL-TS
XLS 28C64 AD-90	Exl	32-PLCC	CMOS	0…+70	<165	<11	<90		TTL-TS

2865 — 8192x8-Bit EEPROM



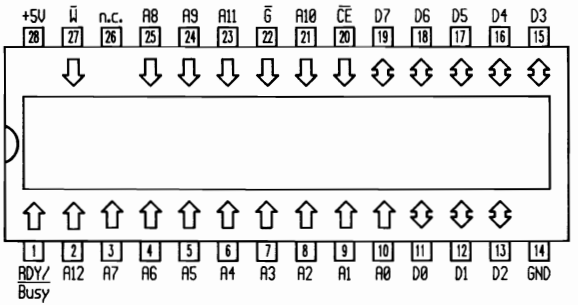
RDY/$\overline{Busy}$ = device ready/busy (open-drain output)

$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	RDY/$\overline{Busy}$	Mode
L	L	H	data out	Hi-Z	read
H	X	X	Hi-Z	Hi-Z	standby
L	H	⊓⊔	data in	L	write
X	X	X	Hi-Z	L	busy

2865 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 2865 A-20	Sam	28-DIP	NMOS	0…+70	<660	<275	<200		TTL
KM 2865 A-25	Sam	28-DIP	NMOS	0…+70	<660	<275	<250		TTL
KM 2865 A-30	Sam	28-DIP	NMOS	0…+70	<660	<275	<300		TTL
KM 2865 AH-20	Sam	28-DIP	NMOS	0…+70	<660	<275	<200		TTL
KM 2865 AH-25	Sam	28-DIP	NMOS	0…+70	<660	<275	<250		TTL
KM 2865 AH-30	Sam	28-DIP	NMOS	0…+70	<660	<275	<300		TTL
KM 28C65-15	Sam	28-DIP	CMOS	0…+70	<165	<5,5	<150		TTL
KM 28C65-20	Sam	28-DIP	CMOS	0…+70	<165	<5,5	<200		TTL

2865 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 28C65-25	Sam	28-DIP	CMOS	0...+70	<165	<5,5	<250		TTL

2865 — 8192x8-Bit EEPROM



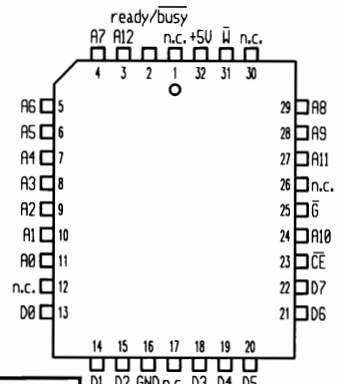
RDY/$\overline{Busy}$ = device ready/busy (open-drain output)

$\overline{CE}$	$\overline{G}$	$\overline{W}$	A9	D_n	Mode
L	L	H	X	data out	read
L	X	L	X	data in	write
L	H	H	X	Hi-Z	output disable
H	X	X	X	Hi-Z	standby
L	+12V	L	X	D_{in} = X	chip erase
L	L	H	+12V	data out	electronic signature

2865 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLE 28C65 AC-110	Exl	28-DIC	CMOS	-40...+85	<165	<11	<110		TTL-TS
XLE 28C65 AC-70	Exl	28-DIC	CMOS	-40...+85	<165	<11	<70		TTL-TS
XLE 28C65 AC-90	Exl	28-DIC	CMOS	-40...+85	<165	<11	<90		TTL-TS
XLE 28C65 AP-110	Exl	28-DIP	CMOS	-40...+85	<165	<11	<110		TTL-TS
XLE 28C65 AP-70	Exl	28-DIP	CMOS	-40...+85	<165	<11	<70		TTL-TS
XLE 28C65 AP-90	Exl	28-DIP	CMOS	-40...+85	<165	<11	<90		TTL-TS
XLM 28C65 AC-110	Exl	28-DIC	CMOS	-55...+125	<165	<11	<110		TTL-TS
XLM 28C65 AC-130	Exl	28-DIC	CMOS	-55...+125	<165	<11	<130		TTL-TS

2865 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLM 28C65 AC-90	Exl	28-DIC	CMOS	-55...+125	<165	<11	<90		TTL-TS
XLS 28C65 AC-110	Exl	28-DIC	CMOS	0...+70	<165	<11	<110		TTL-TS
XLS 28C65 AC-70	Exl	28-DIC	CMOS	0...+70	<165	<11	<70		TTL-TS
XLS 28C65 AC-90	Exl	28-DIC	CMOS	0...+70	<165	<11	<90		TTL-TS
XLS 28C65 AP-110	Exl	28-DIP	CMOS	0...+70	<165	<11	<110		TTL-TS
XLS 28C65 AP-70	Exl	28-DIP	CMOS	0...+70	<165	<11	<70		TTL-TS
XLS 28C65 AP-90	Exl	28-DIP	CMOS	0...+70	<165	<11	<90		TTL-TS

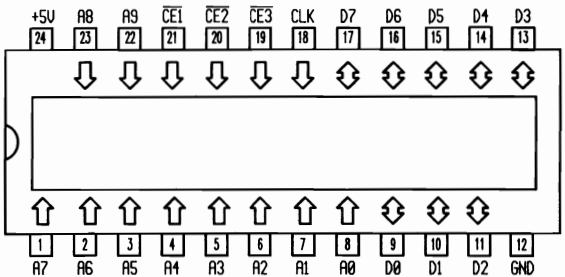
2865 — 8192x8-Bit EEPROM



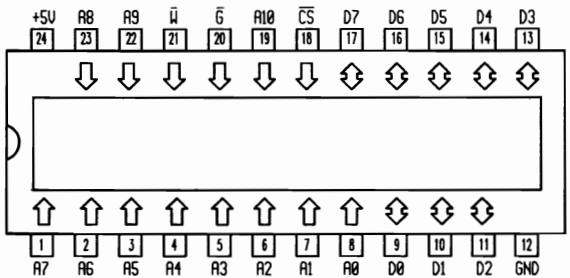
$\overline{CE}$	$\overline{G}$	$\overline{W}$	A9	D_n	Mode
L	L	H	X	data out	read
L	X	L	X	data in	write
L	H	H	X	Hi-Z	output disable
H	X	X	X	Hi-Z	standby
L	+12V	L	X	D_{in} = X	chip erase
L	L	H	+12V	data out	electronic signature

2865 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLE 28C65 AD-110	Exl	32-PLCC	CMOS	-40...+85	<165	<11	<110		TTL-TS
XLE 28C65 AD-70	Exl	32-PLCC	CMOS	-40...+85	<165	<11	<70		TTL-TS
XLE 28C65 AD-90	Exl	32-PLCC	CMOS	-40...+85	<165	<11	<90		TTL-TS
XLS 28C65 AD-110	Exl	32-PLCC	CMOS	0...+70	<165	<11	<110		TTL-TS
XLS 28C65 AD-70	Exl	32-PLCC	CMOS	0...+70	<165	<11	<70		TTL-TS
XLS 28C65 AD-90	Exl	32-PLCC	CMOS	0...+70	<165	<11	<90		TTL-TS

2885 — 1024x8-Bit Register PROM



4016 — 2048x8-Bit static RAM



CS	G	W	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	H	data out	read
L	H	L	data in	write (cycle 1)
L	L	L	data in	write (cycle 2)

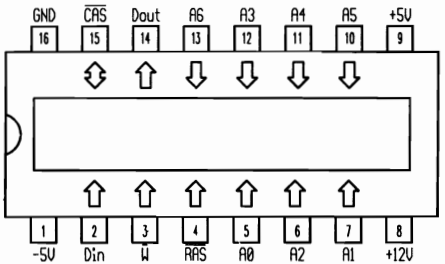
2885 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TBP 28R85 J	Tix	24-TDIC	TTL	0...+70	<630		20		TTL-TS
TBP 28R85 MJ	Tix	24-TDIC	TTL	-55...+125	<660		20		TTL-TS
TBP 28R85 N	Tix	24-TDIP	TTL	0...+70	<630		20		TTL-TS

4016 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9128-10	Amd	24-DIP	NMOS	0...+70	<660		<100		TTL-TS
Am 9128-15	Amd	24-DIP	NMOS	0...+70	<550		<150		TTL-TS
Am 9128-20	Amd	24-DIP	NMOS	0...+70	<770		<200		TTL-TS
Am 9128-70	Amd	24-DIP	NMOS	0...+70	<770		<70		TTL-TS
D 2128-15	Int	24-DIC	NMOS	0...+70	<660		<150		TTL-TS
D 2128-20	Int	24-DIC	NMOS	0...+70	<660		<200		TTL-TS
ET 2128 J-3	Tho	24-DIC	NMOS	0...+70	<550	<82,5	<150		TTL-TS
ET 2128 J-4	Tho	24-DIC	NMOS	0...+70	<550	<82,5	<200		TTL-TS

4016 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
ET 2128 J-5	Tho	24-DIC	NMOS	0...+70	<550	<82,5	<250		TTL-TS
ET 2128 N-3	Tho	24-DIP	NMOS	0...+70	<550	<82,5	<150		TTL-TS
ET 2128 N-4	Tho	24-DIP	NMOS	0...+70	<550	<82,5	<200		TTL-TS
ET 2128 N-5	Tho	24-DIP	NMOS	0...+70	<550	<82,5	<250		TTL-TS
ETL 2128 J-3	Tho	24-DIC	NMOS	0...+70	<385	<55	<150		TTL-TS
ETL 2128 J-4	Tho	24-DIC	NMOS	0...+70	<385	<55	<200		TTL-TS
ETL 2128 J-5	Tho	24-DIC	NMOS	0...+70	<385	<55	<250		TTL-TS
ETL 2128 N-3	Tho	24-DIP	NMOS	0...+70	<385	<55	<150		TTL-TS
ETL 2128 N-4	Tho	24-DIP	NMOS	0...+70	<385	<55	<200		TTL-TS
ETL 2128 N-5	Tho	24-DIP	NMOS	0...+70	<385	<55	<250		TTL-TS
F 3528-25	Fch	24-DIP	NMOS	0...+70	450		<250		TTL-TS
F 3528-35	Fch	24-DIP	NMOS	0...+70	450		<350		TTL-TS
M58725 P	Mit	24-DIP	NMOS	0...+70	<440	<55	<200		TTL-TS
M58725 P-15	Mit	24-DIP	NMOS	0...+70	<440	<55	<150		TTL-TS
M58725 S	Mit	24-DIC	NMOS	0...+70	<440	<55	<200		TTL-TS
M58725 S-15	Mit	24-DIC	NMOS	0...+70	<440	<55	<150		TTL-TS
MB 8128-10	Fui	24-DIP	NMOS	0...+70	<550		<100		TTL-TS
MB 8128-15	Fui	24-DIP	NMOS	0...+70	<385		<150		TTL-TS
MB 8168-55	Fui	24-DIP	NMOS	0...+70	<825		<55		TTL-TS
MB 8168-70	Fui	24-DIP	NMOS	0...+70	<825		<70		TTL-TS
MB 8168-90	Fui	24-DIP	NMOS	0...+70	<825		<90		TTL-TS
MCM 2016 HN-45	Mot	24-TDIP	NMOS	0...+70	<742,5	<110	<45		TTL-TS
MCM 2016 HN-55	Mot	24-TDIP	NMOS	0...+70	<742,5	<110	<55		TTL-TS
MCM 2016 HN-70	Mot	24-TDIP	NMOS	0...+70	<742,5	<110	<70		TTL-TS
MCM 2018 N-35	Mot	24-TDIP	NMOS	0...+70	<742,5	<110	<35		TTL-TS
MCM 2018 N-45	Mot	24-TDIP	NMOS	0...+70	<742,5	<110	<45		TTL-TS
MCM 4016 C-20	Mot	24-DIC	NMOS		400	35	<200		TTL
MCM 4016 L-20	Mot	24-DIC	NMOS		400	35	<200		TTL
MN 4216-20	Mat	24-DIP	NMOS	0...+70	<550		<200		TTL-TS
MN 4216-25	Mat	24-DIP	NMOS	0...+70	<550		<250		TTL-TS
MSM 2128-12 RS	Oki	24-DIP	NMOS	0...+70	<660		<120		TTL-TS
MSM 2128-13 RS	Oki	24-DIP	NMOS	0...+70	<550		<300		TTL-TS
MSM 2128-15 RS	Oki	24-DIP	NMOS	0...+70	<550		<150		TTL-TS
MSM 2128-20 RS	Oki	24-DIP	NMOS	0...+70	<550		<200		TTL-TS
P 2128-15	Int	24-DIP	NMOS	0...+70	<660		<150		TTL-TS
P 2128-20	Int	24-DIP	NMOS	0...+70	<660		<200		TTL-TS
TMM 2016 BP-10	Tos	24-DIP	NMOS	0...+70	<50	<5	<100		TTL-TS

4016 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMM 2016 BP-12	Tos	24-DIP	NMOS	0...+70	<50	<5	<120		TTL-TS
TMM 2016 BP-15	Tos	24-DIP	NMOS	0...+70	<50	<5	<150		TTL-TS
TMM 2016 BP-90	Tos	24-DIP	NMOS	0...+70	<50	<5	<90		TTL-TS
TMM 2016 D	Tos	24-DIC	NMOS	0...+70	<550		<150		TTL-TS
TMM 2016 D-1	Tos	24-DIC	NMOS	0...+70	<660		<100		TTL-TS
TMM 2016 D-2	Tos	24-DIC	NMOS	0...+70	<770		<200		TTL-TS
TMM 2016 P	Tos	24-DIP	NMOS	0...+70	<550		<150		TTL-TS
TMM 2016 P-1	Tos	24-DIP	NMOS	0...+70	<660		<100		TTL-TS
TMM 2016 P-2	Tos	24-DIP	NMOS	0...+70	<770		<200		TTL-TS
TMM 2018 AP-25	Tos	24-TDIP	NMOS	0...+70	<150	<20	<25		TTL-TS
TMM 2018 AP-35	Tos	24-TDIP	NMOS	0...+70	<135	<20	<35		TTL-TS
TMM 2018 AP-45	Tos	24-TDIP	NMOS	0...+70	<135	<20	<45		TTL-TS
TMS 4016-12 NL	Tix	24-DIP	NMOS	0...+70	<385		<120		TTL-TS
TMS 4016-15 NL	Tix	24-DIP	NMOS	0...+70	<385		<150		TTL-TS
TMS 4016-20 NL	Tix	24-DIP	NMOS	0...+70	<385		<200		TTL-TS
TMS 4016-25 NL	Tix	24-DIP	NMOS	0...+70	<385		<250		TTL-TS
µPD 4016 C-1	Nip	24-DIP	NMOS	0...+70	<330	<83	<250		TTL-TS
µPD 4016 C-2	Nip	24-DIP	NMOS	0...+70	<330	<83	<200		TTL-TS
µPD 4016 C-3	Nip	24-DIP	NMOS	0...+70	<330	<83	<150		TTL-TS
µPD 4016 CX-15	Nip	24-DIP	NMOS	0...+70	<330	<83	<150		TTL-TS
µPD 4016 CX-20	Nip	24-DIP	NMOS	0...+70	<330	<83	<200		TTL-TS
µPD 4016 CX-25	Nip	24-DIP	NMOS	0...+70	<330	<83	<250		TTL-TS
µPD 4016 D-1	Nip	24-DIC	NMOS	0...+70	<330	<83	<250		TTL-TS
µPD 4016 D-2	Nip	24-DIC	NMOS	0...+70	<330	<83	<200		TTL-TS
µPD 4016 D-3	Nip	24-DIC	NMOS	0...+70	<330	<83	<150		TTL-TS

4116 — 16384x1-Bit dynamic RAM



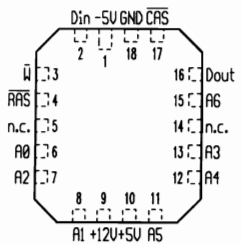
4116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 9016 C	Amd	16-DIP	NMOS	0...+70	<464	<20	<300	<2	TTL-TS
Am 9016 D	Amd	16-DIP	NMOS	0...+70	<464	<20	<250	<2	TTL-TS
Am 9016 E	Amd	16-DIP	NMOS	0...+70	<464	<20	<200	<2	TTL-TS
Am 9016 F	Amd	16-DIP	NMOS	0...+70	<464	<20	<150	<2	TTL-TS
F 4116-2 D	Fch	16-DIC	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
F 4116-2 P	Fch	16-DIP	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
F 4116-3 D	Fch	16-DIC	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
F 4116-3 P	Fch	16-DIP	NMOS	0...+70	<463	<20	<200	<2	TTL-TS

4116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 4116-4 D	Fch	16-DIC	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
F 4116-4 P	Fch	16-DIP	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
HM 4716 A-1	Hit	16-DIC	NMOS	0...+70	350	<20	<120	2	TTL-TS
HM 4716 A-2	Hit	16-DIC	NMOS	0...+70	350	<20	<150	2	TTL-TS
HM 4716 A-3	Hit	16-DIC	NMOS	0...+70	350	<20	<200	2	TTL-TS
HM 4716 A-4	Hit	16-DIC	NMOS	0...+70	350	<20	<250	2	TTL-TS
HM 4716 AP-1	Hit	16-DIP	NMOS	0...+70	350	<20	<120	2	TTL-TS
HM 4716 AP-2	Hit	16-DIP	NMOS	0...+70	350	<20	<150	2	TTL-TS
HM 4716 AP-3	Hit	16-DIP	NMOS	0...+70	350	<20	<200	2	TTL-TS
HM 4716 AP-4	Hit	16-DIP	NMOS	0...+70	350	<20	<250	2	TTL-TS
HYB 4116-P2	Sie	16-DIP	NMOS	0...+70	<462	<18	<150	<2	TTL-TS
HYB 4116-P3	Sie	16-DIP	NMOS	0...+70	<462	<18	<200	<2	TTL-TS
IM 4116-2 D	Isi	16-DIC	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
IM 4116-2 J	Isi	16-DIC	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
IM 4116-2 P	Isi	16-DIP	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
IM 4116-3 D	Isi	16-DIC	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
IM 4116-3 J	Isi	16-DIC	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
IM 4116-3 P	Isi	16-DIP	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
IM 4116-4 D	Isi	16-DIC	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
IM 4116-4 J	Isi	16-DIC	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
IM 4116-4 P	Isi	16-DIP	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
LH 6116-3	Sha	16-DIP	NMOS	0...+70	<442	<19,5	<200	<2	TTL-TS
LH 6116-4	Sha	16-DIP	NMOS	0...+70	<442	<19,5	<250	<2	TTL-TS
LH 6116-5	Sha	16-DIP	NMOS	0...+70	<442	<19,5	<300	<2	TTL-TS
M 58759-15	Mit	16-DIP	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
M 58759-20	Mit	16-DIP	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
M 58759-25	Mit	16-DIP	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
M5K4116 P-2	Mit	16-DIP	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
M5K4116 P-3	Mit	16-DIP	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
M5K4116 S-2	Mit	16-DIC	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
M5K4116 S-3	Mit	16-DIC	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
MB 8116 E	Fui	16-DIP	NMOS	0...+70	<443	<19	<200	<2	TTL-TS
MB 8116 H	Fui	16-DIP	NMOS	0...+70	<443	<19	<150	<2	TTL-TS
MB 8216 E	Fui	16-DIP	NMOS	0...+70	<443	<19	<120	<2	TTL-TS
MB 8216 N	Fui	16-DIP	NMOS	0...+70	<443	<19	<250	<2	TTL-TS
MCM 4116 BC-15	Mot	16-DIC	NMOS	0...+70	463	<20	<150	<2	TTL-TS
MCM 4116 BC-20	Mot	16-DIC	NMOS	0...+70	463	<20	<200	<2	TTL-TS

4116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 4116 BC-25	Mot	16-DIC	NMOS	0...+70	463	<20	<250	<2	TTL-TS
MCM 4116 BC-30	Mot	16-DIC	NMOS	0...+70	463	<20	<300	<2	TTL-TS
MCM 4116 BP-15	Mot	16-DIP	NMOS	0...+70	463	<20	<150	<2	TTL-TS
MCM 4116 BP-20	Mot	16-DIP	NMOS	0...+70	463	<20	<200	<2	TTL-TS
MCM 4116 BP-25	Mot	16-DIP	NMOS	0...+70	463	<20	<250	<2	TTL-TS
MCM 4116 BP-30	Mot	16-DIP	NMOS	0...+70	463	<20	<300	<2	TTL-TS
MCM 6616-3 L	Mot	16-DIC	NMOS	0...+70	<595	<26,4	<200	<2	TTL-TS
MCM 6616-3 P	Mot	16-DIP	NMOS	0...+70	<595	<26,4	<200	<2	TTL-TS
MCM 6616-4 L	Mot	16-DIC	NMOS	0...+70	<595	<26,4	<250	<2	TTL-TS
MCM 6616-4 P	Mot	16-DIP	NMOS	0...+70	<595	<26,4	<250	<2	TTL-TS
MCM 6616-5 L	Mot	16-DIC	NMOS	0...+70	<595	<26,4	<300	<2	TTL-TS
MCM 6616-5 P	Mot	16-DIP	NMOS	0...+70	<595	<26,4	<300	<2	TTL-TS
MCM 6616 L	Mot	16-DIC	NMOS	0...+70			<350	<2	TTL-TS
MK 4116 J-2	Mos	16-DIC	NMOS	0...+70	<462	<20	<150	<2	TTL-TS
MK 4116 J-3	Mos	16-DIC	NMOS	0...+70	<462	<20	<200	<2	TTL-TS
MK 4116 J-4	Mos	16-DIC	NMOS	0...+70	<462	<20	<250	<2	TTL-TS
MK 4116 N-2	Mos	16-DIP	NMOS	0...+70	<462	<20	<150	<2	TTL-TS
MK 4116 N-3	Mos	16-DIP	NMOS	0...+70	<462	<20	<200	<2	TTL-TS
MK 4116 N-4	Mos	16-DIP	NMOS	0...+70	<462	<20	<250	<2	TTL-TS
MKB 4116 J-2	Mos	16-DIC	NMOS	0...+70	<462	<20	<150	<2	TTL-TS
MKB 4116 J-3	Mos	16-DIC	NMOS	0...+70	<462	<20	<200	<2	TTL-TS
MKB 4116 J-4	Mos	16-DIC	NMOS	0...+70	<462	<20	<250	<2	TTL-TS
MKB 4116 J-82	Tho	16-DIC	NMOS	-55...+110	<462	<30	<150	<2	TTL-TS
MKB 4116 J-83	Mos	16-DIC	NMOS	-55...+85	<462	<30	<200	<2	TTL-TS
MKB 4116 J-83	Tho	16-DIC	NMOS	-55...+110	<462	<30	<200	<2	TTL-TS
MKB 4116 J-84	Mos	16-DIC	NMOS	-55...+85	<462	<30	<250	<2	TTL-TS
MKB 4116 J-84	Tho	16-DIC	NMOS	-55...+110	<462	<30	<250	<2	TTL-TS
MKB 4116 J-93	Mos	16-DIC	NMOS	-55...+85	<462	<30	<200	<1	TTL-TS
MKB 4116 P-82	Tho	16-DIP	NMOS	-55...+110	<462	<30	<150	<2	TTL-TS
MKB 4116 P-83	Mos	16-DIP	NMOS	-55...+85	<462	<30	<200	<2	TTL-TS
MKB 4116 P-83	Tho	16-DIP	NMOS	-55...+110	<462	<30	<200	<2	TTL-TS
MKB 4116 P-84	Mos	16-DIP	NMOS	-55...+85	<462	<30	<250	<2	TTL-TS
MKB 4116 P-84	Tho	16-DIP	NMOS	-55...+110	<462	<30	<250	<2	TTL-TS
MKB 4116 P-93	Mos	16-DIP	NMOS	-55...+85	<462	<30	<200	<1	TTL-TS
MM 5290-2	Nsc	16-DIP	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
MM 5290-2 J	Nsc	16-DIC	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
MM 5290-3	Nsc	16-DIP	NMOS	0...+70	<463	<20	<200	<2	TTL-TS

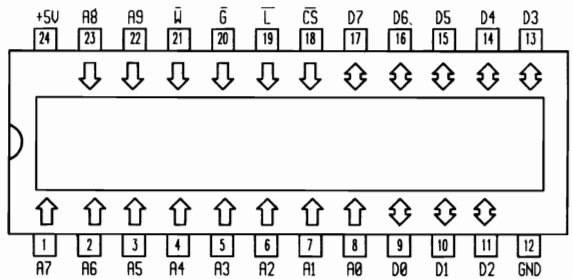
4116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MM 5290-3 J	Nsc	16-DIC	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
MM 5290-4	Nsc	16-DIP	NMOS	0...+70	<463	<20	<300	<2	TTL-TS
MM 5290-4 J	Nsc	16-DIC	NMOS	0...+70	<463	<20	<300	<2	TTL-TS
MSM 3716-2 AS	Oki	16-DIP	NMOS		<528		<150		TTL-TS
MSM 3716-3 AS	Oki	16-DIP	NMOS		<528		<200		TTL-TS
N 2690-2	Sig	16-DIP	NMOS	0...+70			<150	<2	TTL-TS
N 2690-3	Sig	16-DIP	NMOS	0...+70			<200	<2	TTL-TS
N 2690-4	Sig	16-DIP	NMOS	0...+70			<250	<2	TTL-TS
TMM 416 C-3	Tos	16-DIC	NMOS	0...+70	<464	<20	<200	<2	TTL-TS
TMM 416 C-4	Tos	16-DIC	NMOS	0...+70	<464	<20	<250	<2	TTL-TS
TMM 416 D-2	Tos	16-DIC	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
TMM 416 D-3	Tos	16-DIC	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
TMM 416 D-4	Tos	16-DIC	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
TMM 416 P-2	Tos	16-DIP	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
TMM 416 P-3	Tos	16-DIP	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
TMM 416 P-4	Tos	16-DIP	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
TMS 4070-1 JL	Tix	16-DIC	NMOS	0...+70	<980	<19	<300	<2	TTL-TS
TMS 4070-1 N	Tix	16-DIP	NMOS	0...+70	<980	<19	<300	<2	TTL-TS
TMS 4070-2 JL	Tix	16-DIC	NMOS	0...+70	<980	<19	<250	<2	TTL-TS
TMS 4070-2 N	Tix	16-DIP	NMOS	0...+70	<980	<19	<250	<2	TTL-TS
TMS 4070 JL	Tix	16-DIC	NMOS	0...+70	<980	<19	<350	<2	TTL-TS
TMS 4070 N	Tix	16-DIP	NMOS	0...+70	<980	<19	<350	<2	TTL-TS
TMS 4116-15 NL	Tix	16-DIP	NMOS	0...+70	<463	<20	<150	<2	TTL-TS
TMS 4116-20 NL	Tix	16-DIP	NMOS	0...+70	<463	<20	<200	<2	TTL-TS
TMS 4116-25 NL	Tix	16-DIP	NMOS	0...+70	<463	<20	<250	<2	TTL-TS
2117-2	Int	16-DIP	NMOS	0...+70	<464	<40	<150	<2	TTL-TS
2117-3	Int	16-DIP	NMOS	0...+70	<464	<40	<200	<2	TTL-TS
2117-4	Int	16-DIP	NMOS	0...+70	<464	<40	<250	<2	TTL-TS
µPD 416 C	Nip	16-DIP	NMOS	0...+75	462	20	<300		TTL-TS
µPD 416 C-1	Nip	16-DIP	NMOS	0...+75	462	20	<250		TTL-TS
µPD 416 C-2	Nip	16-DIP	NMOS	0...+75	462	20	<200		TTL-TS
µPD 416 C-3	Nip	16-DIP	NMOS	0...+75	462	20	<150		TTL-TS
µPD 416 D	Nip	16-DIC	NMOS	0...+75	462	20	<300		TTL-TS
µPD 416 D-1	Nip	16-DIC	NMOS	0...+75	462	20	<250		TTL-TS
µPD 416 D-2	Nip	16-DIC	NMOS	0...+75	462	20	<200		TTL-TS
µPD 416 D-3	Nip	16-DIC	NMOS	0...+75	462	20	<150		TTL-TS

4116 — 16384x1-Bit dynamic RAM



4116 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MKB 4116 E-82	Tho	18-LCC	NMOS	-55...+110	<462	<30	<150	<2	TTL-TS
MKB 4116 E-83	Tho	18-LCC	NMOS	-55...+110	<462	<30	<200	<2	TTL-TS
MKB 4116 E-84	Tho	18-LCC	NMOS	-55...+110	<462	<30	<250	<2	TTL-TS

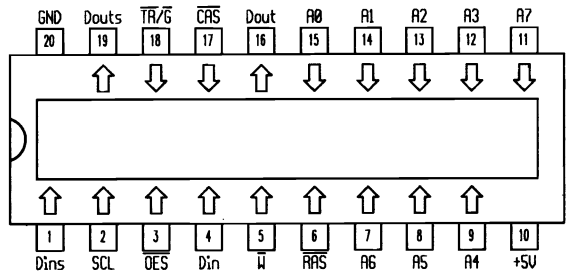
4118 — 1024x8-Bit static RAM



4118 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4118 N-1	Mos	24-DIP	NMOS	0...+70	<400	<300	<120		TTL-TS
MK 4118 N-2	Mos	24-DIP	NMOS	0...+70	<400	<300	<150		TTL-TS
MK 4118 N-3	Mos	24-DIP	NMOS	0...+70	<400	<300	<200		TTL-TS
MK 4118 N-4	Mos	24-DIP	NMOS	0...+70	<400	<300	<250		TTL-TS
MK 4118 P-1	Mos	24-DIC	NMOS	0...+70	<400	<300	<120		TTL-TS
MK 4118 P-2	Mos	24-DIC	NMOS	0...+70	<400	<300	<150		TTL-TS
MK 4118 P-3	Mos	24-DIC	NMOS	0...+70	<400	<300	<200		TTL-TS
MK 4118 P-4	Mos	24-DIC	NMOS	0...+70	<400	<300	<250		TTL-TS

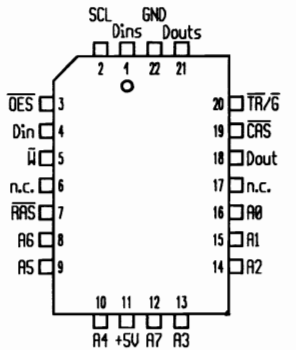
4118 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4801 P-55	Mos	24-DIC	NMOS	0...+70	<625	<475	<55		TTL-TS
MK 4801 P-70	Mos	24-DIC	NMOS	0...+70	<625	<475	<70		TTL-TS
MK 4801 P-90	Mos	24-DIC	NMOS	0...+70	<625	<475	<90		TTL-TS
MKB 4118 N-2	Mos	24-DIP	NMOS	0...+70	<400	<300	<150		TTL-TS
MKB 4118 N-3	Mos	24-DIP	NMOS	0...+70	<400	<300	<200		TTL-TS
MKB 4118 N-4	Mos	24-DIP	NMOS	0...+70	<400	<300	<250		TTL-TS
MKB 4118 P-2	Mos	24-DIC	NMOS	0...+70	<400	<300	<150		TTL-TS
MKB 4118 P-3	Mos	24-DIC	NMOS	0...+70	<400	<300	<200		TTL-TS
MKB 4118 P-4	Mos	24-DIC	NMOS	0...+70	<400	<300	<250		TTL-TS

4161 — 65536x1-Bit Multiport Video RAM

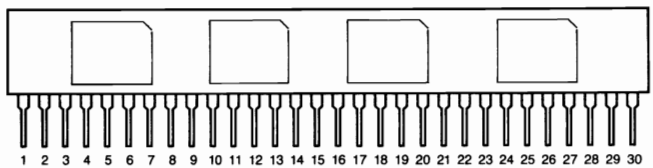


4161 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SMJ 4161-15 JD	Tix	20-DIC	NMOS	-55...+100	<550	<137,5	<150	<4	TTL-TS
SMJ 4161-20 JD	Tix	20-DIC	NMOS	-55...+100	<550	<137,5	<200	<4	TTL-TS
TMS 4161-15 NL	Tix	20-DIP	NMOS	0...+70	<385	<110	<150	<4	TTL-TS
TMS 4161-20 NL	Tix	20-DIP	NMOS	0...+70	<385	<110	<200	<4	TTL-TS

4161 — 65536x1-Bit Multiport Video RAM



4161 — 65536x4-Bit dynamic RAM-Modul

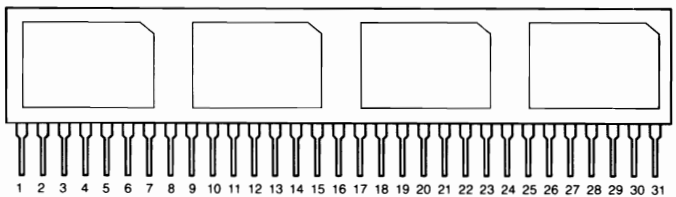


1 = +5V	9 = GND	17 = Ds2	25 = $\overline{W}$
2 = $\overline{OES}$	10 = $\overline{TR/G}$	18 = D2	26 = Ds3
3 = Ds0	11 = Ds1	19 = $\overline{CAS3}$	27 = D3
4 = D0	12 = D1	20 = A5	28 = $\overline{CAS4}$
5 = $\overline{CAS1}$	13 = $\overline{CAS2}$	21 = A6	29 = SCL
6 = A0	14 = A3	22 = GND	30 = +5V
7 = A1	15 = A4	23 = A7	
8 = A2	16 = n.c.	24 = $\overline{RAS}$	

4161 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4161-15 FML	Tix	22-PLCC	NMOS	0...+70	<385	<110	<150	<4	TTL-TS
TMS 4161-20 FML	Tix	22-PLCC	NMOS	0...+70	<385	<110	<200	<4	TTL-TS

4161 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4161 GW 4-15 L	Tix	30-SIP	CMOS	0...+70	1000	256	<150	<4	TTL-TS
TM 4161 GW 4-20 L	Tix	30-SIP	CMOS	0...+70	1000	256	<200	<4	TTL-TS
TM 4161 GY 4-15 L	Tix	30-SIP	CMOS	0...+70	1000	256	<150	<4	TTL-TS
TM 4161 GY 4-20 L	Tix	30-SIP	CMOS	0...+70	1000	256	<200	<4	TTL-TS

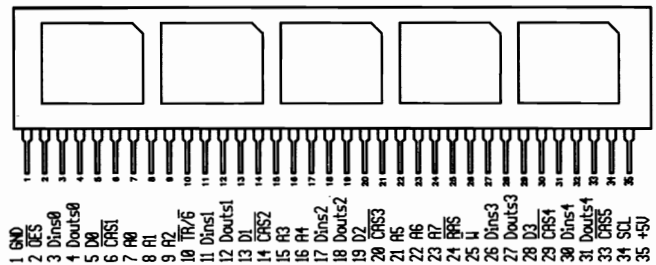
4161 — 65536x4-Bit dynamic RAM-Modul



1 = GND	9 = A2	17 = Dins2	25 = $\overline{W}$
2 = $\overline{OES}$	10 = $\overline{TR/G}$	18 = Douts2	26 = Dins3
3 = Dins0	11 = Dins1	19 = D2	27 = Douts3
4 = Douts0	12 = Douts1	20 = $\overline{CAS3}$	28 = D3
5 = D0	13 = D1	21 = A5	29 = $\overline{CAS4}$
6 = $\overline{CAS1}$	14 = $\overline{CAS2}$	22 = A6	30 = SCL
7 = A0	15 = A3	23 = A7	31 = +5V
8 = A1	16 = A4	24 = $\overline{RAS}$	

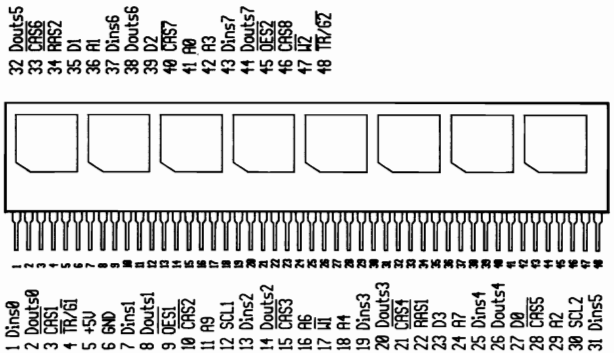
4161 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4161 EV 4-15 L	Tix	31-SIP	CMOS	0...+70	800	320	<150	<4	TTL-TS
TM 4161 EV 4-20 L	Tix	31-SIP	CMOS	0...+70	700	280	<200	<4	TTL-TS

4161 — 65536x5-Bit dynamic RAM-Modul



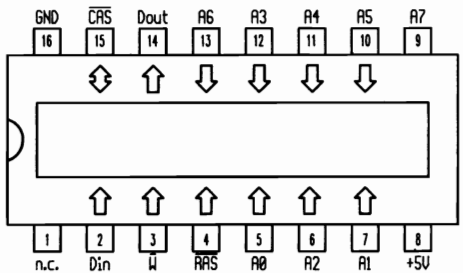
4161 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4161 EP 5-15 L	Tix	35-SIP	CMOS	0...+70	1000	400	<150	<4	TTL-TS
TM 4161 EP 5-20 L	Tix	35-SIP	CMOS	0...+70	875	350	<200	<4	TTL-TS

4161 — 131072x4-Bit dynamic RAM-Modul



4161 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4161 SE 8-15 L	Tix	48-SIP	CMOS	0...+70	1320	640	<150	<4	TTL-TS
TM 4161 SE 8-20 L	Tix	48-SIP	CMOS	0...+70	1180	560	<200	<4	TTL-TS

4164 — 65536x1-Bit dynamic RAM

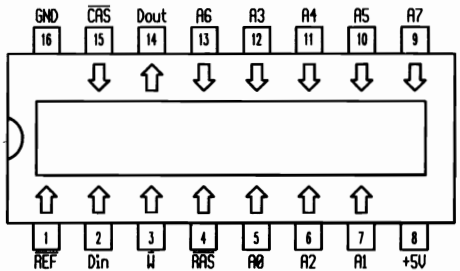


4164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
C 2164-15	Int	16-DIC	NMOS	0...+70	<275	<38,5	<150	<2	TTL-TS
C 2164-20	Int	16-DIC	NMOS	0...+70	<275	<38,5	<200	<2	TTL-TS
C 2164-25	Int	16-DIC	NMOS	0...+70	<275	<38,5	<250	<2	TTL-TS
C 2164 A-15	Int	16-DIP	NMOS	0...+70	<302	<27,5	<150	<2	TTL-TS
C 2164 A-20	Int	16-DIP	NMOS	0...+70	<247	<27,5	<200	<2	TTL-TS
F 4164-1	Fch	16-DIC	NMOS	0...+70	<209	<19,25	<120	<4	TTL-TS
F 4164-2	Fch	16-DIC	NMOS	0...+70	<209	<19,25	<150	<4	TTL-TS
F 4164-3	Fch	16-DIC	NMOS	0...+70	<209	<19,25	<200	<4	TTL-TS
HM 4864-2	Hit	16-DIC	NMOS	0...+70	330	<20	<150	<2	TTL-TS
HM 4864-3	Hit	16-DIC	NMOS	0...+70	330	<20	<200	<2	TTL-TS
HM 4864 A-12	Hit	16-DIC	NMOS	0...+70	275	<20	<120	<2	TTL-TS
HM 4864 A-15	Hit	16-DIC	NMOS	0...+70	275	<20	<150	<2	TTL-TS
HM 4864 A-20	Hit	16-DIC	NMOS	0...+70	275	<20	<200	<2	TTL-TS

4164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 4864 AP-12	Hit	16-DIP	NMOS	0...+70	275	<20	<120	<2	TTL-TS
HM 4864 AP-15	Hit	16-DIP	NMOS	0...+70	275	<20	<150	<2	TTL-TS
HM 4864 AP-20	Hit	16-DIP	NMOS	0...+70	275	<20	<200	<2	TTL-TS
HM 4864 P-2	Hit	16-DIP	NMOS	0...+70	330	<20	<150	<2	TTL-TS
HM 4864 P-3	Hit	16-DIP	NMOS	0...+70	330	<20	<200	<2	TTL-TS
KM 4164 B-10	Sam	16-DIP	NMOS	0...+70	<330	<22	<100	<2	TTL-TS
KM 4164 B-12	Sam	16-DIP	NMOS	0...+70	<110	<22	<120	<2	TTL-TS
KM 4164 B-15	Sam	16-DIP	NMOS	0...+70	<247,5	<22	<150	<2	TTL-TS
M5K4164 ANP-10	Mit	16-DIP	NMOS	0...+70	<247,5	<22	<100	<2	TTL-TS
M5K4164 ANP-12	Mit	16-DIP	NMOS	0...+70	<220	<22	<120	<2	TTL-TS
M5K4164 ANP-15	Mit	16-DIP	NMOS	0...+70	<220	<22	<150	<2	TTL-TS
M5K4164 NP-15	Mit	16-DIP	NMOS	0...+70	<220	<22	<150	<2	TTL-TS
M5K4164 NP-20	Mit	16-DIP	NMOS	0...+70	<192,5	<22	<200	<2	TTL-TS
M5K4164 NS-15	Mit	16-DIC	NMOS	0...+70	<275	<27,5	<150	<2	TTL-TS
M5K4164 NS-20	Mit	16-DIC	NMOS	0...+70	<275	<27,5	<200	<2	TTL-TS
M5M4164 NP-12	Mit	16-DIP	NMOS	0...+70	<242	<33	<120	<2	TTL-TS
MB 8264-15	Fui	16-DIC	NMOS	0...+70	<302	<27,5	<150	<2	TTL-TS
MB 8264-20	Fui	16-DIC	NMOS	0...+70	<302	<27,5	<200	<2	TTL-TS
MB 8264 A-10	Fui	16-DIC	NMOS	0...+70	<330	<22	<100	<2	TTL-TS
MB 8264 A-12	Fui	16-DIC	NMOS	0...+70	<330	<22	<120	<2	TTL-TS
MCM 6665-15	Mot	16-DIC	NMOS	0...+70	<275	<30	<150	<2	TTL-TS
MCM 6665-20	Mot	16-DIC	NMOS	0...+70	<275	<30	<200	<2	TTL-TS
MCM 6665 L25	Mot	16-DIC	NMOS	0...+70	<275	<30	<250	<2	TTL-TS
MKB 4564 P-82	Tho	16-DIP	NMOS	-55...+110	<330	<27,5	<150	<2	TTL-TS
MKB 4564 P-83	Tho	16-DIP	NMOS	-55...+110	<330	<27,5	<200	<2	TTL-TS
MN 4164 P-12 A	Mat	16-DIP	NMOS	0...+70	<275	<27,5	<120	<2	TTL-TS
MN 4164 P-15	Mat	16-DIP	NMOS	0...+70	<275	<27,5	<150	<2	TTL-TS
MN 4164 P-15 A	Mat	16-DIP	NMOS	0...+70	<275	<27,5	<150	<2	TTL-TS
MN 4164 P-20	Mat	16-DIP	NMOS	0...+70	<275	<27,5	<200	<2	TTL-TS
MN 4164 P-25	Mat	16-DIP	NMOS	0...+70	<275	<27,5	<250	<2	TTL-TS
MSM 3764-12 AS	Oki	16-DIP	NMOS	0...+70	<247	<34,6	<120	<2	TTL-TS
MSM 3764-15 AS	Oki	16-DIP	NMOS	0...+70	<247	<29,7	<150	<2	TTL-TS
MSM 3764-20 AS	Oki	16-DIP	NMOS	0...+70	<247	<29,7	<200	<2	TTL-TS
NMC 3764-12 N	Nsc	16-DIP	NMOS	0...+70	<248	<26	<120	<2	TTL-TS
NMC 3764-15 N	Nsc	16-DIP	NMOS	0...+70	<248	<26	<150	<2	TTL-TS
NMC 3764-20 N	Nsc	16-DIP	NMOS	0...+70	<248	<26	<200	<2	TTL-TS
NSC 4164-1	Nsc	16-DIP	NMOS	0...+70	<247	<22	<120	<4	TTL-TS

4164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NSC 4164-2	Nsc	16-DIP	NMOS	0...+70	<247	<22	<150	<4	TTL-TS
SMJ 4164-12 JDL	Tix	16-DIC	NMOS	0...+70	<264	<27,5	<120	<4	TTL-TS
SMJ 4164-12 JDS	Tix	16-DIC	NMOS	-55...+110	<264	<27,5	<120	<4	TTL-TS
SMJ 4164-15 JDL	Tix	16-DIC	NMOS	0...+70	<247,5	<27,5	<150	<4	TTL-TS
SMJ 4164-15 JDS	Tix	16-DIC	NMOS	-55...+110	<247,5	<27,5	<150	<4	TTL-TS
SMJ 4164-20 JDL	Tix	16-DIC	NMOS	0...+70	<203,5	<27,5	<200	<4	TTL-TS
SMJ 4164-20 JDS	Tix	16-DIC	NMOS	-55...+110	<203,5	<27,5	<200	<4	TTL-TS
TMM 4164 C-3	Tos	16-DIC	NMOS	0...+70	<275	<27,5	<150	<2	TTL-TS
TMM 4164 C-4	Tos	16-DIC	NMOS	0...+70	<275	<27,5	<200	<2	TTL-TS
TMS 4164-12 JDL	Tix	16-DIC	NMOS	0...+70	<203	<27,5	<120	<4	TTL-TS
TMS 4164-12 NL	Tix	16-DIP	NMOS	0...+70	<203	<27,5	<120	<4	TTL-TS
TMS 4164-15 JDL	Tix	16-DIC	NMOS	0...+70	<203	<27,5	<150	<4	TTL-TS
TMS 4164-15 NL	Tix	16-DIP	NMOS	0...+70	<203	<27,5	<150	<4	TTL-TS
TMS 4164-20 JDL	Tix	16-DIC	NMOS	0...+70	<203	<27,5	<200	<4	TTL-TS
TMS 4164-20 NL	Tix	16-DIP	NMOS	0...+70	<203	<27,5	<200	<4	TTL-TS
TMS 4164-25 JDL	Tix	16-DIC	NMOS	0...+70	<203	<27,5	<250	<4	TTL-TS
TMS 4164-25 NL	Tix	16-DIP	NMOS	0...+70	<203	<27,5	<250	<4	TTL-TS
2164-5	Int	16-DIC	NMOS	0...+70	<368	<44	<150	<2	TTL-TS
2164-6	Int	16-DIC	NMOS	0...+70	<330	<44	<200	<2	TTL-TS
µPD 4164 C-1	Nip	16-DIP	NMOS	0...+70	<250	28	<250	<2	TTL-TS
µPD 4164 C-12	Nip	16-DIP	NMOS	0...+70	<303	28	<120	<2	TTL-TS
µPD 4164 C-15	Nip	16-DIP	NMOS	0...+70	<275	28	<150	<2	TTL-TS
µPD 4164 C-2	Nip	16-DIP	NMOS	0...+70	<275	28	<200	<2	TTL-TS
µPD 4164 C-20	Nip	16-DIP	NMOS	0...+70	<250	28	<200	<2	TTL-TS
µPD 4164 C-3	Nip	16-DIP	NMOS	0...+70	<330	28	<150	<2	TTL-TS
µPD 4164 D-1	Nip	16-DIC	NMOS	0...+70	<250	28	<250	<2	TTL-TS
µPD 4164 D-12	Nip	16-DIC	NMOS	0...+70	<303	28	<120	<2	TTL-TS
µPD 4164 D-15	Nip	16-DIC	NMOS	0...+70	<275	28	<150	<2	TTL-TS
µPD 4164 D-2	Nip	16-DIC	NMOS	0...+70	<275	28	<200	<2	TTL-TS
µPD 4164 D-20	Nip	16-DIC	NMOS	0...+70	<250	28	<200	<2	TTL-TS
µPD 4164 D-3	Nip	16-DIC	NMOS	0...+70	<330	28	<150	<2	TTL-TS
µPD 4164 G-15	Nip	16-FLAT	NMOS	0...+70	<275	28	<150	<2	TTL-TS
µPD 4164 G-20	Nip	16-FLAT	NMOS	0...+70	<250	28	<200	<2	TTL-TS

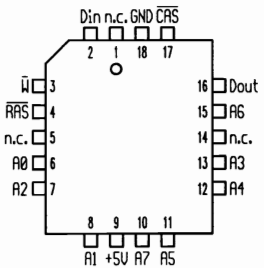
4164 — 65536x1-Bit dynamic RAM



4164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5K4164 S-15	Mit	16-DIC	NMOS	0...+70			<150	<2	TTL-TS
M5K4164 S-20	Mit	16-DIC	NMOS	0...+70			<200	<2	TTL-TS
M5M4164 P-12	Mit	16-DIP	NMOS	0...+70	<242	<33	<120	<2	TTL-TS
MB 8265-15	Fui	16-DIP	NMOS	0...+70	<275	<27,5	<150	<2	TTL-TS
MB 8265-20	Fui	16-DIP	NMOS	0...+70	<247	<27,5	<200	<2	TTL-TS
MB 8265 A-10	Fui	16-DIP	NMOS	0...+70	<330	<25	<100	<2	TTL-TS
MB 8265 A-12	Fui	16-DIP	NMOS	0...+70	<300	<25	<120	<2	TTL-TS
MB 8266 A-10	Fui	16-DIP	NMOS	0...+70	<330	<25	<100	<2	TTL-TS
MB 8266 A-12	Fui	16-DIP	NMOS	0...+70	<300	<25	<120	<2	TTL-TS
MCM 6664-15	Mot	16-DIC	NMOS	0...+70	<275	<30	<150	<2	TTL-TS
MCM 6664-20	Mot	16-DIC	NMOS	0...+70	<275	<30	<200	<2	TTL-TS
MK 4164 J-12	Mos	16-DIC	NMOS	0...+70	200	10	<120	<2	TTL-TS
MK 4164 N-12	Mos	16-DIP	NMOS	0...+70	200	10	<120	<2	TTL-TS

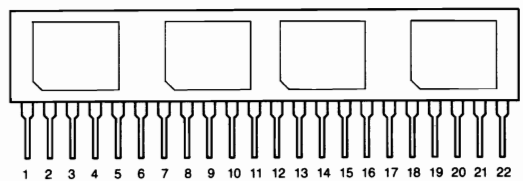
4164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 4865 AP-12	Hit	16-DIP	NMOS	0...+70	<275	<30,25	<120	<2	TTL-TS
HM 4865 AP-15	Hit	16-DIP	NMOS	0...+70	<275	<30,25	<150	<2	TTL-TS
HM 4865 AP-20	Hit	16-DIP	NMOS	0...+70	<275	<30,25	<200	<2	TTL-TS
M5K4164 AP-10	Mit	16-DIP	NMOS	0...+70	<247,5	<22	<100	<2	TTL-TS
M5K4164 AP-12	Mit	16-DIP	NMOS	0...+70	<220	<22	<120	<2	TTL-TS
M5K4164 AP-15	Mit	16-DIP	NMOS	0...+70	<192,5	<22	<150	<2	TTL-TS
M5K4164 P-15	Mit	16-DIP	NMOS	0...+70	<220	<22	<150	<2	TTL-TS
M5K4164 P-20	Mit	16-DIP	NMOS	0...+70	<192,5	<22	<200	<2	TTL-TS

4164 — 65536x1-Bit dynamic RAM



4164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MKB 4564 E-82	Tho	18-LCC	NMOS	-55...+110	<330	<27,5	<150	<2	TTL-TS
MKB 4564 E-83	Tho	18-LCC	NMOS	-55...+110	<330	<27,5	<200	<2	TTL-TS
SMJ 4164-12 FGL	Tix	18-LCC	NMOS	0...+70	<264	<27,5	<120	<4	TTL-TS
SMJ 4164-12 FGS	Tix	18-LCC	NMOS	-55...+110	<264	<27,5	<120	<4	TTL-TS
SMJ 4164-15 FGL	Tix	18-LCC	NMOS	0...+70	<247,5	<27,5	<150	<4	TTL-TS
SMJ 4164-15 FGS	Tix	18-LCC	NMOS	-55...+110	<247,5	<27,5	<150	<4	TTL-TS
SMJ 4164-20 FGL	Tix	18-LCC	NMOS	0...+70	<203,5	<27,5	<200	<4	TTL-TS
SMJ 4164-20 FGS	Tix	18-LCC	NMOS	-55...+110	<203,5	<27,5	<200	<4	TTL-TS
TMS 4164-12 FPL	Tix	18-PLCC	NMOS	0...+70	<203	<27,5	<120	<4	TTL-TS
TMS 4164-15 FPL	Tix	18-PLCC	NMOS	0...+70	<203	<27,5	<150	<4	TTL-TS
TMS 4164-20 FPL	Tix	18-PLCC	NMOS	0...+70	<203	<27,5	<200	<4	TTL-TS
TMS 4164-25 FPL	Tix	18-PLCC	NMOS	0...+70	<203	<27,5	<250	<4	TTL-TS

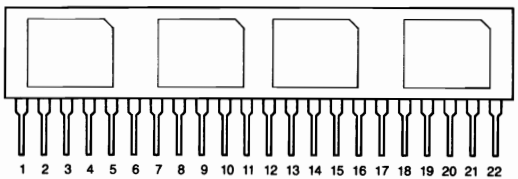
4164 — 262144x1-Bit dynamic RAM-Modul



1 = GND	7 = Din	13 = $\overline{CAS}$	19 = $\overline{RAS3}$
2 = +5V	8 = $\overline{W}$	14 = $\overline{RAS2}$	20 = A5
3 = $\overline{RAS0}$	9 = $\overline{RAS1}$	15 = A2	21 = +5V
4 = Dout	10 = A0	16 = A1	22 = GND
5 = A3	11 = A7	17 = n.c.	
6 = A6	12 = n.c.	18 = A4	

4164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4164 FA 1-12 L	Tix	22-SIP	CMOS	0...+70	800	70	<120	<4	TTL-TS
TM 4164 FA 1-15 L	Tix	22-SIP	CMOS	0...+70	700	70	<150	<4	TTL-TS
TM 4164 FA 1-20 L	Tix	22-SIP	CMOS	0...+70	540	70	<200	<4	TTL-TS
TM 4164 FC 1-12 L	Tix	22-SIP	CMOS	0...+70	800	70	<120	<4	TTL-TS
TM 4164 FC 1-15 L	Tix	22-SIP	CMOS	0...+70	700	70	<150	<4	TTL-TS
TM 4164 FC 1-20 L	Tix	22-SIP	CMOS	0...+70	540	70	<200	<4	TTL-TS

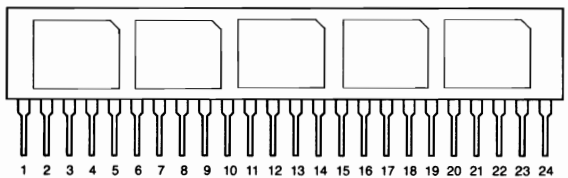
4164 — 65536x4-Bit dynamic RAM-Modul



1 = n.c.	7 = A5	13 = A3	19 = $\overline{RAS}$
2 = +5V	8 = A4	14 = A6	20 = Din3
3 = Din0	9 = Din1	15 = Dout2	21 = Dout3
4 = Dout0	10 = Dout1	16 = Din2	22 = GND
5 = $\overline{CAS}$	11 = $\overline{W}$	17 = A2	
6 = A7	12 = A1	18 = A0	

4164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4164 EA 4-12 L	Tix	22-SIP	CMOS	0...+70	800	70	<120	<4	TTL-TS
TM 4164 EA 4-15 L	Tix	22-SIP	CMOS	0...+70	700	70	<150	<4	TTL-TS
TM 4164 EA 4-20 L	Tix	22-SIP	CMOS	0...+70	540	70	<200	<4	TTL-TS
TM 4164 EC 4-12 L	Tix	22-SIP	CMOS	0...+70	800	70	<120	<4	TTL-TS
TM 4164 EC 4-15 L	Tix	22-SIP	CMOS	0...+70	700	70	<150	<4	TTL-TS
TM 4164 EC 4-20 L	Tix	22-SIP	CMOS	0...+70	540	70	<200	<4	TTL-TS

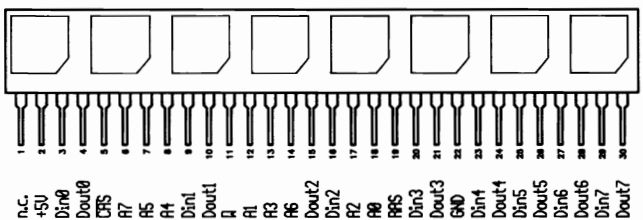
4164 — 65536x5-Bit dynamic RAM-Modul



1 = n.c.	7 = A5	13 = A3	19 = $\overline{RAS}$
2 = +5V	8 = A4	14 = A6	20 = Din3
3 = Din0	9 = Din1	15 = Dout2	21 = Dout3
4 = Dout0	10 = Dout1	16 = Din2	22 = GND
5 = $\overline{CAS}$	11 = $\overline{W}$	17 = A2	23 = Din4
6 = A7	12 = A1	18 = A0	24 = Dout4

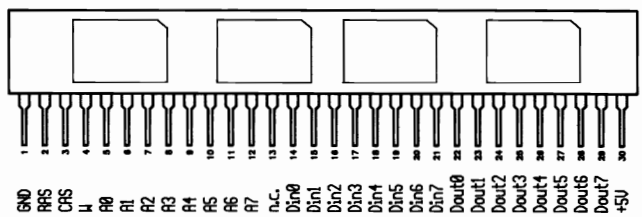
4164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4164 EH 5-12 L	Tix	24-SIP	CMOS	0...+70	1000	87,5	<120	<4	TTL-TS
TM 4164 EH 5-15 L	Tix	24-SIP	CMOS	0...+70	875	87,5	<150	<4	TTL-TS
TM 4164 EH 5-20 L	Tix	24-SIP	CMOS	0...+70	675	87,5	<200	<4	TTL-TS
TM 4164 EQ 5-12 L	Tix	24-SIP	CMOS	0...+70	1000	87,5	<120	<4	TTL-TS
TM 4164 EQ 5-15 L	Tix	24-SIP	CMOS	0...+70	875	87,5	<150	<4	TTL-TS
TM 4164 EQ 5-20 L	Tix	24-SIP	CMOS	0...+70	675	87,5	<200	<4	TTL-TS

4164 — 65536x8-Bit dynamic RAM-Modul



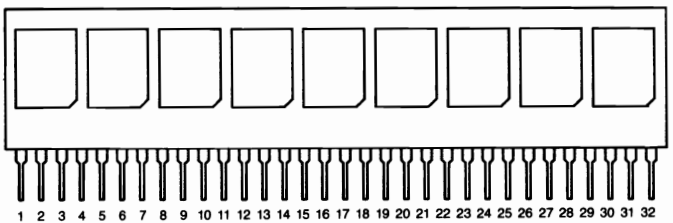
4164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4164 EK 8-12 L	Tix	30-SIP	CMOS	0...+70	1600	140	<120	<4	TTL-TS
TM 4164 EK 8-15 L	Tix	30-SIP	CMOS	0...+70	1400	140	<150	<4	TTL-TS
TM 4164 EK 8-20 L	Tix	30-SIP	CMOS	0...+70	1080	140	<200	<4	TTL-TS

4164 — 65536x8-Bit dynamic RAM-Modul



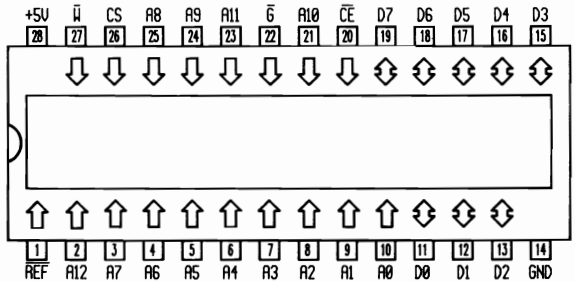
4164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4164 FT 8-12 L	Tix	30-SIP	CMOS	0...+70	1600	140	<120	<4	TTL-TS
TM 4164 FT 8-15 L	Tix	30-SIP	CMOS	0...+70	1400	140	<150	<4	TTL-TS
TM 4164 FT 8-20 L	Tix	30-SIP	CMOS	0...+70	1080	140	<200	<4	TTL-TS

4164 — 65536x9-Bit dynamic RAM-Modul



1 = n.c.	9 = Din1	17 = A2	25 = Din5
2 = +5V	10 = Dout1	18 = A0	26 = Dout5
3 = Din0	11 = $\overline{W}$	19 = $\overline{RAS}$	27 = Din6
4 = Dout0	12 = A1	20 = Din3	28 = Dout6
5 = $\overline{CAS}$	13 = A3	21 = Dout3	29 = Din7
6 = A7	14 = A6	22 = GND	30 = Dout7
7 = A5	15 = Dout2	23 = Din4	31 = Din8
8 = A4	16 = Din2	24 = Dout4	32 = Dout8

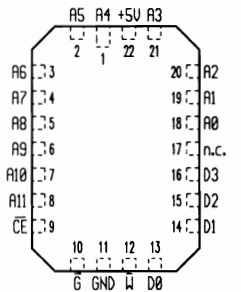
4168 — 8192x8-Bit dynamic RAM



4164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4164 FN 9-12 L	Tix	32-SIP	CMOS	0...+70	1800	157,5	<120	<4	TTL-TS
TM 4164 FN 9-15 L	Tix	32-SIP	CMOS	0...+70	1575	157,5	<150	<4	TTL-TS
TM 4164 FN 9-20 L	Tix	32-SIP	CMOS	0...+70	1215	157,5	<120	<4	TTL-TS

4168 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 4364-15	Mat	28-DIP	NMOS	0...+70	<330	<44	<150	<2	TTL-TS
µPD 4168 C-15	Nip	28-DIP	NMOS	0...+70	<330	27,5	<150	<2	TTL-TS
µPD 4168 C-20	Nip	28-DIP	NMOS	0...+70	<303	27,5	<200	<2	TTL-TS
µPD 4168 C-25	Nip	28-DIP	NMOS	0...+70	<275	27,5	<250	<2	TTL-TS

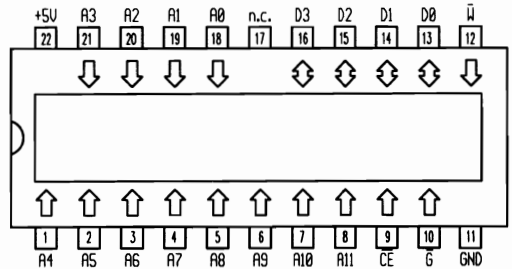
4178 — 4096x1-Bit static RAM



CE	G	W	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

4178 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 41H78 E-20	Tho	22-LCC	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H78 E-25	Tho	22-LCC	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H78 E-35	Tho	22-LCC	CMOS	0...+70	<550	<44	<35		TTL-TS

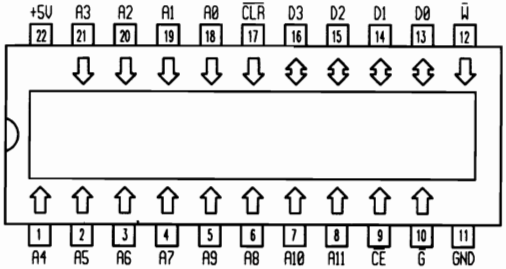
4178 — 4096x1-Bit static RAM



CE	G	W	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

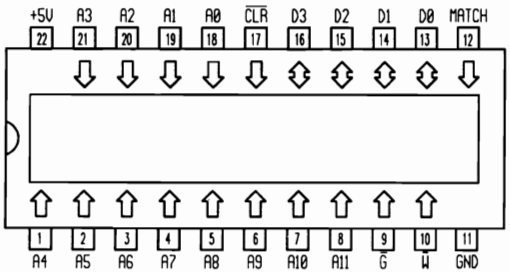
4178 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 41H78 N-20	Tho	22-DIP	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H78 N-25	Tho	22-DIP	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H78 N-35	Tho	22-DIP	CMOS	0...+70	<550	<44	<35		TTL-TS
MK 41H78 P-20	Tho	22-DIC	CMOS	0...+70	<550	<44	<20		TTL-TS
MK 41H78 P-25	Tho	22-DIC	CMOS	0...+70	<550	<44	<25		TTL-TS
MK 41H78 P-35	Tho	22-DIC	CMOS	0...+70	<550	<44	<35		TTL-TS

4179 — 4096x4-Bit static RAM



CE	G	W	CLR	D_{out}	Power	Mode
H	X	X	X	Hi-Z	standby	deselect
L	X	L	H	data in	active	write
L	L	H	H	data out	active	read
L	H	H	H	Hi-Z	active	read
L	X	L	L	Hi-Z	active	flash clear
L	L	H	L	Low-Z	active	flash clear
L	H	H	L	Hi-Z	active	flash clear

4180 — 4096x4-Bit stat. RAM w. 4-Bit Comparator



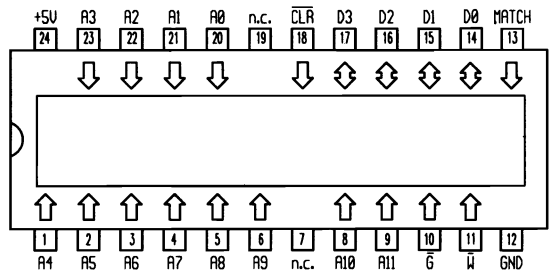
W	G	CLR	Match	Mode
H	H	H	valid	compare
L	X	H	invalid	write
H	L	H	invalid	read
X	X	L	invalid	flash clear

4179 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 41H79 N-20	Sgs	22-DIP	CMOS	0...+70	<660	<88	<20		TTL-TS
MK 41H79 N-25	Sgs	22-DIP	CMOS	0...+70	<660	<88	<25		TTL-TS
MK 41H79 N-35	Sgs	22-DIP	CMOS	0...+70	<660	<88	<35		TTL-TS
MK 41H79 P-20	Sgs	22-DIC	CMOS	0...+70	<660	<88	<20		TTL-TS
MK 41H79 P-25	Sgs	22-DIC	CMOS	0...+70	<660	<88	<25		TTL-TS
MK 41H79 P-35	Sgs	22-DIC	CMOS	0...+70	<660	<88	<35		TTL-TS

4180 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 4180 P-22	Mot	22-DIP	CMOS	0...+70			<22		TTL-TS
MCM 4180 P-25	Mot	22-DIP	CMOS	0...+70			<25		TTL-TS
MCM 4180 P-30	Mot	22-DIP	CMOS	0...+70			<30		TTL-TS
MK 41H80 N-20	Sgs	22-DIP	CMOS	0...+70	<660		<20		TTL-TS
MK 41H80 N-22	Sgs	22-DIP	CMOS	0...+70	<660		<22		TTL-TS
MK 41H80 N-25	Sgs	22-DIP	CMOS	0...+70	<660		<25		TTL-TS
MK 41H80 N-35	Sgs	22-DIP	CMOS	0...+70	<660		<35		TTL-TS
MK 41S80 N-12	Sgs	22-DIP	CMOS	0...+70	<660		<12		TTL-TS

4180 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 41S80 N-15	Sgs	22-DIP	CMOS	0...+70	<660		<15		TTL-TS

4180 — 4096x4-Bit stat. RAM w. 4-Bit Comparator

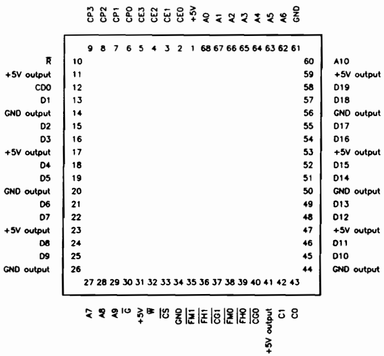


W	G	CLR	Match	Mode
H	H	H	valid	compare
L	X	H	invalid	write
H	L	H	invalid	read
X	X	L	invalid	flash clear

4180 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 41S80 X-12	Sgs	24-FLAT	CMOS	0...+70	<660		<12		TTL-TS
MK 41S80 X-15	Sgs	24-FLAT	CMOS	0...+70	<660		<15		TTL-TS

4202

2048x20-Bit stat. RAM m. Komparator



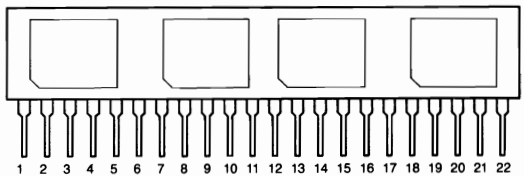
$\overline{R}$	$\overline{CS}$	CE_n	$\overline{W}$	$\overline{G}$	$\overline{FM}_x$	$\overline{FH}_x$	$\overline{CG}_x$	C_x	D_{out}	Mode
H	—	X	—	—	L	X	X	L	—	force miss*
H	—	X	—	—	H	L	X	H	—	force hit*
H	—	X	—	—	H	H	H	Hi-Z	—	compare disable*
H	X	F	X	X	H	H	X	Hi-Z	Hi-Z	standby
H	X	T	H	H	H	H	H	Hi-Z	data in	compare
H	X	T	H	H	H	H	L	H or L	data in	compare
H	H	T	L	X	H	H	L	H	Hi-Z	hit
H	H	T	X	L	H	H	L	H	Hi-Z	hit
H	L	T	L	X	H	H	L	H	data in	write
H	L	T	H	L	H	H	L	H	data out	read
L	H	X	X	X	—	—	—	—	Hi-Z	reset
L	X	F	X	X	—	—	—	—	Hi-Z	reset
L	X	X	H	H	—	—	—	—	Hi-Z	reset
L	X	X	H	L	—	—	—	—	Low-Z	reset
L	L	T	L	X	—	—	—	—	Hi-Z	not allowed**
L	X	T	H	H	H	H	L	L	data in	reset***

F= falsch, CE_n paßt nicht zu P_n; T= richtig, CE_n paßt zu P_n.
F= false, CE_n pattern does not match P_n pattern; T= true, CE_n pattern does match P_n pattern.
F= incorrect, CE_n ne s'adapte pas à P_n; T= correct, CE_n s'adapte à P_n.
F= errato, CE_n non è conforme a P_n; T= esatto, CE_n è conforme a P_n.
F= falso, el patrón CE_n no coincide con ell P_n; T= correcto, el patrón CE_n coincide con el P_n.

* Force hit/miss Funktion sind von den anderen Funktionen unabhängig.
** Kann den Reset unterbrechen ohne das Chip zu beschädigen.
*** Reset fordert ein Low-Pegel an C_x, während eines Vergleiches, falls CD_{outo} D_{in}= H.
* Force hit/miss operations independent of other RAM operations.
** May disrupt Reset, will not damage device.
*** Reset will force C_x low during compare when CD_{outo} is D_{in}= H.
* Fonctions Force hit/miss indépendantes des autres fonctions.
** Peut interrompre la fonction Reset sans détériorer la puce.
*** La fonction Reset exige un niveau Low (bas) sur C_x pendant une comparaison, lorsque CD_{outo} D_{in}= H.
* Funzioni hit/miss indipendenti dalle altre funzioni.
** Può interrompere il reset senza danneggiare il chip.
*** Reset richiede un livello basso a C_x durante un confronto, se CD_{out}= Din= H.
* Las funciones force hit/miss no dependen de las demás funciones del RAM.
** Puede interrumpir el reset sin dañar el chip.
*** Reset exige que C_x presente nivel bajo durante la comparación si CD_{outo} es D_{in}= H.

4202 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4202 Q-20	Sgs	68-PLCC	CMOS	0...+70	<1375	<275	<20		TTL-TS
MK 4202 Q-22	Sgs	68-PLCC	CMOS	0...+70	<1375	<275	<22		TTL-TS
MK 4202 Q-25	Sgs	68-PLCC	CMOS	0...+70	<1375	<275	<25		TTL-TS

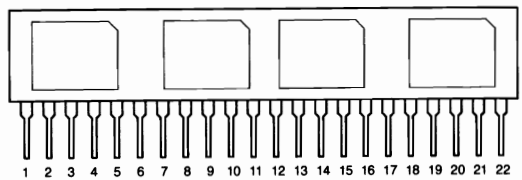
4256 — 1048576x1-Bit dynamic RAM-Modul



1 = GND	7 = Din	13 = $\overline{CAS}$	19 = $\overline{RAS3}$
2 = +5V	8 = W	14 = $\overline{RAS2}$	20 = A5
3 = $\overline{RAS0}$	9 = $\overline{RAS1}$	15 = A2	21 = +5V
4 = Dout	10 = A0	16 = A1	22 = GND
5 = A3	11 = A7	17 = A8	
6 = A6	12 = n.c.	18 = A4	

4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4256 FA 1-12 L	Tix	22-SIP	CMOS	0...+70	362,5	50	<120	<4	TTL-TS
TM 4256 FA 1-15 L	Tix	22-SIP	CMOS	0...+70	312,5	50	<150	<4	TTL-TS
TM 4256 FA 1-20 L	Tix	22-SIP	CMOS	0...+70	262,5	50	<200	<4	TTL-TS
TM 4256 FC 1-12 L	Tix	22-SIP	CMOS	0...+70	362,5	50	<120	<4	TTL-TS
TM 4256 FC 1-15 L	Tix	22-SIP	CMOS	0...+70	312,5	50	<150	<4	TTL-TS
TM 4256 FC 1-20 L	Tix	22-SIP	CMOS	0...+70	262,5	50	<200	<4	TTL-TS

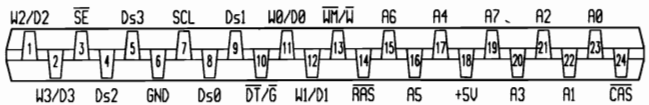
4256 — 262144x4-Bit dynamic RAM-Modul



1 = A8	7 = A5	13 = A3	19 = $\overline{RAS}$
2 = +5V	8 = A4	14 = A6	20 = Din3
3 = Din0	9 = Din1	15 = Dout2	21 = Dout3
4 = Dout0	10 = Dout1	16 = Din2	22 = GND
5 = $\overline{CAS}$	11 = $\overline{W}$	17 = A2	
6 = A7	12 = A1	18 = A0	

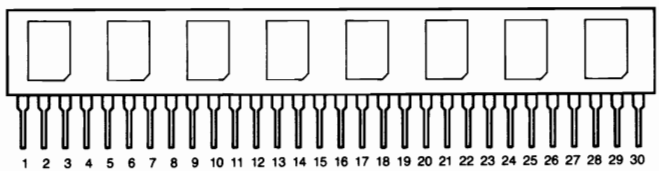
4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 44256-12	Sam	22-SIP	NMOS	0...+70			<120	<4	TTL-TS
KMM 44256-15	Sam	22-SIP	NMOS	0...+70			<150	<4	TTL-TS
KMM 54256-10	Sam	22-SIC	NMOS	0...+70			<100	<4	TTL-TS
KMM 54256-12	Sam	22-SIC	NMOS	0...+70			<120	<4	TTL-TS
MC 41256A4 A-12	Nec	22-SIP	NMOS	0...+70	<1826	110	<120	4	TTL-TS
MC 41256A4 A-15	Nec	22-SIP	NMOS	0...+70	<1540	110	<150	4	TTL-TS
TM 4256 EA 4-12 L	Tix	22-SIP	CMOS	0...+70	1300	50	<120	<4	TTL-TS
TM 4256 EA 4-15 L	Tix	22-SIP	CMOS	0...+70	1100	50	<150	<4	TTL-TS
TM 4256 EA 4-20 L	Tix	22-SIP	CMOS	0...+70	900	50	<200	<4	TTL-TS
TM 4256 EC 4-12 L	Tix	22-SIP	CMOS	0...+70	1300	50	<120	<4	TTL-TS
TM 4256 EC 4-15 L	Tix	22-SIP	CMOS	0...+70	1100	50	<150	<4	TTL-TS
TM 4256 EC 4-20 L	Tix	22-SIP	CMOS	0...+70	900	50	<200	<4	TTL-TS

4256 — 262144x5-Bit dynamic RAM-Modul



4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MC 41256 A5 A-12	Nec	24-SIP	NMOS	0...+70	<2475	137,5	<120	4	TTL-TS
MC 41256 A5 A-15	Nec	24-SIP	NMOS	0...+70	<1732	137.5	<150	4	TTL-TS
TM 4256 EH 5-12 L	Tix	24-SIP	CMOS	0...+70	1625	62,5	<120	<4	TTL-TS
TM 4256 EH 5-15 L	Tix	24-SIP	CMOS	0...+70	1375	62,5	<150	<4	TTL-TS
TM 4256 EH 5-20 L	Tix	24-SIP	CMOS	0...+70	1125	62,5	<200	<4	TTL-TS
TM 4256 EQ 5-12 L	Tix	24-SIP	CMOS	0...+70	1625	62,5	<120	<4	TTL-TS
TM 4256 EQ 5-15 L	Tix	24-SIP	CMOS	0...+70	1375	62,5	<150	<4	TTL-TS
TM 4256 EQ 5-20 L	Tix	24-SIP	CMOS	0...+70	1125	62,5	<200	<4	TTL-TS

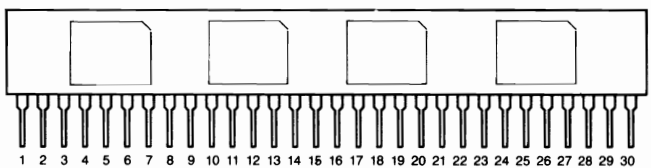
4256 — 262144x8-Bit dynamic RAM-Modul



1 = A8	9 = Din1	17 = A2	25 = Din5
2 = +5V	10 = Dout1	18 = A0	26 = Dout5
3 = Din0	11 = $\overline{W}$	19 = $\overline{RAS}$	27 = Din6
4 = Dout0	12 = A1	20 = Din3	28 = Dout6
5 = $\overline{CAS}$	13 = A3	21 = Dout3	29 = Din7
6 = A7	14 = A6	22 = GND	30 = Dout7
7 = A5	15 = Dout2	23 = Din4	
8 = A4	16 = Din2	24 = Dout4	

4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4256 EK 8-12 L	Tix	30-SIP	CMOS	0...+70	2600	100	<120	<4	TTL-TS
TM 4256 EK 8-15 L	Tix	30-SIP	CMOS	0...+70	2200	100	<150	<4	TTL-TS
TM 4256 EK 8-20 L	Tix	30-SIP	CMOS	0...+70	1800	100	<200	<4	TTL-TS

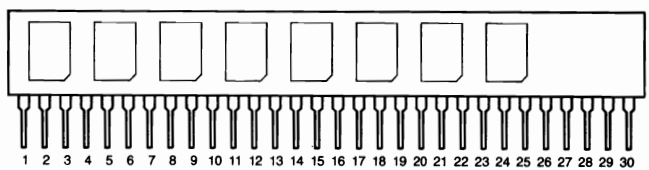
4256 — 262144x8-Bit dynamic RAM-Modul



1 = +5V	9 = GND	17 = A8	25 = D7
2 = $\overline{CAS}$	10 = D2	18 = n.c.	26 = n.c.
3 = D0	11 = A4	19 = n.c.	27 = $\overline{RAS}$
4 = A0	12 = A5	20 = D5	28 = n.c.
5 = A1	13 = D3	21 = $\overline{W}$	29 = n.c.
6 = D1	14 = A6	22 = GND	30 = +5V
7 = A2	15 = A7	23 = D6	
8 = A3	16 = D4	24 = $\overline{PRD}$	

4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4256 GP 8-12 L	Tix	30-SIP	CMOS	0...+70			<120	<4	TTL-TS
TM 4256 GP 8-15 L	Tix	30-SIP	CMOS	0...+70			<150	<4	TTL-TS
TM 4256 GP 8-20 L	Tix	30-SIP	CMOS	0...+70			<200	<4	TTL-TS
TM 4256 GV 8-12 L	Tix	30-SIP	CMOS	0...+70			<120	<4	TTL-TS
TM 4256 GV 8-15 L	Tix	30-SIP	CMOS	0...+70			<150	<4	TTL-TS
TM 4256 GV 8-20 L	Tix	30-SIP	CMOS	0...+70			<200	<4	TTL-TS

4256 — 262144x8-Bit dynamic RAM-Modul

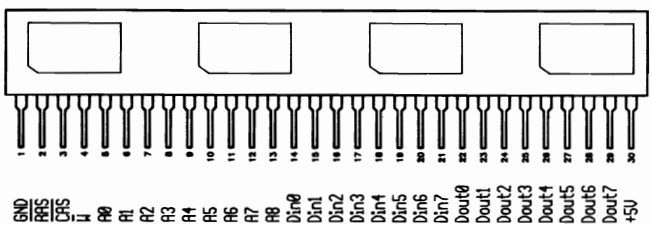


1 = +5V	9 = GND	17 = A8	25 = D7
2 = $\overline{CAS}$	10 = D2	18 = n.c.	26 = n.c.
3 = D0	11 = A4	19 = n.c.	27 = $\overline{RAS}$
4 = A0	12 = A5	20 = D5	28 = n.c.
5 = A1	13 = D3	21 = $\overline{W}$	29 = n.c.
6 = D1	14 = A6	22 = GND	30 = +5V
7 = A2	15 = A7	23 = D6	
8 = A3	16 = D4	24 = n.c.	

4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 48256-12	Sam	30-SIP	NMOS	0...+70	<3300	<198	<120	<4	TTL-TS
KMM 48256-15	Sam	30-SIP	NMOS	0...+70	<2860	<198	<150	<4	TTL-TS
KMM 58256-12	Sam	30-SIC	NMOS	0...+70	<3300	<198	<120	<4	TTL-TS
KMM 58256-15	Sam	30-SIC	NMOS	0...+70	<2860	<198	<150	<4	TTL-TS
MC 41256 A8 A-12	Nec	30-SIP	NMOS	0...+70	<3652	220	<120	4	TTL-TS
MC 41256 A9 A-12	Nec	30-SIP	NMOS	0...+70	<4108	247.5	<120	4	TTL-TS
MC 41256 A8 A-15	Nec	30-SIP	NMOS	0...+70	<3080	220	<150	4	TTL-TS
MC 41256 A9 A-15	Nec	30-SIP	NMOS	0...+70	<3465	247.5	<150	4	TTL-TS

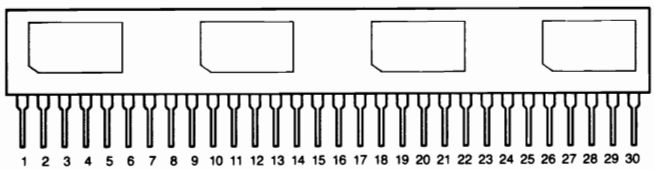
4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MC 41256 A8 B-12	Nec	30-SIC	NMOS	0...+70	<3652	220	<120	4	TTL-TS
MC 41256 A9 B-12	Nec	30-SIC	NMOS	0...+70	<4108	247.5	<120	4	TTL-TS
MC 41256 A8 B-15	Nec	30-SIC	NMOS	0...+70	<3080	220	<150	4	TTL-TS
MC 41256 A9 B-15	Nec	30-SIC	NMOS	0...+70	<3465	247.5	<150	4	TTL-TS
MH 25608 J-10	Mit	30-SIC	NMOS	0...+70	<2880	<200	<100	<4	TTL-TS
MH 25608 J-12	Mit	30-SIC	NMOS	0...+70	<2640	<200	<120	<4	TTL-TS
MH 25608 J-15	Mit	30-SIC	NMOS	0...+70	<2440	<200	<150	<4	TTL-TS
MH 25608 J-85	Mit	30-SIC	NMOS	0...+70	<3080	<200	<85	<4	TTL-TS
MH 25608 JA-10	Mit	30-SIP	NMOS	0...+70	<2880	<200	<100	<4	TTL-TS
MH 25608 JA-12	Mit	30-SIP	NMOS	0...+70	<2640	<200	<120	<4	TTL-TS
MH 25608 JA-15	Mit	30-SIP	NMOS	0...+70	<2440	<200	<150	<4	TTL-TS
MH 25608 JA-85	Mit	30-SIP	NMOS	0...+70	<3080	<200	<85	<4	TTL-TS
TM 4256 FL 8-12 L	Tix	30-SIP	CMOS	0...+70	2600	100	<120	<4	TTL-TS
TM 4256 FL 8-15 L	Tix	30-SIP	CMOS	0...+70	2200	100	<150	<4	TTL-TS
TM 4256 FL 8-20 L	Tix	30-SIP	CMOS	0...+70	1800	100	<200	<4	TTL-TS
TM 4256 GU 8-12 L	Tix	30-SIP	CMOS	0...+70	2600	100	<120	<4	TTL-TS
TM 4256 GU 8-15 L	Tix	30-SIP	CMOS	0...+70	2200	100	<150	<4	TTL-TS
TM 4256 GU 8-20 L	Tix	30-SIP	CMOS	0...+70	1800	100	<200	<4	TTL-TS

4256 — 262144x8-Bit dynamic RAM-Modul



4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4256 FT 8-10 L	Tix	30-SIP	CMOS	0...+70	3000	100	<100	<4	TTL-TS
TM 4256 FT 8-12 L	Tix	30-SIP	CMOS	0...+70	2600	100	<120	<4	TTL-TS
TM 4256 FT 8-15 L	Tix	30-SIP	CMOS	0...+70	2200	100	<150	<4	TTL-TS
TM 4256 FT 8-20 L	Tix	30-SIP	CMOS	0...+70	1800	100	<200	<4	TTL-TS

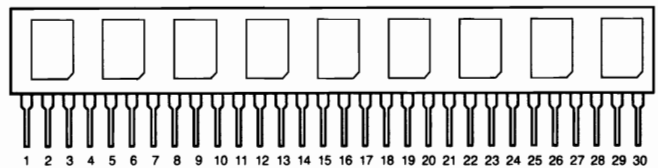
4256 — 262144x8-Bit dynamic RAM-Modul



1 = GND	9 = A4	17 = Din3	25 = Dout3
2 = $\overline{RAS}$	10 = A5	18 = Din4	26 = Dout4
3 = $\overline{CAS}$	11 = A6	19 = Din5	27 = Dout5
4 = $\overline{W}$	12 = A7	20 = Din6	28 = Dout6
5 = A0	13 = A8	21 = Din7	29 = Dout7
6 = A1	14 = Din0	22 = Dout0	30 = + 5V
7 = A2	15 = Din1	23 = Dout1	
8 = A3	16 = Din2	24 = Dout2	

4256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4256 FT 8-10 L	Tix	30-SIP	CMOS	0...+70	3000	100	<100	<4	TTL-TS
TM 4256 FT 8-12 L	Tix	30-SIP	CMOS	0...+70	2600	100	<120	<4	TTL-TS
TM 4256 FT 8-15 L	Tix	30-SIP	CMOS	0...+70	2200	100	<150	<4	TTL-TS
TM 4256 FT 8-20 L	Tix	30-SIP	CMOS	0...+70	1800	100	<200	<4	TTL-TS

4256 — 262144x9-Bit dynamic RAM-Modul

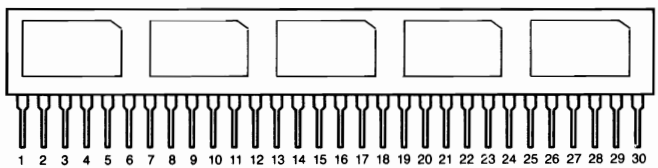


1 = + 5V	9 = GND	17 = A8	25 = D7
2 = $\overline{CAS}$	10 = D2	18 = n.c.	26 = Dout8
3 = D0	11 = A4	19 = n.c.	27 = $\overline{RAS}$
4 = A0	12 = A5	20 = D5	28 = $\overline{CAS}$
5 = A1	13 = D3	21 = $\overline{W}$	29 = Din8
6 = D1	14 = A6	22 = GND	30 = + 5V
7 = A2	15 = A7	23 = D6	
8 = A3	16 = D4	24 = n.c.	

4256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYM 39500 S-80	Sie	30-SIC	NMOS	0...+70	<1045	<41,25	<80	<8	TTL-TS
KMM 49256-12	Sam	30-SIP	NMOS	0...+70	<3712	<225,5	<120	<4	TTL-TS
KMM 49256-15	Sam	30-SIP	NMOS	0...+70	<3217	<225,5	<150	<4	TTL-TS
KMM 59256-12	Sam	30-SIC	NMOS	0...+70	<3712	<225,5	<120	<4	TTL-TS
KMM 59256-15	Sam	30-SIC	NMOS	0...+70	<3217	<225,5	<150	<4	TTL-TS
MH 25609 J-10	Mit	30-SIC	NMOS	0...+70	<3240	<225	<100	<4	TTL-TS
MH 25609 J-12	Mit	30-SIC	NMOS	0...+70	<2970	<225	<120	<4	TTL-TS
MH 25609 J-15	Mit	30-SIC	NMOS	0...+70	<2750	<225	<150	<4	TTL-TS

4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MH 25609 J-85	Mit	30-SIC	NMOS	0...+70	<3470	<225	<85	<4	TTL-TS
MH 25609 JA-10	Mit	30-SIP	NMOS	0...+70	<3240	<225	<100	<4	TTL-TS
MH 25609 JA-12	Mit	30-SIP	NMOS	0...+70	<2970	<225	<120	<4	TTL-TS
MH 25609 JA-15	Mit	30-SIP	NMOS	0...+70	<2750	<225	<150	<4	TTL-TS
MH 25609 JA-85	Mit	30-SIP	NMOS	0...+70	<3740	<225	<85	<4	TTL-TS
TM 4256 EL 9-12 L	Tix	30-SIP	CMOS	0...+70	2925	115	<120	<4	TTL-TS
TM 4256 EL 9-15 L	Tix	30-SIP	CMOS	0...+70	2475	115	<150	<4	TTL-TS
TM 4256 EL 9-20 L	Tix	30-SIP	CMOS	0...+70	2025	115	<200	<4	TTL-TS
TM 4256 GU 9-12 L	Tix	30-SIP	CMOS	0...+70	2925	115	<120	<4	TTL-TS
TM 4256 GU 9-15 L	Tix	30-SIP	CMOS	0...+70	2475	115	<150	<4	TTL-TS
TM 4256 GU 9-20 L	Tix	30-SIP	CMOS	0...+70	2025	115	<200	<4	TTL-TS

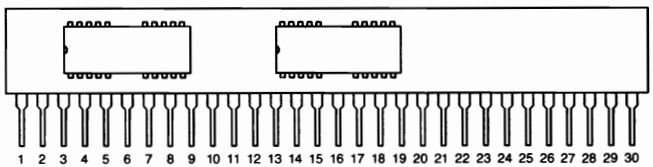
4256 — 262144x9-Bit dynamic RAM-Modul



1 = +5V	9 = GND	17 = A8	25 = D7
2 = $\overline{CAS}$	10 = D2	18 = n.c.	26 = Dout8
3 = D0	11 = A4	19 = n.c.	27 = $\overline{RAS}$
4 = A0	12 = A5	20 = D5	28 = $\overline{CAS}$
5 = A1	13 = D3	21 = $\overline{W}$	29 = Din8
6 = D1	14 = A6	22 = GND	30 = +5V
7 = A2	15 = A7	23 = D6	
8 = A3	16 = D4	24 = $\overline{PRD}$	

4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4256 GP 9-12 L	Tix	30-SIP	CMOS	0...+70			<120	<4	TTL-TS
TM 4256 GP 9-15 L	Tix	30-SIP	CMOS	0...+70			<150	<4	TTL-TS
TM 4256 GP 9-20 L	Tix	30-SIP	CMOS	0...+70			<200	<4	TTL-TS
TM 4256 GV 9-12 L	Tix	30-SIP	CMOS	0...+70			<120	<4	TTL-TS
TM 4256 GV 9-15 L	Tix	30-SIP	CMOS	0...+70			<150	<4	TTL-TS
TM 4256 GV 9-20 L	Tix	30-SIP	CMOS	0...+70			<200	<4	TTL-TS

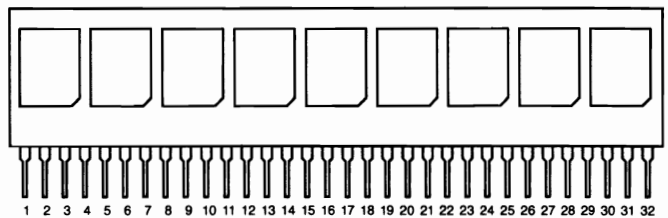
4256 — 262144x8-Bit dynamic RAM-Modul



1 = +5V	9 = GND	17 = A8	25 = D7
2 = $\overline{CAS}$	10 = D2	18 = n.c.	26 = n.c.
3 = D0	11 = A4	19 = n.c.	27 = $\overline{RAS}$
4 = A0	12 = A5	20 = D5	28 = n.c.
5 = A1	13 = D3	21 = $\overline{W}$	29 = n.c.
6 = D1	14 = A6	22 = GND	30 = +5V
7 = A2	15 = A7	23 = D6	
8 = A3	16 = D4	24 = n.c.	

4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MH 25608 AJ-10	Mit	30-SIC	NMOS	0...+70	<716	<5,5	<100	<8	TTL-TS
MH 25608 AJ-12	Mit	30-SIC	NMOS	0...+70	<606	<5,5	<120	<8	TTL-TS
MH 25608 AJ-8	Mit	30-SIC	NMOS	0...+70	<826	<5,5	<80	<8	TTL-TS
MH 25608 AJA-10	Mit	30-SIP	NMOS	0...+70	<716	<5,5	<100	<8	TTL-TS
MH 25608 AJA-12	Mit	30-SIP	NMOS	0...+70	<606	<5,5	<120	<8	TTL-TS
MH 25608 AJA-8	Mit	30-SIP	NMOS	0...+70	<826	<5,5	<80	<8	TTL-TS

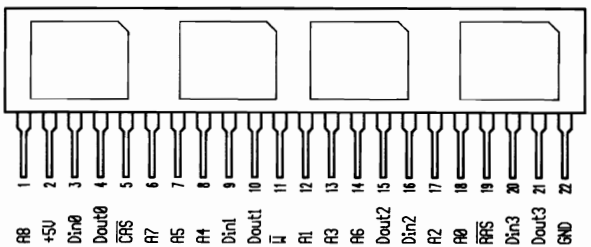
4256 — 262144x9-Bit dynamic RAM-Modul



1 = A8	9 = Din1	17 = A2	25 = Din5
2 = +5V	10 = Dout1	18 = A0	26 = Dout5
3 = Din0	11 = $\overline{W}$	19 = $\overline{RAS}$	27 = Din6
4 = Dout0	12 = A1	20 = Din3	28 = Dout6
5 = $\overline{CAS}$	13 = A3	21 = Dout3	29 = Din7
6 = A7	14 = A6	22 = GND	30 = Dout7
7 = A5	15 = Dout2	23 = Din4	31 = Din8
8 = A4	16 = Din2	24 = Dout4	32 = Dout8

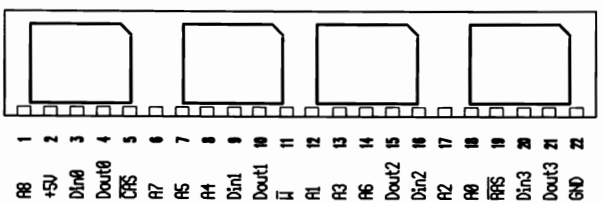
4256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4256 FN 9-12 L	Tix	32-SIP	CMOS	0...+70	2925	112,5	<120	<4	TTL-TS
TM 4256 FN 9-15 L	Tix	32-SIP	CMOS	0...+70	2475	112,5	<150	<4	TTL-TS
TM 4256 FN 9-20 L	Tix	32-SIP	CMOS	0...+70	2025	112,5	<200	<4	TTL-TS

4257 — 262144x4-Bit dynamic RAM-Modul



4257 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 44257-12	Sam	22-SIP	NMOS	0...+70			<120	<4	TTL-TS
KMM 44257-15	Sam	22-SIP	NMOS	0...+70			<150	<4	TTL-TS

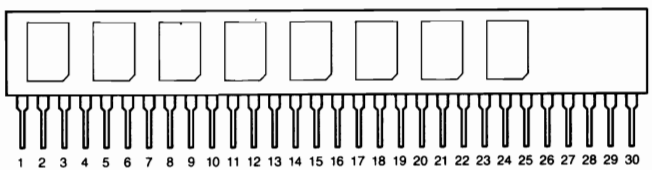
4257 — 262144x4-Bit dynamic RAM-Modul



4257 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 54257-10	Sam	22-SIP	NMOS	0...+70			<100	<4	TTL-TS
KMM 54257-12	Sam	22-SIP	NMOS	0...+70			<120	<4	TTL-TS

4257

262144x8-Bit dynamic RAM-Modul

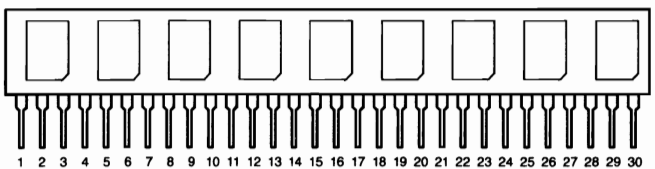


1 = +5V	9 = GND	17 = A8	25 = D7
2 = $\overline{CAS}$	10 = D2	18 = n.c.	26 = n.c.
3 = D0	11 = A4	19 = n.c.	27 = $\overline{RAS}$
4 = A0	12 = A5	20 = D5	28 = n.c.
5 = A1	13 = D3	21 = $\overline{W}$	29 = n.c.
6 = D1	14 = A6	22 = GND	30 = +5V
7 = A2	15 = A7	23 = D6	
8 = A3	16 = D4	24 = n.c.	

4257 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 48257-12	Sam	30-SIP	NMOS	0...+70	<3300	<198	<120	<4	TTL-TS
KMM 48257-15	Sam	30-SIP	NMOS	0...+70	<2860	<198	<150	<4	TTL-TS
KMM 58257-12	Sam	30-SIC	NMOS	0...+70	<3300	<198	<120	<4	TTL-TS
KMM 58257-15	Sam	30-SIC	NMOS	0...+70	<2860	<198	<150	<4	TTL-TS
TM 4257 FL 8-12 L	Tix	30-SIP	CMOS	0...+70	2600	100	<120	<4	TTL-TS
TM 4257 FL 8-15 L	Tix	30-SIP	CMOS	0...+70	2200	100	<150	<4	TTL-TS
TM 4257 FL 8-20 L	Tix	30-SIP	CMOS	0...+70	1800	100	<200	<4	TTL-TS
TM 4257 GU 8-12 L	Tix	30-SIP	CMOS	0...+70	2600	100	<120	<4	TTL-TS
TM 4257 GU 8-15 L	Tix	30-SIP	CMOS	0...+70	2200	100	<150	<4	TTL-TS
TM 4257 GU 8-20 L	Tix	30-SIP	CMOS	0...+70	1800	100	<200	<4	TTL-TS

4257

262144x9-Bit dynamic RAM-Modul

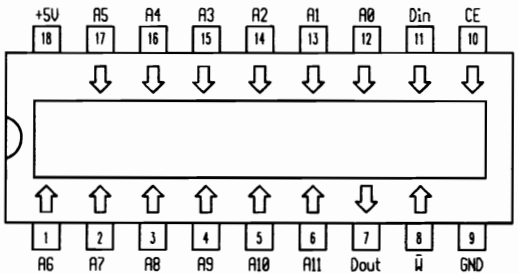


1 = +5V	9 = GND	17 = A8	25 = D7
2 = $\overline{CAS}$	10 = D2	18 = n.c.	26 = Dout8
3 = D0	11 = A4	19 = n.c.	27 = $\overline{RAS}$
4 = A0	12 = A5	20 = D5	28 = $\overline{CAS}$
5 = A1	13 = D3	21 = $\overline{W}$	29 = Din8
6 = D1	14 = A6	22 = GND	30 = +5V
7 = A2	15 = A7	23 = D6	
8 = A3	16 = D4	24 = n.c.	

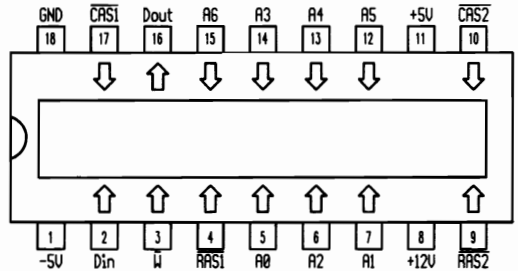
4257 Type	Herst. Manuf. Fabr. Prod. Fabr.	Gehäuse Case Boîtier Carcassa Cápsula	Techn. Techn. Techn. Tecn. Tecn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KMM 49257-12	Sam	30-SIP	NMOS	0...+70	<3712	<225,5	<120	<4	TTL-TS
KMM 49257-15	Sam	30-SIP	NMOS	0...+70	<3217	<225,5	<150	<4	TTL-TS
KMM 59257-12	Sam	30-SIC	NMOS	0...+70	<3712	<225,5	<120	<4	TTL-TS
KMM 59257-15	Sam	30-SIC	NMOS	0...+70	<3217	<225,5	<150	<4	TTL-TS
TM 4257 EL 9-12 L	Tix	30-SIP	CMOS	0...+70	2925	115	<120	<4	TTL-TS
TM 4257 EL 9-15 L	Tix	30-SIP	CMOS	0...+70	2475	115	<150	<4	TTL-TS
TM 4257 EL 9-20 L	Tix	30-SIP	CMOS	0...+70	2025	115	<200	<4	TTL-TS
TM 4257 GU 9-12 L	Tix	30-SIP	CMOS	0...+70	2925	115	<120	<4	TTL-TS

4257 Typ · Type · Tipo	Herst. Manuf. Fabr. Prod. Fabr.	Gehäuse Case Boîtier Carcassa Cápsula	Techn. Techn. Techn. Tecn. Tecn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
TM 4257 GU 9-15 L	Tix	30-SIP	CMOS	0...+70	2475	115	<150	<4	TTL-TS
TM 4257 GU 9-20 L	Tix	30-SIP	CMOS	0...+70	2025	115	<200	<4	TTL-TS

4315 — 4096x1-Bit static RAM



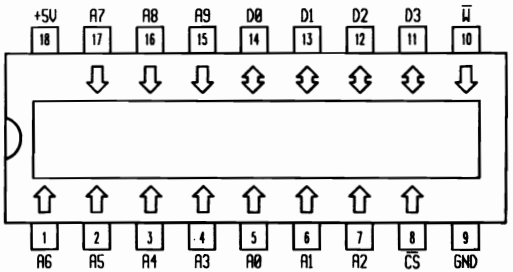
4332 — 32768x1-Bit dynamic RAM



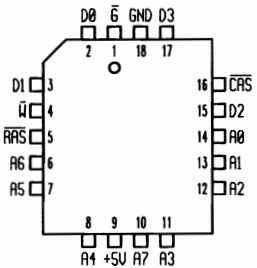
4315 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 4315 P	Hit	18-DIP	CMOS	0...+70	20	10µ	<450		CMOS

4332 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4332 D-3	Mos	18-DIP	NMOS	0...+70	<482	<40	<200	<2	TTL-TS
MKB 4332 D-83	Mos	18-DIP	NMOS	0...+70	<482	<40	<200	<2	TTL-TS
MKB 4332 D-84	Mos	18-DIP	NMOS	0...+70	<482	<40	<250	<2	TTL-TS
MKB 4332 D-93	Mos	18-DIP	NMOS	0...+70	<482	<40	<200	<1	TTL-TS

4334 — 1024x4-Bit static RAM



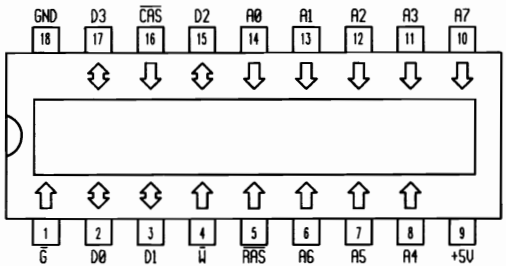
4416 — 16384x4-Bit dynamic RAM



4334 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	$mW/bit	taa ns	tref ms	Output
HM 4334-3	Hit	18-DIC	CMOS	0...+70	20	10µ		<300		TTL-TS
HM 4334-4	Hit	18-DIC	CMOS	0...+70	20	10µ		<450		TTL-TS
HM 4334-P 3	Hit	18-DIP	CMOS	0...+70	20	10µ		<300		TTL-TS
HM 4334 P-3 L	Hit	18-DIP	CMOS	0...+70	20	10µ		<300		TTL-TS
HM 4334-P 4	Hit	18-DIP	CMOS	0...+70	20	10µ		<450		TTL-TS
HM 4334 P-4 L	Hit	18-DIP	CMOS	0...+70	20	10µ		<300		TTL-TS

4416 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	$mW/bit	taa ns	tref ms	Output
TMS 4416-12 FPL	Tix	18-PLCC	NMOS	0...+70	<297	<27,5		<120	<4	TTL-TS
TMS 4416-15 FPL	Tix	18-PLCC	NMOS	0...+70	<297	<27,5		<150	<4	TTL-TS
TMS 4416-20 FPL	Tix	18-PLCC	NMOS	0...+70	<297	<27,5		<200	<4	TTL-TS

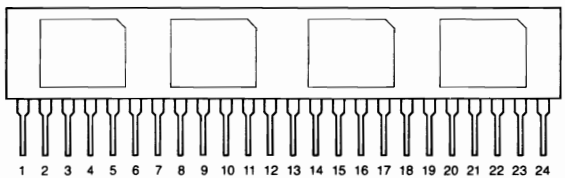
4416 — 16384x4-Bit dynamic RAM



4416 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4416-12 NL	Tix	18-DIP	NMOS	0...+70	<297	<27,5	<120	<4	TTL-TS
TMS 4416-15 NL	Tix	18-DIP	NMOS	0...+70	<297	<27,5	<150	<4	TTL-TS
TMS 4416-20 NL	Tix	18-DIP	NMOS	0...+70	<297	<27,5	<200	<4	TTL-TS
µPD 41416 C-12	Nec	18-DIP	NMOS	0...+70	<303	28	<120	<2	TTL-TS
µPD 41416 C-15	Nec	18-DIP	NMOS	0...+70	<275	28	<150	<2	TTL-TS
µPD 41416 C-20	Nec	18-DIP	NMOS	0...+70	<250	28	<200	<2	TTL-TS

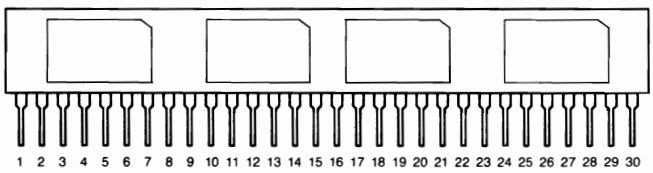
4416 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 4264-12	Mat	18-DIP	NMOS	0...+70	<275	<33	<120	<2	TTL-TS
MN 4264-15	Mat	18-DIP	NMOS	0...+70	<275	<33	<150	<2	TTL-TS
SMJ 4416-12 JDL	Tix	18-DIC	NMOS	0...+70	<264	<27,5	<120	<4	TTL-TS
SMJ 4416-12 JDS	Tix	18-DIC	NMOS	-55...+100	<264	<27,5	<120	<4	TTL-TS
SMJ 4416-15 JDL	Tix	18-DIC	NMOS	0...+70	<264	<27,5	<150	<4	TTL-TS
SMJ 4416-15 JDS	Tix	18-DIC	NMOS	-55...+100	<264	<27,5	<150	<4	TTL-TS
SMJ 4416-20 JDL	Tix	18-DIC	NMOS	0...+70	<231	<27,5	<200	<4	TTL-TS
SMJ 4416-20 JDS	Tix	18-DIC	NMOS	-55...+100	<231	<27,5	<200	<4	TTL-TS

4416 — 32768x8-Bit dynamic RAM-Modul



1 = +5V	7 = D2	13 = $\overline{CAS}$	19 = D6
2 = $\overline{G0}$	8 = D3	14 = A0	20 = D7
3 = $\overline{G1}$	9 = $\overline{RAS0}$	15 = A1	21 = A4
4 = $\overline{W}$	10 = $\overline{RAS1}$	16 = A5	22 = A2
5 = D0	11 = A7	17 = D4	23 = A3
6 = D1	12 = A6	18 = D5	24 = GND

4416 — 16384x16-Bit dynamic RAM-Modul

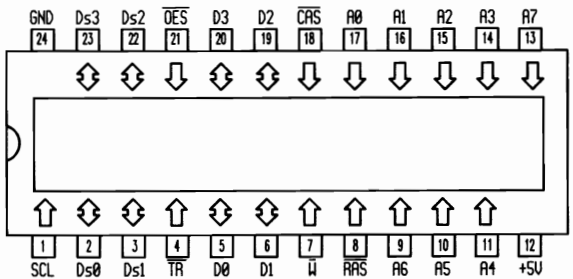


1 = GND	9 = A2	17 = D7	25 = A7
2 = W	10 = A3	18 = A4	26 = D12
3 = D0	11 = G	19 = A5	27 = D13
4 = D1	12 = RAS	20 = D8	28 = D14
5 = D2	13 = CAS	21 = D9	29 = D15
6 = D3	14 = D4	22 = D10	30 = +5V
7 = A0	15 = D5	23 = D11	
8 = A1	16 = D6	24 = A6	

4416 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4416 EE 8-15 L	Tix	24-SIP	CMOS	0...+70	800	70	<150	<4	TTL-TS
TM 4416 EE 8-20 L	Tix	24-SIP	CMOS	0...+70	700	70	<200	<4	TTL-TS
TM 4416 EF 8-15 L	Tix	24-SIP	CMOS	0...+70	800	70	<150	<4	TTL-TS
TM 4416 EF 8-20 L	Tix	24-SIP	CMOS	0...+70	700	70	<200	<4	TTL-TS

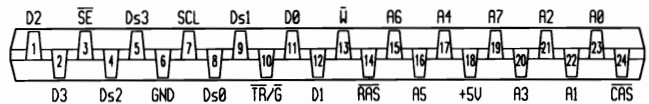
4416 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4416 EJ 16-15 L	Tix	30-SIP	CMOS	0...+70	800	70	<150	<4	TTL-TS
TM 4416 EJ 16-20 L	Tix	30-SIP	CMOS	0...+70	700	70	<200	<4	TTL-TS
TM 4416 ET 16-15 L	Tix	30-SIP	CMOS	0...+70	800	70	<150	<4	TTL-TS
TM 4416 ET 16-20 L	Tix	30-SIP	CMOS	0...+70	700	70	<200	<4	TTL-TS

4461 — 65536x4-Bit Video RAM



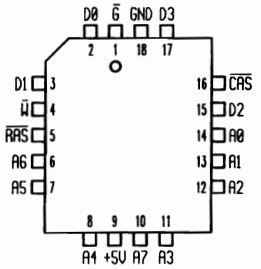
4461 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SMJ 4461-15 JDL	Tix	24-TDIC	NMOS	0...+70	<440	<110	<150	<4	TTL-TS
SMJ 4461-15 JDS	Tix	24-TDIC	NMOS	-55...+110	<440	<110	<150	<4	TTL-TS
TMS 4461-12 NL	Tix	24-TDIP	NMOS	0...+70	<385	<137,5	<120	<4	TTL-TS
TMS 4461-15 NL	Tix	24-TDIP	NMOS	0...+70	<385	<137,5	<150	<4	TTL-TS
TMX 4461 NL	Tix	24-TDIP	NMOS	0...+70	250		<120	<4	TTL-TS

4461 — 65536x4-Bit Multiport Video RAM



4461 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4461-12 SDL	Tix	24-ZIP	NMOS	0...+70	<385	<137,5	<120	<4	TTL-TS
TMS 4461-15 SDL	Tix	24-ZIP	NMOS	0...+70	<385	<137,5	<150	<4	TTL-TS

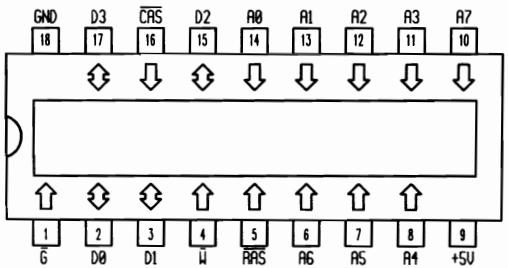
4464 — 65536x4-Bit dynamic RAM



4464 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 50464 CP-12	Hit	18-PLCC	NMOS	0...+70	<456,5	<55	<120	<4	TTL-TS
HM 50464 CP-15	Hit	18-PLCC	NMOS	0...+70	<385	<55	<150	<4	TTL-TS
HM 50464 CP-20	Hit	18-PLCC	NMOS	0...+70	<302,5	<55	<200	<4	TTL-TS
HM 50465 CP-12	Hit	18-PLCC	NMOS	0...+70	<456,5	<55	<120	<4	TTL-TS
HM 50465 CP-15	Hit	18-PLCC	NMOS	0...+70	<385	<55	<150	<4	TTL-TS
HM 50465 CP-20	Hit	18-PLCC	NMOS	0...+70	<302,5	<55	<200	<4	TTL-TS
KM 41464 AJ-12	Sam	18-PLCC	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41464 AJ-15	Sam	18-PLCC	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS

4464 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 4464 AJ-10	Mit	18-PLCC	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4464 AJ-12	Mit	18-PLCC	NMOS	0...+70	<330	<25	<120	<4	TTL-TS
M5M 4464 AJ-15	Mit	18-PLCC	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4464 AJ-8	Mit	18-PLCC	NMOS	0...+70	<385	<25	<80	<4	TTL-TS
MN 41464 AJ-08	Mat	18-PLCC	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41464 AJ-10	Mat	18-PLCC	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41464 AJ-12	Mat	18-PLCC	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
SMJ 4464-12 FVL	Tix	18-LCC	NMOS	0...+70	<440	<44	<120	<4	TTL-TS
SMJ 4464-12 FVS	Tix	18-LCC	NMOS	-55...+110	<440	<44	<120	<4	TTL-TS
SMJ 4464-15 FVL	Tix	18-LCC	NMOS	0...+70	<385	<44	<150	<4	TTL-TS
SMJ 4464-15 FVS	Tix	18-LCC	NMOS	-55...+110	<385	<44	<150	<4	TTL-TS
SMJ 4464-20 FVL	Tix	18-LCC	NMOS	0...+70	<330	<44	<200	<4	TTL-TS
SMJ 4464-20 FVS	Tix	18-LCC	NMOS	-55...+110	<330	<44	<200	<4	TTL-TS
TMM 41464 AT-10	Tos	18-PLCC	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41464 AT-12	Tos	18-PLCC	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
TMM 41464 AT-15	Tos	18-PLCC	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
TMS 4464-10 FML	Tix	18-PLCC	NMOS	0...+70	<330	<25	<100	<4	TTL-TS
TMS 4464-12 FML	Tix	18-PLCC	NMOS	0...+70	<330	<25	<120	<4	TTL-TS
TMS 4464-15 FML	Tix	18-PLCC	NMOS	0...+70	<330	<25	<150	<4	TTL-TS
µPD 41464 L-10	Nec	18-PLCC	NMOS	0...+70	<440	28	<100	<4	TTL-TS
µPD 41464 L-12	Nec	18-PLCC	NMOS	0...+70	<412	28	<120	<4	TTL-TS
µPD 41464 L-15	Nec	18-PLCC	NMOS	0...+70	<385	28	<150	<4	TTL-TS

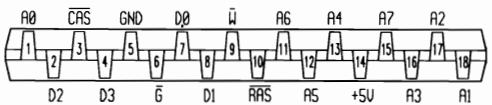
4464 — 65536x4-Bit dynamic RAM



4464 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 50464 P-12	Hit	18-DIP	NMOS	0...+70	<456,5	<55	<120	<4	TTL-TS
HM 50464 P-15	Hit	18-DIP	NMOS	0...+70	<385	<55	<150	<4	TTL-TS
HM 50464 P-20	Hit	18-DIP	NMOS	0...+70	<302,5	<55	<200	<4	TTL-TS
HM 50465 P-12	Hit	18-DIP	NMOS	0...+70	<456,5	<55	<120	<4	TTL-TS
HM 50465 P-15	Hit	18-DIP	NMOS	0...+70	<385	<55	<150	<4	TTL-TS
HM 50465 P-20	Hit	18-DIP	NMOS	0...+70	<302,5	<55	<200	<4	TTL-TS
KM 41464 AP-12	Sam	18-DIP	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41464 AP-15	Sam	18-DIP	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS

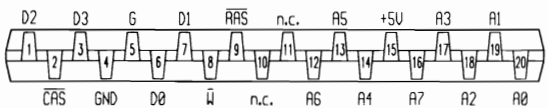
4464 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 4464 AP-10	Mit	18-DIP	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4464 AP-12	Mit	18-DIP	NMOS	0...+70	<330	<25	<120	<4	TTL-TS
M5M 4464 AP-15	Mit	18-DIP	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4464 AP-8	Mit	18-DIP	NMOS	0...+70	<385	<25	<80	<4	TTL-TS
MCM 41464 AP-10	Mot	18-DIP	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
MCM 41464 AP-12	Mot	18-DIP	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
MCM 41464 AP-15	Mot	18-DIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
MN 41464 A-08	Mat	18-DIP	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41464 A-10	Mat	18-DIP	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41464 A-12	Mat	18-DIP	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
SMJ 4464-12 JDL	Tix	18-TDIC	NMOS	0...+70	<440	<44	<120	<4	TTL-TS
SMJ 4464-12 JDS	Tix	18-TDIC	NMOS	-55...+110	<440	<44	<120	<4	TTL-TS
SMJ 4464-15 JDL	Tix	18-TDIC	NMOS	0...+70	<385	<44	<150	<4	TTL-TS
SMJ 4464-15 JDS	Tix	18-TDIC	NMOS	-55...+110	<385	<44	<150	<4	TTL-TS
SMJ 4464-20 JDL	Tix	18-TDIC	NMOS	0...+70	<330	<44	<200	<4	TTL-TS
SMJ 4464-20 JDS	Tix	18-TDIC	NMOS	-55...+110	<330	<44	<200	<4	TTL-TS
TMM 41464 AP-10	Tos	18-DIP	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41464 AP-12	Tos	18-DIP	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
TMM 41464 AP-15	Tos	18-DIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
TMS 4464-10 NL	Tix	18-DIP	NMOS	0...+70	<330	<25	<100	<4	TTL-TS
TMS 4464-12 NL	Tix	18-DIP	NMOS	0...+70	<440	<27,5	<120	<4	TTL-TS
TMS 4464-15 NL	Tix	18-DIP	NMOS	0...+70	<385	<27,5	<150	<4	TTL-TS
TMS 4464-20 NL	Tix	18-DIP	NMOS	0...+70	<330	<27,5	<200	<4	TTL-TS
µPD 41464 C-10	Nec	18-DIP	NMOS	0...+70	<385	28	<100	<4	TTL-TS
µPD 41464 C-12	Nec	18-DIP	NMOS	0...+70	<412	28	<120	<4	TTL-TS
µPD 41464 C-15	Nec	18-DIP	NMOS	0...+70	<440	28	<150	<4	TTL-TS

4464 — 65536x4-Bit dynamic RAM (page mode)



4464 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 41464 AL-08	Mat	18-ZIP	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41464 AL-10	Mat	18-ZIP	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41464 AL-12	Mat	18-ZIP	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS

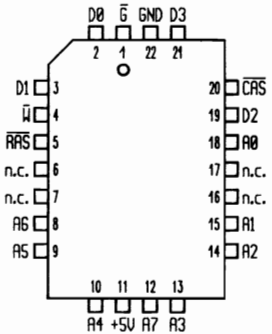
4464 — 65536x4-Bit dynamic RAM



4464 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41464 AZ-12	Sam	20-ZIP	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41464 AZ-15	Sam	20-ZIP	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS
M5M 4464 AL-10	Mit	20-ZIP	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4464 AL-12	Mit	20-ZIP	NMOS	0...+70	<330	<25	<120	<4	TTL-TS
M5M 4464 AL-15	Mit	20-ZIP	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4464 AL-8	Mit	20-ZIP	NMOS	0...+70	<385	<25	<80	<4	TTL-TS
MN 41464 AZ-08	Mat	20-ZIP	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41464 AZ-10	Mat	20-ZIP	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS

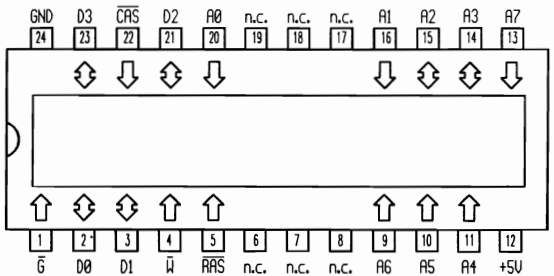
4464 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 41464 AZ-12	Mat	20-ZIP	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
TMM 41464 AZ-10	Tos	20-ZIP	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41464 AZ-12	Tos	20-ZIP	NMOS	0...+70	<398	<28	<120	<4	TTL-TS
TMM 41464 AZ-15	Tos	20-ZIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
µPD 41464 V-10	Nec	20-ZIP	NMOS	0...+70	<440	28	<100	<4	TTL-TS
µPD 41464 V-12	Nec	20-ZIP	NMOS	0...+70	<412	28	<120	<4	TTL-TS
µPD 41464 V-15	Nec	20-ZIP	NMOS	0...+70	<385	28	<150	<4	TTL-TS

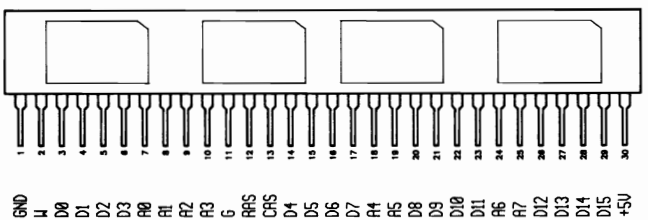
4464 — 65536x4-Bit dynamic RAM



4464 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4464-12 FML	Tix	22-PLCC	NMOS	0...+70	<440	<27,5	<120	<4	TTL-TS
TMS 4464-15 FML	Tix	22-PLCC	NMOS	0...+70	<385	<27,5	<150	<4	TTL-TS
TMS 4464-20 FML	Tix	22-PLCC	NMOS	0...+70	<330	<27,5	<200	<4	TTL-TS

4464	65536x4-Bit dynamic RAM (page mode)	4464	65536x16-Bit dynamic RAM-Modul

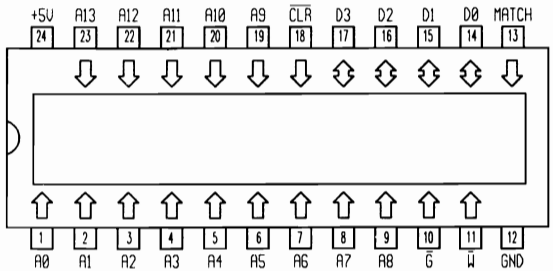




4464 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 41464 AS-08	Mat	24-FLAT	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41464 AS-10	Mat	24-FLAT	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41464 AS-12	Mat	24-FLAT	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS

4464 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TM 4464 EJ 16-12 L	Tix	30-SIP	CMOS	0...+70	1300	50	<120	<4	TTL-TS
TM 4464 EJ 16-15 L	Tix	30-SIP	CMOS	0...+70	1100	50	<150	<4	TTL-TS
TM 4464 EJ 16-20 L	Tix	30-SIP	CMOS	0...+70	900	50	<200	<4	TTL-TS
TM 4464 ET 16-12 L	Tix	30-SIP	CMOS	0...+70	1300	50	<120	<4	TTL-TS
TM 4464 ET 16-15 L	Tix	30-SIP	CMOS	0...+70	1100	50	<150	<4	TTL-TS
TM 4464 ET 16-20 L	Tix	30-SIP	CMOS	0...+70	900	50	<200	<4	TTL-TS

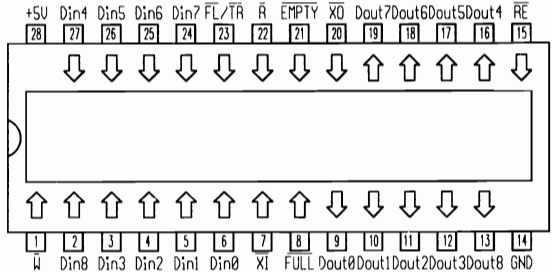
4480 — 16384x4-Bit stat. RAM + 4-BIT Comparator



W	G	CLR	Match	Mode
H	H	H	valid	compare
L	X	H	invalid	write
H	L	H	invalid	read
X	X	L	invalid	flash clear

4480 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 44S80 N-15	Sgs	24-DIP	CMOS	0...+70			<15		TTL-TS
MK 44S80 N-17	Sgs	24-DIP	CMOS	0...+70			<17		TTL-TS
MK 44S80 N-20	Sgs	24-DIP	CMOS	0...+70			<20		TTL-TS
MK 44S80 X-15	Sgs	24-FLAT	CMOS	0...+70			<15		TTL-TS
MK 44S80 X-17	Sgs	24-FLAT	CMOS	0...+70			<17		TTL-TS
MK 44S80 X-20	Sgs	24-FLAT	CMOS	0...+70			<20		TTL-TS

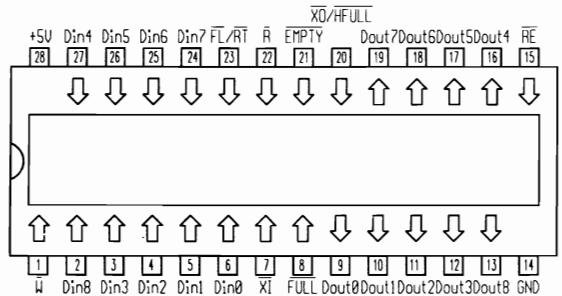
4501 — 512x9-Bit FIFO



4501 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4501 N-10	Tho	28-DIP	CMOS	0...+70	<440	<44	<100		TTL-TS
MK 4501 N-12	Tho	28-DIP	CMOS	0...+70	<440	<44	<120		TTL-TS
MK 4501 N-15	Tho	28-DIP	CMOS	0...+70	<440	<44	<150		TTL-TS
MK 4501 N-20	Tho	28-DIP	CMOS	0...+70	<440	<44	<200		TTL-TS
MK 4501 N-65	Tho	28-DIP	CMOS	0...+70	<440	<44	<65		TTL-TS
MK 4501 N-80	Tho	28-DIP	CMOS	0...+70	<440	<44	<80		TTL-TS
MKB 4501 P-80	Tho	28-DIP	CMOS	-55...+125	<440	<44	<100		TTL-TS
MKB 4501 P-81	Tho	28-DIP	CMOS	-55...+125	<440	<44	<120		TTL-TS

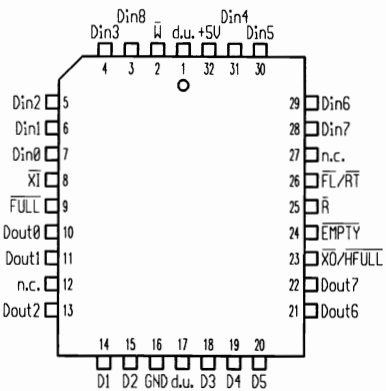
4501 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MKB 4501 P-82	Tho	28-DIP	CMOS	-55...+125	<440	<44	<150		TTL-TS
MKB 4501 P-83	Tho	28-DIP	CMOS	-55...+125	<440	<44	<200		TTL-TS
MKB 4501 P-88	Tho	28-DIP	CMOS	-55...+125	<495	<44	<80		TTL-TS

4501 — 512x9-Bit FIFO



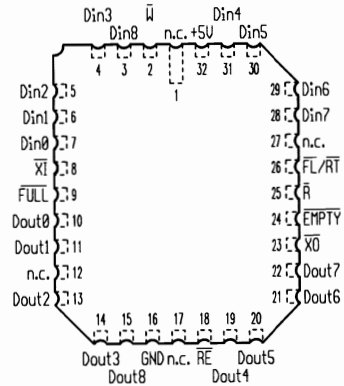
4501 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45H01 N-12	Sgs	28-DIP	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H01 N-25	Sgs	28-DIP	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H01 N-35	Sgs	28-DIP	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H01 N-50	Sgs	28-DIP	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H01 N-65	Sgs	28-DIP	CMOS	0...+70	<660	<66	<65		TTL-TS

4501 — 512x9-Bit FIFO



4501 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45H01 K-12	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H01 K-25	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H01 K-35	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H01 K-50	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H01 K-65	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<65		TTL-TS

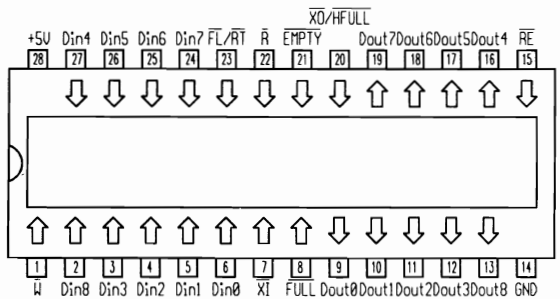
4501 — 512x9-Bit FIFO



4501 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4501 K-10	Sgs	32-PLCC	CMOS	0...+70	<440	<44	<100		TTL-TS
MK 4501 K-12	Sgs	32-PLCC	CMOS	0...+70	<440	<44	<120		TTL-TS
MK 4501 K-15	Sgs	32-PLCC	CMOS	0...+70	<440	<44	<150		TTL-TS
MK 4501 K-20	Sgs	32-PLCC	CMOS	0...+70	<440	<44	<200		TTL-TS
MK 4501 K-65	Sgs	32-PLCC	CMOS	0...+70	<440	<44	<65		TTL-TS
MK 4501 K-80	Sgs	32-PLCC	CMOS	0...+70	<440	<44	<80		TTL-TS
MKB 4501 E-80	Tho	32-LCC	CMOS	-55...+125	<440	<44	<100		TTL-TS
MKB 4501 E-81	Tho	32-LCC	CMOS	-55...+125	<440	<44	<120		TTL-TS

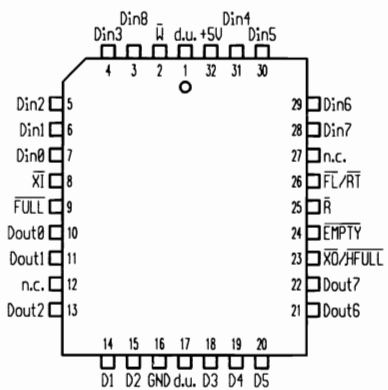
4501 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MKB 4501 E-82	Tho	32-LCC	CMOS	-55...+125	<440	<44	<150		TTL-TS
MKB 4501 E-83	Tho	32-LCC	CMOS	-55...+125	<440	<44	<200		TTL-TS
MKB 4501 E-88	Tho	32-LCC	CMOS	-55...+125	<495	<44	<80		TTL-TS

4502 — **1024x9-Bit FIFO**

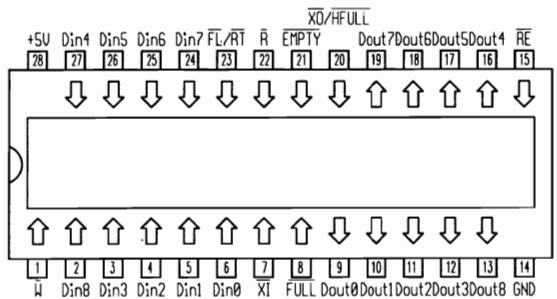


4502 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45H02 N-12	Sgs	28-DIP	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H02 N-25	Sgs	28-DIP	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H02 N-35	Sgs	28-DIP	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H02 N-50	Sgs	28-DIP	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H02 N-65	Sgs	28-DIP	CMOS	0...+70	<660	<66	<65		TTL-TS

4502 — 1024x9-Bit FIFO



4503 — 2048x9-Bit FIFO

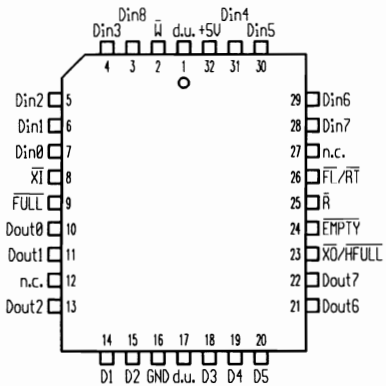


4502 Type	Man	Case	Techn.	T_U °C	P_typ mW	P standby mW	t_aa ns	t_ref ms	Output
					$mW/bit				
MK 45H02 K-12	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H02 K-25	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H02 K-35	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H02 K-50	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H02 K-65	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<65		TTL-TS

4503 Type	Man	Case	Techn.	T_U °C	P_typ mW	P standby mW	t_aa ns	t_ref ms	Output
					$mW/bit				
MK 45H03 N-12	Sgs	28-DIP	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H03 N-25	Sgs	28-DIP	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H03 N-35	Sgs	28-DIP	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H03 N-50	Sgs	28-DIP	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H03 N-65	Sgs	28-DIP	CMOS	0...+70	<660	<66	<65		TTL-TS
MK 4503 N-10	Sgs	28-DIP	CMOS	0...+70	<660	<66	<100		TTL-TS
MK 4503 N-12	Sgs	28-DIP	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 4503 N-15	Sgs	28-DIP	CMOS	0...+70	<660	<66	<150		TTL-TS

4503 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4503 N-20	Sgs	28-DIP	CMOS	0...+70	<660	<66	<200		TTL-TS
MK 4503 N-50	Sgs	28-DIP	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 4503 N-65	Sgs	28-DIP	CMOS	0...+70	<660	<66	<65		TTL-TS
MK 4503 N-80	Sgs	28-DIP	CMOS	0...+70	<660	<66	<80		TTL-TS
MK 45H13 N-12	Sgs	28-TDIP	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H13 N-25	Sgs	28-TDIP	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H13 N-35	Sgs	28-TDIP	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H13 N-50	Sgs	28-TDIP	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H13 N-65	Sgs	28-TDIP	CMOS	0...+70	<660	<66	<65		TTL-TS

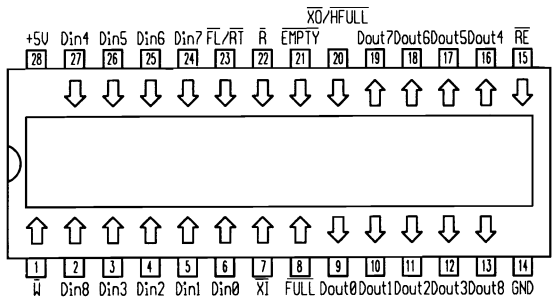
4503 — 2048x9-Bit FIFO



4503 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45H03 K-12	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H03 K-25	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H03 K-35	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H03 K-50	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H03 K-65	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 4503 K-10	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<100		TTL-TS
MK 4503 K-12	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 4503 K-15	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<150		TTL-TS

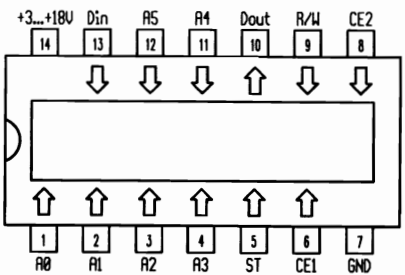
4503 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4503 K-20	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<200		TTL-TS
MK 4503 K-50	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 4503 K-65	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<65		TTL-TS
MK 4503 K-80	Sgs	32-PLCC	CMOS	0...+70	<660	<66	<80		TTL-TS

4504 — 4096x9-Bit FIFO



4504 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45H04 N-12	Sgs	28-DIP	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H04 N-25	Sgs	28-DIP	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H04 N-35	Sgs	28-DIP	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H04 N-50	Sgs	28-DIP	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H04 N-65	Sgs	28-DIP	CMOS	0...+70	<660	<66	<65		TTL-TS

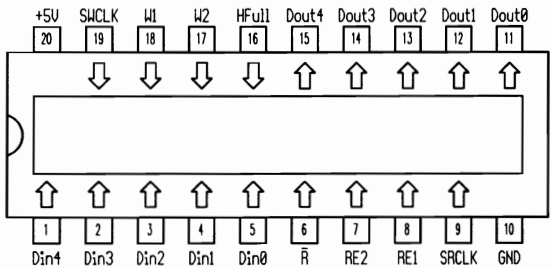
4505 — 64x1-Bit static RAM



Strobe/ CE1/CE2	R/W	D_{out}	Mode
L	L	Hi-Z	disable
H	L	Hi-Z	write
L	H	Hi-Z	disable
H	H	data out	read

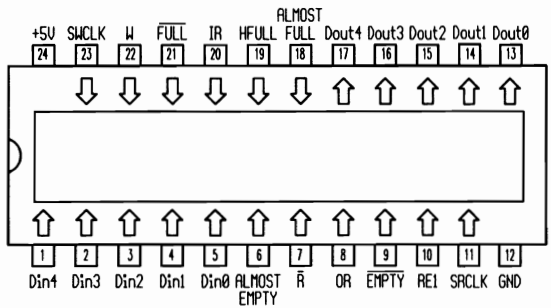
4505 Type	Man	Case	Techn.	T_{vj}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HEF 4505 BD	Val	14-DIC	CMOS	-40...+85	<250µ		<660		TTL-TS
HEF 4505 BD	Val	14-DIC	CMOS	-40...+85	<1		<270		TTL-TS
HEF 4505 BD	Val	14-DIC	CMOS	-40...+85	<3		<200		TTL-TS
HEF 4505 BP	Val	14-DIP	CMOS	-40...+85	<250µ		<660		TTL-TS
HEF 4505 BP	Val	14-DIP	CMOS	-40...+85	<1		<270		TTL-TS
HEF 4505 BP	Val	14-DIP	CMOS	-40...+85	<3		<200		TTL-TS
MCM 14505 AL	Mot	14-DIC	CMOS	-55...+125		<25µ	<750		TTL-TS
MCM 14505 AL	Mot	14-DIC	CMOS	-55...+125		<0,1	<400		TTL-TS
MCM 14505 AL	Mot	14-DIC	CMOS	-55...+125		<0,3	<300		TTL-TS
MCM 14505 CL	Mot	14-DIC	CMOS	-40...+85		<0,25	<750		TTL-TS
MCM 14505 CL	Mot	14-DIC	CMOS	-40...+85		<1	<400		TTL-TS
MCM 14505 CL	Mot	14-DIC	CMOS	-40...+85		<3	<300		TTL-TS
MCM 14505 CP	Mot	14-DIP	CMOS	-40...+85		<0,25	<750		TTL-TS
MCM 14505 CP	Mot	14-DIP	CMOS	-40...+85		<1	<400		TTL-TS
MCM 14505 CP	Mot	14-DIP	CMOS	-40...+85		<3	<300		TTL-TS

4505 — 1024x5-Bit FIFO



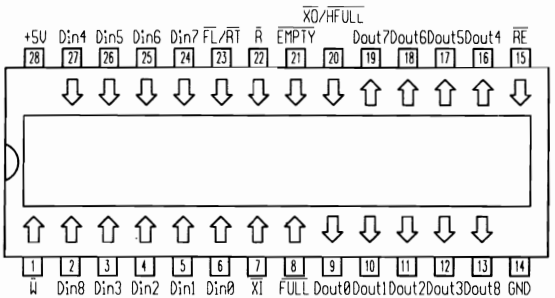
4505 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4505S N-25	Sgs	20-DIP	CMOS	0...+70	<770		<15		TTL-TS
MK 4505S N-33	Sgs	20-DIP	CMOS	0...+70	<770		<20		TTL-TS
MK 4505S N-50	Sgs	20-DIP	CMOS	0...+70	<770		<25		TTL-TS

4505 — 1024x5-Bit FIFO



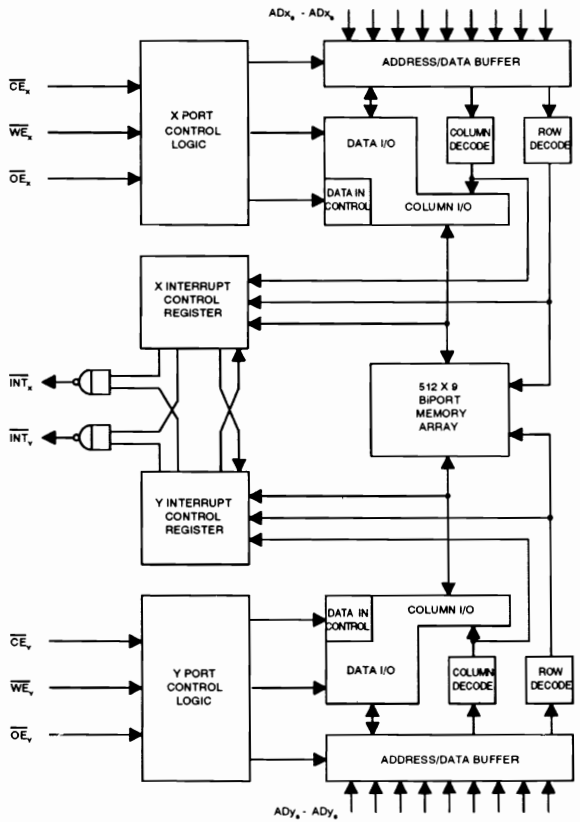
4505 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4505M N-25	Sgs	24-DIP	CMOS	0...+70	<770		<15		TTL-TS
MK 4505M N-33	Sgs	24-DIP	CMOS	0...+70	<770		<20		TTL-TS
MK 4505M N-50	Sgs	24-DIP	CMOS	0...+70	<770		<25		TTL-TS

4508 — 8192x9-Bit FIFO

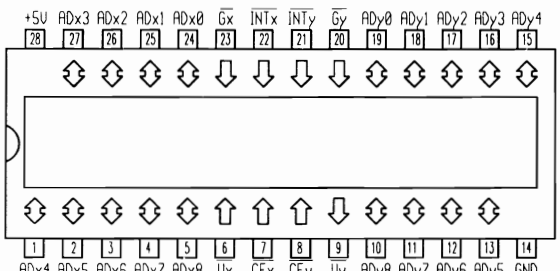


4508 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45H08 N-12	Sgs	28-DIP	CMOS	0...+70	<660	<66	<120		TTL-TS
MK 45H08 N-25	Sgs	28-DIP	CMOS	0...+70	<660	<66	<25		TTL-TS
MK 45H08 N-35	Sgs	28-DIP	CMOS	0...+70	<660	<66	<35		TTL-TS
MK 45H08 N-50	Sgs	28-DIP	CMOS	0...+70	<660	<66	<50		TTL-TS
MK 45H08 N-65	Sgs	28-DIP	CMOS	0...+70	<660	<66	<65		TTL-TS

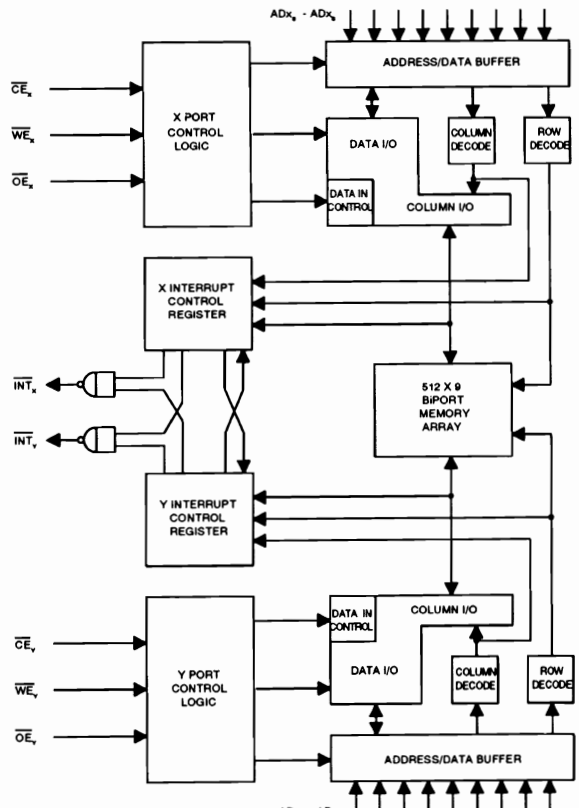
4511 — 512x9-Bit BIPORT RAM



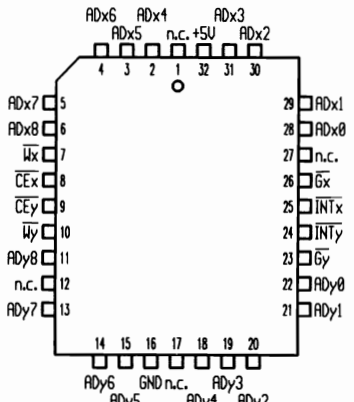
4511 | 512x9-Bit BIPORT-RAM



4511 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4511 N-12	Tho	28-DIP	CMOS	0...+70	<137,5	<5,5	<120		TTL-TS
MK 4511 N-15	Tho	28-DIP	CMOS	0...+70	<137,5	<5,5	<150		TTL-TS
MK 4511 N-20	Tho	28-DIP	CMOS	0...+70	<137,5	<5,5	<200		TTL-TS

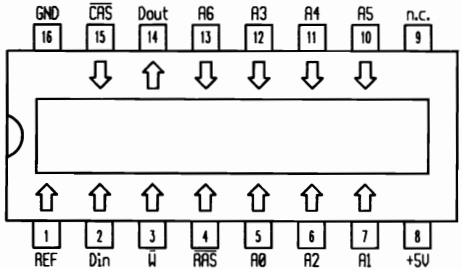


4511 — 512x9-Bit BIPORT-RAM



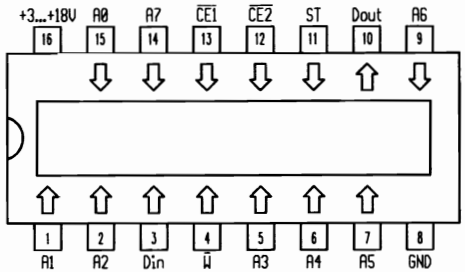
4511 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4511 K-12	Sgs	32-PLCC	CMOS	0...+70	<137,5	<13,75	<120		TTL-TS
MK 4511 K-15	Sgs	32-PLCC	CMOS	0...+70	<137,5	<13,75	<150		TTL-TS
MK 4511 K-20	Sgs	32-PLCC	CMOS	0...+70	<137,5	<13,75	<200		TTL-TS

4516 — 16384x1-Bit dynamic RAM



4516 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4516 J-10	Mos	16-DIC	NMOS	0...+70	<140	<10	<100	<2	TTL-TS
MK 4516 J-12	Mos	16-DIC	NMOS	0...+70	<140	<10	<120	<2	TTL-TS
MK 4516 J-8	Mos	16-DIC	NMOS	0...+70	<140	<10	<80	<2	TTL-TS
MK 4516 N-10	Mos	16-DIP	NMOS	0...+70	<140	<10	<100	<2	TTL-TS
MK 4516 N-12	Mos	16-DIP	NMOS	0...+70	<140	<10	<120	<2	TTL-TS
MK 4516 N-8	Mos	16-DIP	NMOS	0...+70	<140	<10	<80	<2	TTL-TS

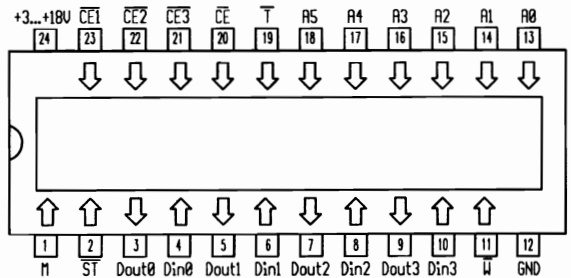
4537 — 256x1-Bit static RAM



CE1	CE2	ST	W	D_{in}	D_{out}	Mode
L	L	L	L	data in	Hi-Z	write
H	L	L	H	X	Hi-Z	read into output Latch
L	L	L	H	X	data out	read

4537 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 14537 AL	Mot	16-DIC	CMOS	-55...+125	<0,5		<4000		TTL-TS
MCM 14537 AL	Mot	16-DIC	CMOS	-55...+125	<2		<1400		TTL-TS
MCM 14537 AL	Mot	16-DIC	CMOS	-55...+125	<6		<1050		TTL-TS
MCM 14537 CL	Mot	16-DIC	CMOS	-40...+85	<0,5		<6000		TTL-TS
MCM 14537 CL	Mot	16-DIC	CMOS	-40...+85	<2		<2000		TTL-TS
MCM 14537 CL	Mot	16-DIC	CMOS	-40...+85	<6		<1500		TTL-TS

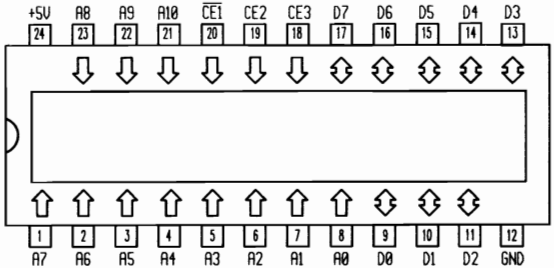
4552 — 64x4-Bit static RAM



CE1	CE2	CE3	T	L	M	ST	W	D_{in}	D_{out}	Mode
L	L	L	X	X	X	L	L	data in	Hi-Z	write
L	L	L	X	L	X	L	X	X	Hi-Z	read into output Latch
L	L	L	L	X	X	X	H	X	data out	read
X	X	X	L	X	H	X	X	X	H	read or write / Dout active

4552 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 14552 AL	Mot	24-DIC	CMOS	-55...+125	<0,025		<3000		TTL-TS
MCM 14552 AL	Mot	24-DIC	CMOS	-55...+125	<0,1		<1050		TTL-TS
MCM 14552 AL	Mot	24-DIC	CMOS	-55...+125	<0,3		<800		TTL-TS
MCM 14552 CL	Mot	24-DIC	CMOS	-40...+85	<0,25		<6000		TTL-TS
MCM 14552 CL	Mot	24-DIC	CMOS	-40...+85	<1		<2100		TTL-TS
MCM 14552 CL	Mot	24-DIC	CMOS	-40...+85	<3		<1600		TTL-TS
MCM 14552 CP	Mot	24-DIP	CMOS	-40...+85	<0,25		<6000		TTL-TS
MCM 14552 CP	Mot	24-DIP	CMOS	-40...+85	<1		<2100		TTL-TS
MCM 14552 CP	Mot	24-DIP	CMOS	-40...+85	<3		<1600		TTL-TS

4615 — 2048x8-Bit EEPROM

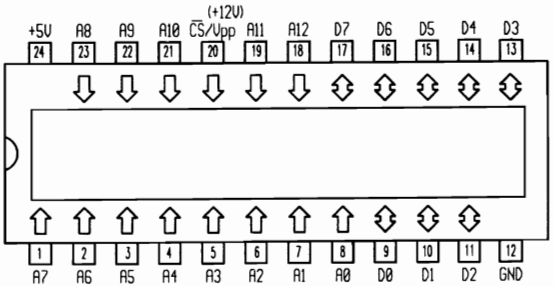


$\overline{CS1}$	CS2	CS3	D_n	Mode
L	H	H	data out	read
<+6V	L	X	Hi-Z	standby
H	X	X	Hi-Z	standby
<+6V	X	L	Hi-Z	standby
V_{pp}	L	X	data in	byte write
V_{pp}	H	X	Hi-Z	chip reset

V_{PP}10,8...20,5V

4615 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLM 46C15 C-70	Exl	24-DIC	CMOS	-55...+125	<550	<247,5	<70		TTL-TS
XLM 46C15 C-85	Exl	24-DIC	CMOS	-55...+125	<550	<247,5	<85		TTL-TS
XLS 46C15 C-55	Exl	24-DIC	CMOS	0...+70	<495	<247,5	<55		TTL-TS
XLS 46C15 C-60	Exl	24-DIC	CMOS	0...+70	<495	<247,5	<60		TTL-TS
XLS 46C15 C-70	Exl	24-DIC	CMOS	0...+70	<495	<247,5	<70		TTL-TS
XLS 46C15 C-85	Exl	24-DIC	CMOS	0...+70	<495	<247,5	<85		TTL-TS
XLS 46C15 P-55	Exl	24-DIP	CMOS	0...+70	<495	<247,5	<55		TTL-TS
XLS 46C15 P-60	Exl	24-DIP	CMOS	0...+70	<495	<247,5	<60		TTL-TS
XLS 46C15 P-70	Exl	24-DIP	CMOS	0...+70	<495	<247,5	<70		TTL-TS
XLS 46C15 P-85	Exl	24-DIP	CMOS	0...+70	<495	<247,5	<85		TTL-TS

4664 — 8192x8-Bit EEPROM



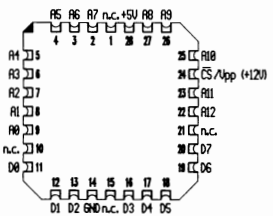
CS/V_{pp}	A10	D_n	Mode
L	X	data out	read
+12V	X	data in	program
L	X	data out	verify
+12V	+12V	Hi-Z	chip reset
H	X	Hi-Z	standby

4664 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLE 46HC64 C-45	Exl	24-DIC	CMOS	-40...+85	<412,5	<192,5	<45		TTL-TS
XLE 46HC64 C-55	Exl	24-DIC	CMOS	-40...+85	<412,5	<192,5	<55		TTL-TS
XLE 46HC64 C-70	Exl	24-DIC	CMOS	-40...+85	<412,5	<192,5	<70		TTL-TS
XLE 46HC64 C-85	Exl	24-DIC	CMOS	-40...+85	<412,5	<192,5	<85		TTL-TS
XLE 46HC64L C-55	Exl	24-DIC	CMOS	-40...+85	<412,5	<11	<55		TTL-TS
XLE 46HC64L C-70	Exl	24-DIC	CMOS	-40...+85	<412,5	<11	<70		TTL-TS
XLE 46HC64L C-85	Exl	24-DIC	CMOS	-40...+85	<412,5	<11	<85		TTL-TS
XLE 46HC64L P3-55	Exl	24-TDIP	CMOS	-40...+85	<412,5	<11	<55		TTL-TS

4664 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLE 46HC64L P3-70	Exl	24-TDIP	CMOS	-40...+85	<412,5	<11	<70		TTL-TS
XLE 46HC64L P3-85	Exl	24-TDIP	CMOS	-40...+85	<412,5	<11	<85		TTL-TS
XLE 46HC64L P-55	Exl	24-DIP	CMOS	-40...+85	<412,5	<11	<55		TTL-TS
XLE 46HC64L P-70	Exl	24-DIP	CMOS	-40...+85	<412,5	<11	<70		TTL-TS
XLE 46HC64L P-85	Exl	24-DIP	CMOS	-40...+85	<412,5	<11	<85		TTL-TS
XLE 46HC64 P3-45	Exl	24-TDIP	CMOS	-40...+85	<412,5	<192,5	<45		TTL-TS
XLE 46HC64 P3-55	Exl	24-TDIP	CMOS	-40...+85	<412,5	<192,5	<55		TTL-TS
XLE 46HC64 P3-70	Exl	24-TDIP	CMOS	-40...+85	<412,5	<192,5	<70		TTL-TS
XLE 46HC64 P3-85	Exl	24-TDIP	CMOS	-40...+85	<412,5	<192,5	<85		TTL-TS
XLE 46HC64 P-45	Exl	24-DIP	CMOS	-40...+85	<412,5	<192,5	<45		TTL-TS
XLE 46HC64 P-55	Exl	24-DIP	CMOS	-40...+85	<412,5	<192,5	<55		TTL-TS
XLE 46HC64 P-70	Exl	24-DIP	CMOS	-40...+85	<412,5	<192,5	<70		TTL-TS
XLE 46HC64 P-85	Exl	24-DIP	CMOS	-40...+85	<412,5	<192,5	<85		TTL-TS
XLM 46HC64 C-45	Exl	24-DIC	CMOS	-55...+125	<412,5	<192,5	<45		TTL-TS
XLM 46HC64 C-55	Exl	24-DIC	CMOS	-55...+125	<412,5	<192,5	<55		TTL-TS
XLM 46HC64 C-70	Exl	24-DIC	CMOS	-55...+125	<412,5	<192,5	<70		TTL-TS
XLM 46HC64 C-85	Exl	24-DIC	CMOS	-55...+125	<412,5	<192,5	<85		TTL-TS
XLM 46HC64L C-55	Exl	24-DIC	CMOS	-55...+125	<412,5	<11	<55		TTL-TS
XLM 46HC64L C-70	Exl	24-DIC	CMOS	-55...+125	<412,5	<11	<70		TTL-TS
XLM 46HC64L C-85	Exl	24-DIC	CMOS	-55...+125	<412,5	<11	<85		TTL-TS
XLS 46HC64 C-35	Exl	24-DIC	CMOS	0...+70	<412,5	<192,5	<35		TTL-TS
XLS 46HC64 C-45	Exl	24-DIC	CMOS	0...+70	<412,5	<192,5	<45		TTL-TS
XLS 46HC64 C-55	Exl	24-DIC	CMOS	0...+70	<412,5	<192,5	<55		TTL-TS
XLS 46HC64 C-70	Exl	24-DIC	CMOS	0...+70	<412,5	<192,5	<70		TTL-TS
XLS 46HC64L C-45	Exl	24-DIC	CMOS	0...+70	<412,5	<11	<45		TTL-TS
XLS 46HC64L C-55	Exl	24-DIC	CMOS	0...+70	<412,5	<11	<55		TTL-TS
XLS 46HC64L C-70	Exl	24-DIC	CMOS	0...+70	<412,5	<11	<70		TTL-TS
XLS 46HC64L P3-45	Exl	24-TDIP	CMOS	0...+70	<412,5	<11	<45		TTL-TS
XLS 46HC64L P3-55	Exl	24-TDIP	CMOS	0...+70	<412,5	<11	<55		TTL-TS
XLS 46HC64L P3-70	Exl	24-TDIP	CMOS	0...+70	<412,5	<11	<70		TTL-TS
XLS 46HC64L P-45	Exl	24-DIP	CMOS	0...+70	<412,5	<11	<45		TTL-TS
XLS 46HC64L P-55	Exl	24-DIP	CMOS	0...+70	<412,5	<11	<55		TTL-TS
XLS 46HC64L P-70	Exl	24-DIP	CMOS	0...+70	<412,5	<11	<70		TTL-TS
XLS 46HC64 P3-35	Exl	24-TDIP	CMOS	0...+70	<412,5	<192,5	<35		TTL-TS
XLS 46HC64 P3-45	Exl	24-TDIP	CMOS	0...+70	<412,5	<192,5	<45		TTL-TS
XLS 46HC64 P-35	Exl	24-DIP	CMOS	0...+70	<412,5	<192,5	<35		TTL-TS
XLS 46HC64 P3-55	Exl	24-TDIP	CMOS	0...+70	<412,5	<192,5	<55		TTL-TS

4664 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLS 46HC64 P3-70	Exl	24-TDIP	CMOS	0...+70	<412,5	<192,5	<70		TTL-TS
XLS 46HC64 P-45	Exl	24-DIP	CMOS	0...+70	<412,5	<192,5	<45		TTL-TS
XLS 46HC64 P-55	Exl	24-DIP	CMOS	0...+70	<412,5	<192,5	<55		TTL-TS
XLS 46HC64 P-70	Exl	24-DIP	CMOS	0...+70	<412,5	<192,5	<70		TTL-TS

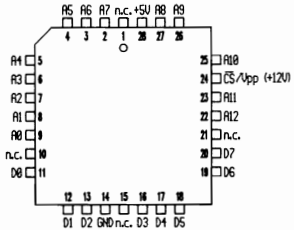
4664 — 8192x8-Bit EEPROM



CS/V_{pp}	A10	D_n	Mode
L	X	data out	read
+12V	X	data in	program
L	X	data out	verify
+12V	+12V	Hi-Z	chip reset
H	X	Hi-Z	standby

4664 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLM 46HC64 L-45	Exl	28-LCC	CMOS	-55...+125	<412,5	<192,5	<45		TTL-TS
XLM 46HC64 L-55	Exl	28-LCC	CMOS	-55...+125	<412,5	<192,5	<55		TTL-TS
XLM 46HC64 L-70	Exl	28-LCC	CMOS	-55...+125	<412,5	<192,5	<70		TTL-TS
XLM 46HC64 L-85	Exl	28-LCC	CMOS	-55...+125	<412,5	<192,5	<85		TTL-TS
XLM 46HC64L L-55	Exl	28-LCC	CMOS	-55...+125	<412,5	<11	<55		TTL-TS
XLM 46HC64L L-70	Exl	28-LCC	CMOS	-55...+125	<412,5	<11	<70		TTL-TS
XLM 46HC64L L-85	Exl	28-LCC	CMOS	-55...+125	<412,5	<11	<85		TTL-TS

4664 — 8192x8-Bit EEPROM

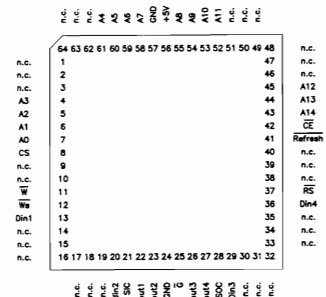


CS/V_{pp}	A10	D_n	Mode
L	X	data out	read
+12V	X	data in	program
L	X	data out	verify
+12V	+12V	Hi-Z	chip reset
H	X	Hi-Z	standby

4664 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLE 46HC64 D-45	Exl	28-PLCC	CMOS	-40...+85	<412,5	<192,5	<45		TTL-TS
XLE 46HC64 D-55	Exl	28-PLCC	CMOS	-40...+85	<412,5	<192,5	<55		TTL-TS
XLE 46HC64 D-70	Exl	28-PLCC	CMOS	-40...+85	<412,5	<192,5	<70		TTL-TS
XLE 46HC64 D-85	Exl	28-PLCC	CMOS	-40...+85	<412,5	<192,5	<85		TTL-TS
XLE 46HC64L D-55	Exl	28-PLCC	CMOS	-40...+85	<412,5	<11	<55		TTL-TS
XLE 46HC64L D-70	Exl	28-PLCC	CMOS	-40...+85	<412,5	<11	<70		TTL-TS
XLE 46HC64L D-85	Exl	28-PLCC	CMOS	-40...+85	<412,5	<11	<85		TTL-TS
XLS 46HC64 D-35	Exl	28-PLCC	CMOS	0...+70	<412,5	<192,5	<35		TTL-TS

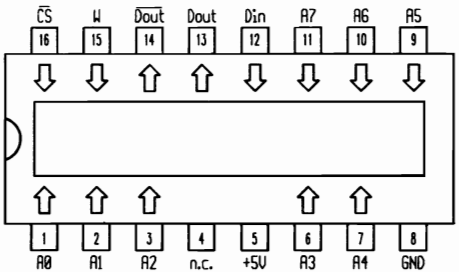
4664 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
XLS 46HC64 D-45	Exl	28-PLCC	CMOS	0...+70	<412,5	<192,5	<45		TTL-TS
XLS 46HC64 D-55	Exl	28-PLCC	CMOS	0...+70	<412,5	<192,5	<55		TTL-TS
XLS 46HC64 D-70	Exl	28-PLCC	CMOS	0...+70	<412,5	<192,5	<70		TTL-TS

4701 — 327680 words x 4-Bit dynam. Video-RAM



4701 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 4701	Mat	64-PLCC	NMOS	0...+70	<825	<110	<240	<2	TTL

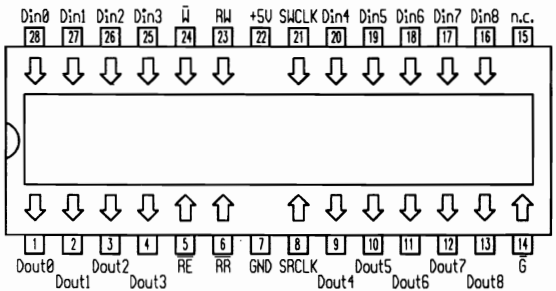
4720 — 256x1-Bit static RAM



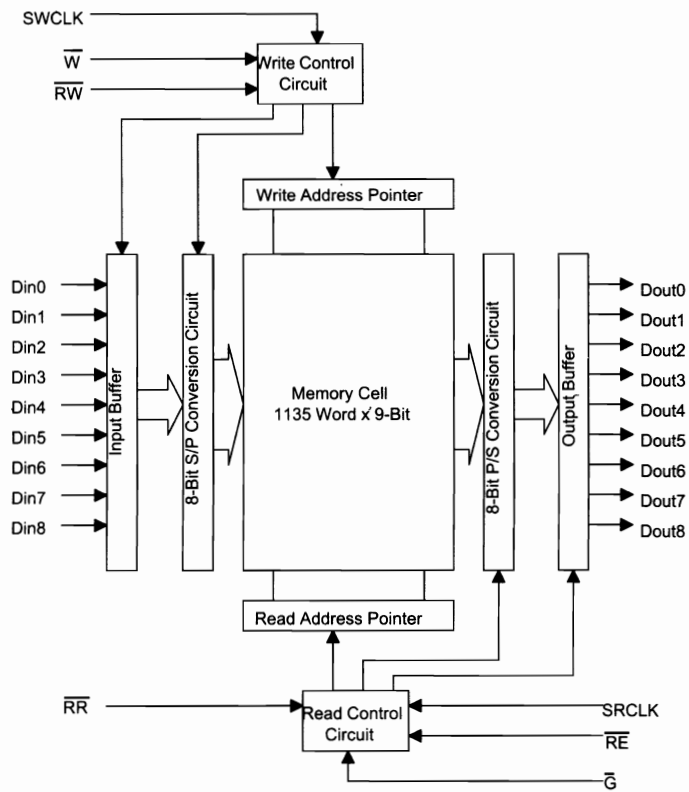
$\overline{CS}$	W	D_{out}	$\overline{D_{out}}$	Mode
L	H	Hi-Z	Hi-Z	write
L	L	data out	data out	read
H	X	Hi-Z	HI-Z	not selected

4720 Type	Man	Case	Techn.	T_{vj}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HEF 4720 BD	Val	16-DIC	CMOS	-40...+85	<10		<580		TTL-TS
HEF 4720 BD	Val	16-DIC	CMOS	-40...+85	<40		<220		TTL-TS
HEF 4720 BD	Val	16-DIC	CMOS	-40...+85	<150		<160		TTL-TS
HEF 4720 BP	Val	16-DIP	CMOS	-40...+85	<10		<580		TTL-TS
HEF 4720 BP	Val	16-DIP	CMOS	-40...+85	<40		<220		TTL-TS
HEF 4720 BP	Val	16-DIP	CMOS	-40...+85	<150		<160		TTL-TS
HEF 4720 BT	Val	16-FLAT	CMOS	-40...+85	<10		<580		TTL-TS
HEF 4720 BT	Val	16-FLAT	CMOS	-40...+85	<40		<220		TTL-TS
HEF 4720 BT	Val	16-FLAT	CMOS	-40...+85	<150		<160		TTL-TS
HEF 4720 VD	Val	16-DIC	CMOS	-40...+85	<10		<580		TTL-TS
HEF 4720 VD	Val	16-DIC	CMOS	-40...+85	<40		<220		TTL-TS
HEF 4720 VP	Val	16-DIP	CMOS	-40...+85	<10		<580		TTL-TS
HEF 4720 VP	Val	16-DIP	CMOS	-40...+85	<40		<220		TTL-TS
HEF 4720 VT	Val	16-FLAT	CMOS	-40...+85	<10		<580		TTL-TS
HEF 4720 VT	Val	16-FLAT	CMOS	-40...+85	<40		<220		TTL-TS

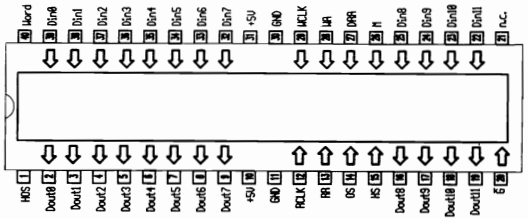
4760 — 1135 words x 9-Bit Digital Video RAM

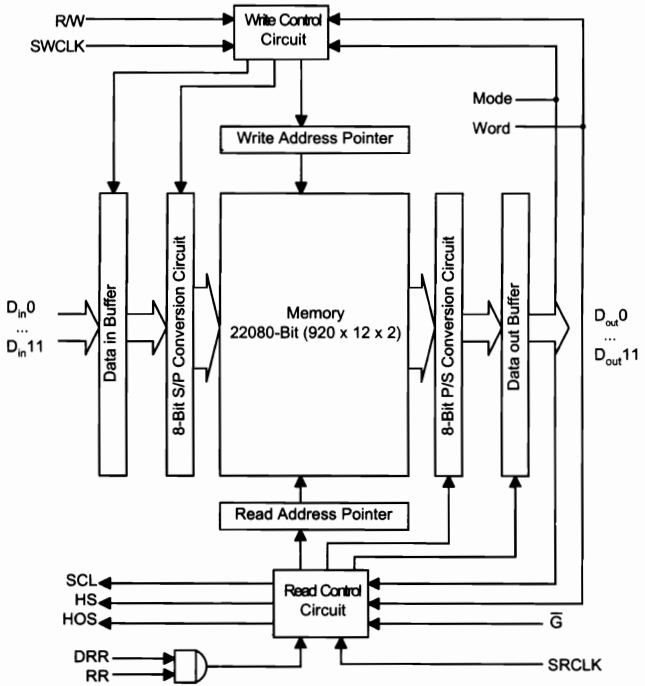


4760 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
MN 4760	Mat	28-DIP	CMOS	0...+70	<440	<50		TTL



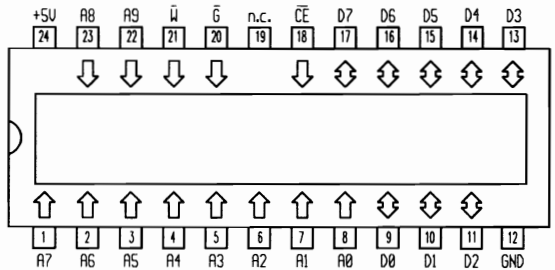
4780 — 920 words x 12-Bit x 2 Digital Video RAM





4780 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 4780 A	Mat	40-TDIP	CMOS	0...+70	<495				TTL

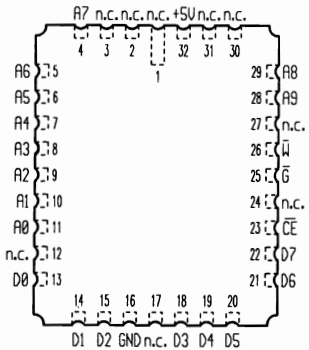
4801 — 1024x8-Bit static RAM



$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

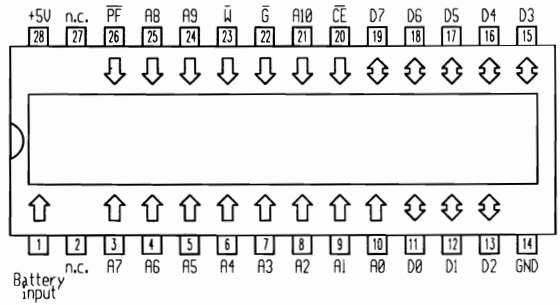
4801 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4801 JA-1	Tho	24-DIC	NMOS	0...+70	<440		<120		TTL-TS
MK 4801 JA-2	Tho	24-DIC	NMOS	0...+70	<440		<150		TTL-TS
MK 4801 JA-3	Tho	24-DIC	NMOS	0...+70	<440		<200		TTL-TS
MK 4801 JA-4	Tho	24-DIC	NMOS	0...+70	<440		<250		TTL-TS
MK 4801 JA-55	Tho	24-DIC	NMOS	0...+70	<687,5		<55		TTL-TS
MK 4801 JA-70	Tho	24-DIC	NMOS	0...+70	<687,5		<70		TTL-TS
MK 4801 JA-90	Tho	24-DIC	NMOS	0...+70	<687,5		<90		TTL-TS
MK 4801 NA-1	Tho	24-DIP	NMOS	0...+70	<440		<120		TTL-TS
MK 4801 NA-2	Tho	24-DIP	NMOS	0...+70	<440		<150		TTL-TS
MK 4801 NA-3	Tho	24-DIP	NMOS	0...+70	<440		<200		TTL-TS
MK 4801 NA-4	Tho	24-DIP	NMOS	0...+70	<440		<250		TTL-TS
MK 4801 PA-1	Tho	24-DIC	NMOS	0...+70	<440		<120		TTL-TS
MK 4801 PA-2	Tho	24-DIC	NMOS	0...+70	<440		<150		TTL-TS
MK 4801 PA-3	Tho	24-DIC	NMOS	0...+70	<440		<200		TTL-TS
MK 4801 PA-4	Tho	24-DIC	NMOS	0...+70	<440		<250		TTL-TS
MK 4801 PA-55	Tho	24-DIC	NMOS	0...+70	<687,5		<55		TTL-TS
MK 4801 PA-70	Tho	24-DIC	NMOS	0...+70	<687,5		<70		TTL-TS
MK 4801 PA-90	Tho	24-DIC	NMOS	0...+70	<687,5		<90		TTL-TS
MKB 4801A J81	Tho	24-DIC	NMOS	-55...+125	<660		<120		TTL-TS
MKB 4801A J82	Tho	24-DIC	NMOS	-55...+125	<660		<150		TTL-TS
MKB 4801A J83	Tho	24-DIC	NMOS	-55...+125	<660		<200		TTL-TS
MKB 4801A J870	Tho	24-DIC	NMOS	-55...+125	<660		<70		TTL-TS
MKB 4801A J890	Tho	24-DIC	NMOS	-55...+125	<660		<90		TTL-TS
MKB 4801A P81	Tho	24-DIP	NMOS	-55...+125	<660		<120		TTL-TS
MKB 4801A P82	Tho	24-DIP	NMOS	-55...+125	<660		<150		TTL-TS
MKB 4801A P83	Tho	24-DIP	NMOS	-55...+125	<660		<200		TTL-TS
MKB 4801A P870	Tho	24-DIP	NMOS	-55...+125	<660		<70		TTL-TS
MKB 4801A P890	Tho	24-DIP	NMOS	-55...+125	<660		<90		TTL-TS

4801 — 1024x8-Bit static RAM



CE	G	W	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

4802 — 2048x8-Bit static RAM

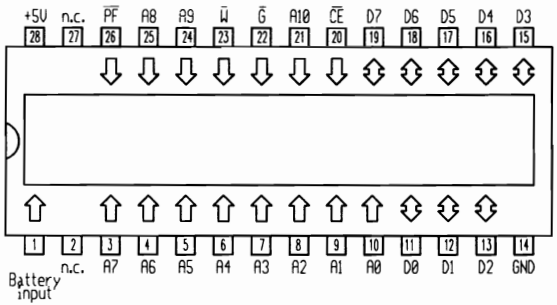


CE	G	W	V_{CC}	D_n	Power	Mode
H	X	X	≧4,75V ≦5,5V	Hi-Z	standby	deselect
L	X	L	≧4,75V ≦5,5V	data in	active	write
L	L	H	≧4,75V ≦5,5V	data out	active	read
L	H	H	≧4,75V ≦5,5V	Hi-Z	active	read
X	X	X	<4,5V	Hi-Z	CMOS standby	write protect

4801 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MKB 4801A E81	Tho	32-LCC	NMOS	-55...+125	<660		<120		TTL-TS
MKB 4801A E82	Tho	32-LCC	NMOS	-55...+125	<660		<150		TTL-TS
MKB 4801A E83	Tho	32-LCC	NMOS	-55...+125	<660		<200		TTL-TS
MKB 4801A E870	Tho	32-LCC	NMOS	-55...+125	<660		<70		TTL-TS
MKB 4801A E890	Tho	32-LCC	NMOS	-55...+125	<660		<90		TTL-TS

4802 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48C02 LN-15	Tho	28-DIP	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48C02 LN-20	Tho	28-DIP	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48C02 LN-25	Tho	28-DIP	CMOS	0...+70	<440	<16,5	<250		TTL-TS
MK 48C02 N-15	Tho	28-DIP	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48C02 N-20	Tho	28-DIP	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48C02 N-25	Tho	28-DIP	CMOS	0...+70	<440	<16,5	<250		TTL-TS

4802 — 2048x8-Bit static RAM Zeropower

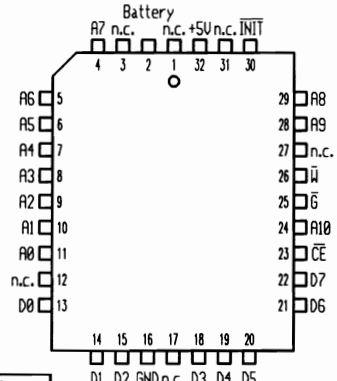


CE	G	W	Vcc	Dn	Mode
H	X	X	≥4,75V ≤5,5V*	Hi-Z	deselect
L	X	L	≥4,75V ≤5,5V*	data in	write
L	L	H	≥4,75V ≤5,5V*	data out	read
L	H	H	≥4,75V ≤5,5V*	Hi-Z	read
X	X	X	≤4,5V >3V**	Hi-Z	power fail deselect
X	X	X	≤3V	Hi-Z	Battery backup

* MK 4812 ≥4,5V ≤5,5V ** MK 4812 ≤4,2V >3V

4802 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
MK 48C02 AN-15	Sgs	28-DIP	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48C02 AN-20	Sgs	28-DIP	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48C02 AN-25	Sgs	28-DIP	CMOS	0...+70	<440	<16,5	<250		TTL-TS
MK 48C12 AN-15	Sgs	28-DIP	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48C12 AN-20	Sgs	28-DIP	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48C12 AN-25	Sgs	28-DIP	CMOS	0...+70	<440	<16,5	<250		TTL-TS

4802 — 2048x8-Bit static RAM Zeropower

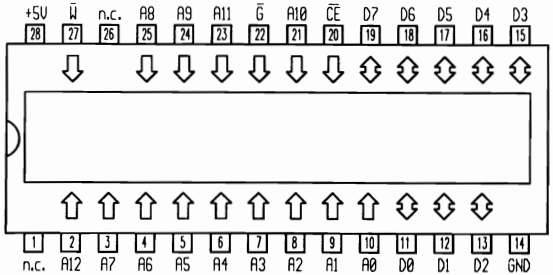


CE	G	W	Vcc	Dn	Mode
H	X	X	≥4,75V ≤5,5V*	Hi-Z	deselect
L	X	L	≥4,75V ≤5,5V*	data in	write
L	L	H	≥4,75V ≤5,5V*	data out	read
L	H	H	≥4,75V ≤5,5V*	Hi-Z	read
X	X	X	≤4,5V >3V**	Hi-Z	power fail deselect
X	X	X	≤3V	Hi-Z	Battery backup

* MK 4812 ≥4,5V ≤5,5V ** MK 4812 ≤4,2V >3V

4802 Typ · Type · Tipo	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
MK 48C02 AK-15	Sgs	32-PLCC	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48C02 AK-20	Sgs	32-PLCC	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48C02 AK-25	Sgs	32-PLCC	CMOS	0...+70	<440	<16,5	<250		TTL-TS
MK 48C12 AK-15	Sgs	32-PLCC	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48C12 AK-20	Sgs	32-PLCC	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48C12 AK-25	Sgs	32-PLCC	CMOS	0...+70	<440	<16,5	<250		TTL-TS

4808 — 8192x8-Bit static RAM Zeropower

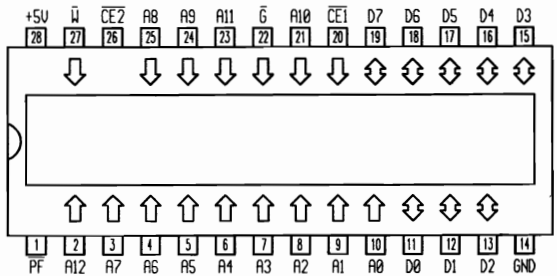


$\overline{CE}$	$\overline{G}$	$\overline{W}$	V_{CC}	D_n	Power	Mode
H	X	X	≥4,75V ≤5,5V	Hi-Z	standby	deselect
L	X	L	≥4,75V ≤5,5V	data in	active	write
L	L	H	≥4,75V ≤5,5V	data out	active	read
L	H	H	≥4,75V ≤5,5V	Hi-Z	active	read
X	X	X	>3V <4,75V	Hi-Z	CMOS standby	write protect
X	X	X	≤3V	Hi-Z	Battery backup	deselect

4808 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48T08 B-10	Sgs	28-DIP	CMOS	0...+70	<440	<27,5	<100		TTL-TS
MK 48T08 B-12	Sgs	28-DIP	CMOS	0...+70	<440	<27,5	<120		TTL-TS
MK 48T08 B-15	Sgs	28-DIP	CMOS	0...+70	<440	<27,5	<150		TTL-TS
MK 48T08 B-20	Sgs	28-DIP	CMOS	0...+70	<440	<27,5	<200		TTL-TS
MK 48Z08 B-15	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<150		TTL-TS
MK 48Z08 B-20	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<200		TTL-TS
MK 48Z08 B-25	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<250		TTL-TS
MK 48Z08 B-55	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<55		TTL-TS

4808 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48Z08 B-70	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<70		TTL-TS
MK 48Z18 B-15	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<150		TTL-TS
MK 48Z18 B-20	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<200		TTL-TS
MK 48Z18 B-25	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<250		TTL-TS
MK 48Z18 B-55	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<55		TTL-TS
MK 48Z18 B-70	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<70		TTL-TS

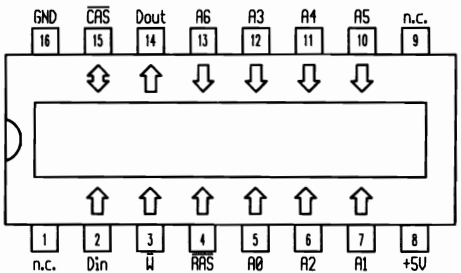
4809 — 8192x8-Bit static RAM Zeropower



$\overline{CE1}$	CE2	$\overline{G}$	$\overline{W}$	V_{CC}	D_n	Power	Mode
H	X	X	X	≧4,75V ≦5,5V	Hi-Z	standby	deselect
X	L	X	X	≧4,75V ≦5,5V	Hi-Z	standby	deselect
L	H	X	L	≧4,75V ≦5,5V	data in	active	write
L	H	L	H	≧4,75V ≦5,5V	data out	active	read
L	H	H	H	≧4,75V ≦5,5V	Hi-Z	active	read
X	X	X	X	<4,75V >3V	Hi-Z	CMOS standby	deselect
X	X	X	X	≦3V	Hi-Z	Battery backup	deselect

4809 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48Z09 B-15	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<150		TTL-TS
MK 48Z09 B-20	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<200		TTL-TS
MK 48Z09 B-25	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<250		TTL-TS
MK 48Z09 B-55	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<55		TTL-TS
MK 48Z09 B-70	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<70		TTL-TS
MK 48Z19 B-15	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<150		TTL-TS
MK 48Z19 B-20	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<200		TTL-TS
MK 48Z19 B-25	Sgs	28-DIP	CMOS	0...+70	<275	<16,5	<250		TTL-TS
MK 48Z19 B-55	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<55		TTL-TS
MK 48Z19 B-70	Sgs	28-DIP	CMOS	0...+70	<687,5	<16,5	<70		TTL-TS

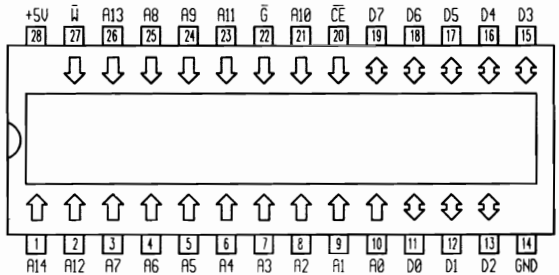
4816 — 16384x1-Bit dynamic RAM



4816 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
C 2118-10	Int	16-DIC	NMOS	0...+70	<148	<22	<100	<2	TTL-TS
C 2118-12	Int	16-DIC	NMOS	0...+70	<148	<22	<120	<2	TTL-TS
C 2118-15	Int	16-DIC	NMOS	0...+70	<148	<22	<150	<2	TTL-TS
C 2118-3	Int	16-DIC	NMOS	0...+70	<150	<11	<100	<2	TTL-TS
C 2118-4	Int	16-DIC	NMOS	0...+70	<137	<11	<120	<2	TTL-TS
C 2118-7	Int	16-DIC	NMOS	0...+70	<126	<11	<150	<2	TTL-TS
HM 4816 A-3	Hit	16-DIC	NMOS	0...+70	<150	<11	<100	<2	TTL-TS
HM 4816 A-3E	Hit	16-DIC	NMOS	0...+70	<150	<11	<105	<2	TTL-TS

4816 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 4816 A-4	Hit	16-DIC	NMOS	0...+70	<137	<11	<120	<2	TTL-TS
HM 4816 A-7	Hit	16-DIC	NMOS	0...+70	<126	<11	<150	<2	TTL-TS
HM 4816 AP-3	Hit	16-DIP	NMOS	0...+70	<150	<11	<100	<2	TTL-TS
HM 4816 AP-3E	Hit	16-DIP	NMOS	0...+70	<150	<11	<105	<2	TTL-TS
HM 4816 AP-4	Hit	16-DIP	NMOS	0...+70	<137	<11	<120	<2	TTL-TS
HM 4816 AP-7	Hit	16-DIP	NMOS	0...+70	<126	<11	<150	<2	TTL-TS
MB 8118-10	Fui	16-DIP	NMOS	0...+70	<181	<16,5	<100	<2	TTL-TS
MB 8118-12	Fui	16-DIP	NMOS	0...+70	<181	<16,5	<120	<2	TTL-TS
MCM 4517 C-10	Mot	16-DIC	NMOS	0...+70	<150	<14	<100	<2	TTL-TS
MCM 4517 C-12	Mot	16-DIC	NMOS	0...+70	<150	<14	<120	<2	TTL-TS
MCM 4517 C-15	Mot	16-DIC	NMOS	0...+70	<150	<14	<150	<2	TTL-TS
MCM 4517 C-20	Mot	16-DIC	NMOS	0...+70	<150	<14	<200	<2	TTL-TS
MCM 4517 P-10	Mot	16-DIP	NMOS	0...+70	<150	<14	<100	<2	TTL-TS
MCM 4517 P-12	Mot	16-DIP	NMOS	0...+70	<150	<14	<120	<2	TTL-TS
MCM 4517 P-15	Mot	16-DIP	NMOS	0...+70	<150	<14	<150	<2	TTL-TS
MCM 4517 P-20	Mot	16-DIP	NMOS	0...+70	<150	<14	<200	<2	TTL-TS
NMC 5295-2	Nsc	16-DIP	NMOS	0...+70	<192	<22	<80	<2	TTL-TS
NMC 5295-3	Nsc	16-DIP	NMOS	0...+70	<192	<22	<100	<2	TTL-TS
NMC 5295-4	Nsc	16-DIP	NMOS	0...+70	<192	<22	<120	<2	TTL-TS

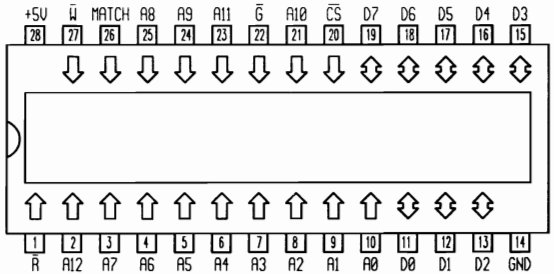
4830 — 32768x8-Bit static RAM Zeropower



$\overline{CE}$	$\overline{G}$	$\overline{W}$	V_{CC}	D_n	Power	Mode
H	X	X	≧4,75V ≦5,5V	Hi-Z	standby	deselect
L	X	L	≧4,75V ≦5,5V	data in	active	write
L	L	H	≧4,75V ≦5,5V	data out	active	read
L	H	H	≧4,75V ≦5,5V	Hi-Z	active	read
X	X	X	>3V <4,75V	Hi-Z	CMOS standby	write protect
X	X	X	≦3V	Hi-Z	Battery backup	deselect

4830 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48Z30A B-10	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<100		TTL-TS
MK 48Z30A B-12	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<120		TTL-TS
MK 48Z30A B-15	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<150		TTL-TS
MK 48Z30 B-10	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<100		TTL-TS
MK 48Z30 B-12	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<120		TTL-TS
MK 48Z30 B-15	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<150		TTL-TS
MK 48Z32A B-10	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<100		TTL-TS
MK 48Z32A B-12	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<120		TTL-TS
MK 48Z32A B-15	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<150		TTL-TS
MK 48Z32 B-10	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<100		TTL-TS
MK 48Z32 B-12	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<120		TTL-TS
MK 48Z32 B-15	Sgs	28-DIP	CMOS	0...+70	<495	<16,5	<150		TTL-TS

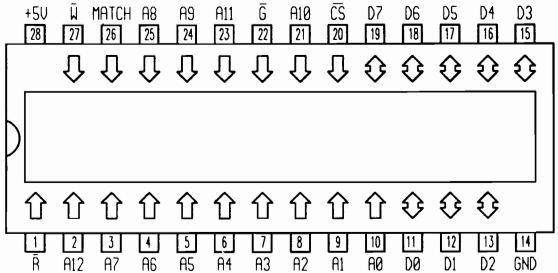
4874 — 8192x8-Bit Stat. RAM w. 8-Bit Comparator



CE	G	W	CLR	D_{out}	Power	Mode
H	X	X	X	Hi-Z	standby	deselect
L	X	L	H	data in	active	write
L	L	H	H	data out	active	read
L	H	H	H	Hi-Z	active	read
L	X	L	L	Hi-Z	active	flash clear
L	L	H	L	Low-Z	active	flash clear
L	H	H	L	Hi-Z	active	flash clear

4874 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $	t_{aa} ns	t_{ref} ms	Output
MK 48H74 N-35	Sgs	28-DIP	CMOS	0...+70	<687,5	<35		TTL-TS
MK 48H74 N-45	Sgs	28-DIP	CMOS	0...+70	<687,5	<45		TTL-TS
MK 48H74 N-55	Sgs	28-DIP	CMOS	0...+70	<687,5	<55		TTL-TS
MK 48H74 P-35	Sgs	28-DIC	CMOS	0...+70	<687,5	<35		TTL-TS
MK 48H74 P-45	Sgs	28-DIC	CMOS	0...+70	<687,5	<45		TTL-TS
MK 48H74 P-55	Sgs	28-DIC	CMOS	0...+70	<687,5	<55		TTL-TS
MK 48S74 N-20	Sgs	28-TDIP	CMOS	0...+70	<825	<20		TTL-TS
MK 48S74 N-22	Sgs	28-TDIP	CMOS	0...+70	<825	<22		TTL-TS
MK 48S74 N-25	Sgs	28-TDIP	CMOS	0...+70	<825	<25		TTL-TS
MK 48S74 X-20	Sgs	28-FLAT	CMOS	0...+70	<825	<20		TTL-TS
MK 48S74 X-22	Sgs	28-FLAT	CMOS	0...+70	<825	<22		TTL-TS
MK 48S74 X-25	Sgs	28-FLAT	CMOS	0...+70	<825	<25		TTL-TS
MK 48S75 N-20	Sgs	28-DIP	CMOS	0...+70	<825	<20		TTL-TS
MK 48S75 N-22	Sgs	28-DIP	CMOS	0...+70	<825	<22		TTL-TS
MK 48S75 N-25	Sgs	28-DIP	CMOS	0...+70	<825	<25		TTL-TS

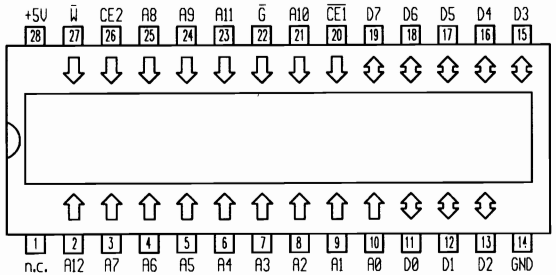
4880 — 8192x8-Bit Stat. Cache RAM w. Comparator



$\overline{CE}$	$\overline{G}$	$\overline{W}$	$\overline{CLR}$	D_{out}	Power	Mode
H	X	X	X	Hi-Z	standby	deselect
L	X	L	H	data in	active	write
L	L	H	H	data out	active	read
L	H	H	H	Hi-Z	active	read
L	X	L	L	Hi-Z	active	flash clear
L	L	H	L	Low-Z	active	flash clear
L	H	H	L	Hi-Z	active	flash clear

4880 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48S80 N-15	Sgs	28-TDIP	CMOS	0...+70			<15		TTL-TS
MK 48S80 N-17	Sgs	28-TDIP	CMOS	0...+70			<17		TTL-TS
MK 48S80 N-20	Sgs	28-TDIP	CMOS	0...+70			<20		TTL-TS
MK 48S80 X-15	Sgs	28-FLAT	CMOS	0...+70			<15		TTL-TS
MK 48S80 X-17	Sgs	28-FLAT	CMOS	0...+70			<17		TTL-TS
MK 48S80 X-20	Sgs	28-FLAT	CMOS	0...+70			<20		TTL-TS

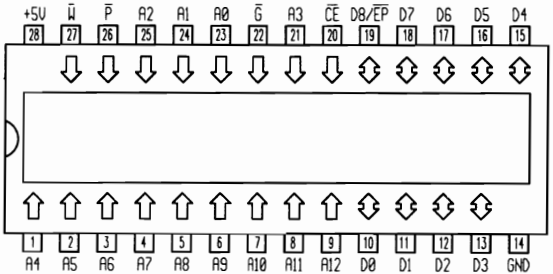
4889 — 8192x9-Bit static RAM



$\overline{W}$	$\overline{CE1}$	CE2	$\overline{G}$	D_n	Power	Mode
X	H	X	X	Hi-Z	standby	deselect
X	X	L	X	Hi-Z	standby	deselect
H	L	H	H	Hi-Z	active	read
H	L	H	L	data out	active	read
L	L	H	X	data in	active	write

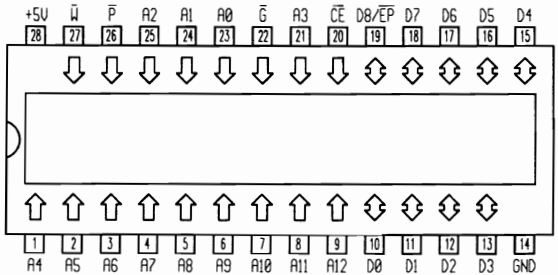
4889 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48H89 N-20	Sgs	28-TDIP	CMOS	0...+70			<20		TTL-TS
MK 48H89 N-25	Sgs	28-TDIP	CMOS	0...+70			<25		TTL-TS
MK 48H89 N-35	Sgs	28-TDIP	CMOS	0...+70			<35		TTL-TS

4898 — 8192x8-Bit static Parity RAM



* Funktioniert als 8 K × 9 Bit statisches RAM wenn (P = H).
* Operation as an 8 K × 9 Bit static RAM (P = H).
* Fonctionne en tant que RAM statique 8 K × 9 bits lorsque (P = H).
* Funziona come RAM statico da 8 K × 9 bit se (P = H).
* Funciona como RAM estática de 8 K × 9 bits cuando (P = H).

4899 — 8192x9-Bit static Parity RAM

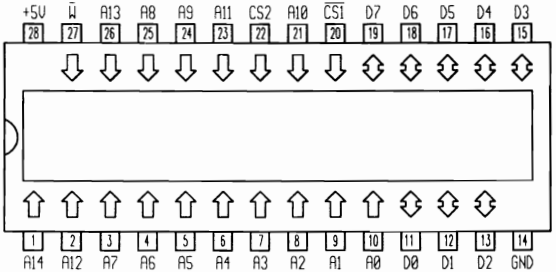


* Funktioniert als 8 K × 9 Bit statisches RAM wenn (P = H).
* Operation as an 8 K × 9 Bit static RAM (P = H).
* Fonctionne en tant que RAM statique 8 K × 9 bits lorsque (P = H).
* Funziona come RAM statico da 8 K × 9 bit se (P = H).
* Funciona como RAM estática de 8 K × 9 bits cuando (P = H).

4898 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48H98 N-20	Sgs	28-TDIP	CMOS	0...+70			<20		TTL-TS
MK 48H98 N-30	Sgs	28-TDIP	CMOS	0...+70			<30		TTL-TS
MK 48H98 N-40	Sgs	28-TDIP	CMOS	0...+70			<40		TTL-TS

4899 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48H99 N-20	Sgs	28-TDIP	CMOS	0...+70			<20		TTL-TS
MK 48H99 N-30	Sgs	28-TDIP	CMOS	0...+70			<30		TTL-TS
MK 48H99 N-40	Sgs	28-TDIP	CMOS	0...+70			<40		TTL-TS

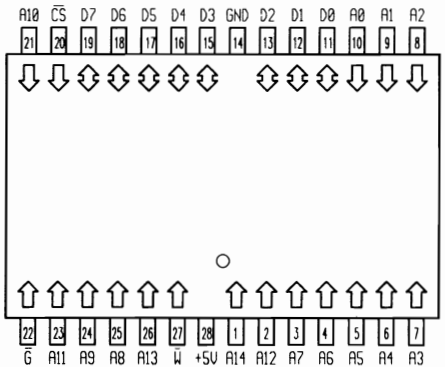
5255 — 32768x8-Bit static RAM



$\overline{CS1}$	CS2	$\overline{W}$	D_{out}	Power	Mode
H	X	X	Hi-Z	standby	not selected
X	L	X	Hi-Z	standby	not selected
L	H	L	data in	active	write
L	H	H	data out	active	read

5255 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 5255 BFP-10	Mit	28-FLAT	CMOS	0...+70	<385	<11	<100		TTL-TS
M5M 5255 BFP-10L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5255 BFP-10LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5255 BFP-12	Mit	28-FLAT	CMOS	0...+70	<385	<11	<120		TTL-TS
M5M 5255 BFP-12L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5255 BFP-12LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5255 BFP-70	Mit	28-FLAT	CMOS	0...+70	<385	<11	<70		TTL-TS
M5M 5255 BFP-70L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<70		TTL-TS
M5M 5255 BFP-70LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<70		TTL-TS
M5M 5255 BFP-85	Mit	28-FLAT	CMOS	0...+70	<385	<11	<85		TTL-TS
M5M 5255 BFP-85L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<85		TTL-TS
M5M 5255 BFP-85LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<85		TTL-TS
M5M 5255 BKP-10	Mit	28-TDIP	CMOS	0...+70	<385	<11	<100		TTL-TS
M5M 5255 BKP-10L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5255 BKP-10LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5255 BKP-12	Mit	28-TDIP	CMOS	0...+70	<385	<11	<120		TTL-TS
M5M 5255 BKP-12L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5255 BKP-12LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5255 BKP-70	Mit	28-TDIP	CMOS	0...+70	<385	<11	<70		TTL-TS
M5M 5255 BKP-70L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<70		TTL-TS
M5M 5255 BKP-70LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<70		TTL-TS
M5M 5255 BKP-85	Mit	28-TDIP	CMOS	0...+70	<385	<11	<85		TTL-TS
M5M 5255 BKP-85L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<85		TTL-TS
M5M 5255 BKP-85LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<85		TTL-TS
M5M 5255 BP-10	Mit	28-DIP	CMOS	0...+70	<385	<11	<100		TTL-TS
M5M 5255 BP-10L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5255 BP-10LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5255 BP-12	Mit	28-DIP	CMOS	0...+70	<385	<11	<120		TTL-TS
M5M 5255 BP-12L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5255 BP-12LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5255 BP-70	Mit	28-DIP	CMOS	0...+70	<385	<11	<70		TTL-TS
M5M 5255 BP-70L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<70		TTL-TS
M5M 5255 BP-70LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<70		TTL-TS
M5M 5255 BP-85	Mit	28-DIP	CMOS	0...+70	<385	<11	<85		TTL-TS
M5M 5255 BP-85L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<85		TTL-TS
M5M 5255 BP-85LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<85		TTL-TS

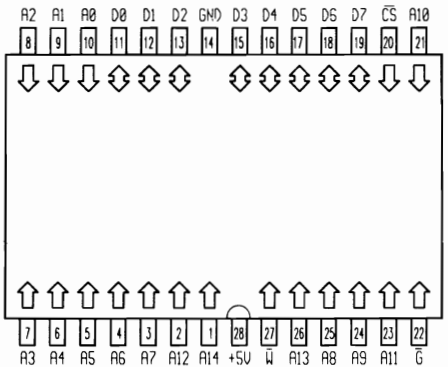
5256 — 32768x8-Bit static RAM



$\overline{CS}$	$\overline{G}$	$\overline{W}$	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	H	data out	read
L	H	L	data in	write (cycle 1)
L	L	L	data in	write (cycle 2)

5256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 5256 BVP-10L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5256 BVP-10LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5256 BVP-12L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5256 BVP-12LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5256 BVP-15L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<150		TTL-TS
M5M 5256 BVP-15LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<150		TTL-TS

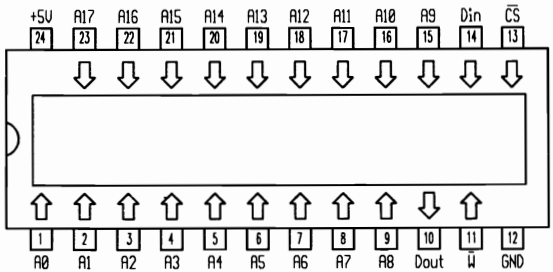
5256 — 32768x8-Bit static RAM



$\overline{CS}$	$\overline{G}$	$\overline{W}$	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	H	data out	read
L	H	L	data in	write (cycle 1)
L	L	L	data in	write (cycle 2)

5256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 5256 BRV-10L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5256 BRV-10LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5256 BRV-12L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5256 BRV-12LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5256 BRV-15L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<150		TTL-TS
M5M 5256 BRV-15LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<150		TTL-TS

5257 — 262144x1-Bit static RAM

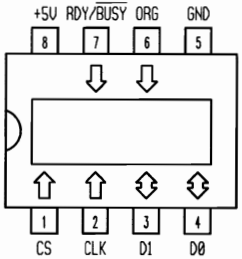


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

5257 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 5257 AJ-25	Mit	24-FLAT	CMOS	0...+70	<420	<55	<25		TTL-TS
M5M 5257 AJ-30	Mit	24-FLAT	CMOS	0...+70	<420	<55	<30		TTL-TS
M5M 5257 AP-25	Mit	24-DIP	CMOS	0...+70	<420	<55	<25		TTL-TS
M5M 5257 AP-30	Mit	24-DIP	CMOS	0...+70	<420	<55	<30		TTL-TS
M5M 5257 BJ-15	Mit	24-FLAT	CMOS	0...+70	<420	<16,5	<15		TTL-TS
M5M 5257 BJ-20	Mit	24-FLAT	CMOS	0...+70	<420	<16,5	<20		TTL-TS
M5M 5257 BP-15	Mit	24-DIP	CMOS	0...+70	<420	<16,5	<15		TTL-TS
M5M 5257 BP-20	Mit	24-DIP	CMOS	0...+70	<420	<16,5	<20		TTL-TS

5257 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 5257 J-35	Mit	24-FLAT	CMOS	0...+70	<420	<16,5	<35		TTL-TS
M5M 5257 J-45	Mit	24-FLAT	CMOS	0...+70	<420	<16,5	<45		TTL-TS
M5M 5257 J-45L	Mit	24-FLAT	CMOS	0...+70	<420	<1,65	<45		TTL-TS
M5M 5257 P-35	Mit	24-DIP	CMOS	0...+70	<420	<16,5	<35		TTL-TS
M5M 5257 P-45	Mit	24-DIP	CMOS	0...+70	<420	<16,5	<45		TTL-TS
M5M 5257 P-45L	Mit	24-DIP	CMOS	0...+70	<420	<1,65	<45		TTL-TS

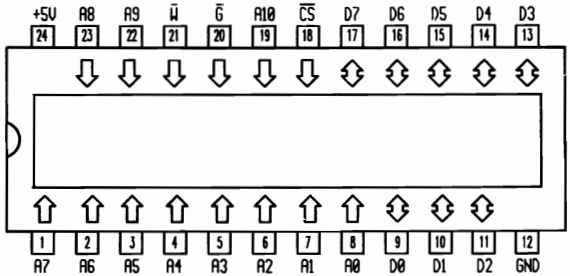
5911 — 128x8-Bit serial EEPROM



Start-Bit	Operation-Code	Address 128x8	Address 64x16	Data 128x8	Data 64x16	Mode
1	1000	A6...A0	A5...A0			read address
1	X100	A6...A0	A5...A0	$D_7...D_0$	$D_{15}...D_0$	program
1	0011	0000000	000000			program enable (PEN)
1	0000	0000000	000000			program disable (PDS)
1	0010	0000000	000000			erase all addresses (ERAL)
1	0001	0000000	000000	$D_7...D_0$	$D_{15}...D_0$	program all addresses (WRAL)

5911 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TS 59C11 CP	Sgs	8-DIP	CMOS	0...+70	<22	<0,55			
TS 59C11 VP	Sgs	8-DIP	CMOS	-40...+85	<22	<0,55			

6116 — 2048x8-Bit static RAM



$\overline{CS}$	$\overline{G}$	$\overline{W}$	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	H	data out	read
L	H	L	data in	write (cycle 1)
L	L	L	data in	write (cycle 2)

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6116-2	Hit	24-DIC	CMOS	0...+70	180	0,1	<120		TTL
HM 6116-3	Hit	24-DIC	CMOS	0...+70	180	0,1	<150		TTL
HM 6116-4	Hit	24-DIC	CMOS	0...+70	180	0,1	<200		TTL
HM 6116 ALP-12	Hit	24-DIP	CMOS	0...+70	<275	<16,5	<120		TTL-TS
HM 6116 ALP-15	Hit	24-DIP	CMOS	0...+70	<220	<16,5	<150		TTL-TS
HM 6116 ALP-20	Hit	24-DIP	CMOS	0...+70	<165	<16,5	<200		TTL-TS
HM 6116 ALSP-12	Hit	24-TDIP	CMOS	0...+70	<275	<16,5	<120		TTL-TS
HM 6116 ALSP-15	Hit	24-TDIP	CMOS	0...+70	<220	<16,5	<150		TTL-TS

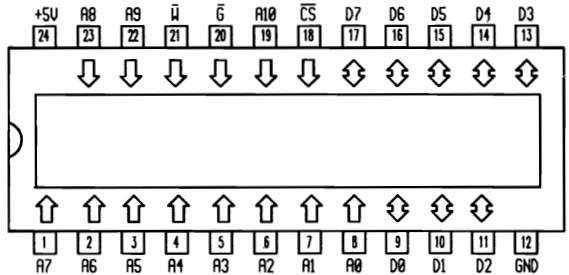
6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6116 ALSP-20	Hit	24-TDIP	CMOS	0...+70	<165	<16,5	<200		TTL-TS
HM 6116 AP-12	Hit	24-DIP	CMOS	0...+70	<330	<22	<120		TTL-TS
HM 6116 AP-15	Hit	24-DIP	CMOS	0...+70	<247,5	<22	<150		TTL-TS
HM 6116 AP-20	Hit	24-DIP	CMOS	0...+70	<192,5	<22	<200		TTL-TS
HM 6116 ASP-12	Hit	24-TDIP	CMOS	0...+70	<330	<22	<120		TTL-TS
HM 6116 ASP-15	Hit	24-TDIP	CMOS	0...+70	<247,5	<22	<150		TTL-TS
HM 6116 ASP-20	Hit	24-TDIP	CMOS	0...+70	<192,5	<22	<200		TTL-TS
HM 6116 FP-2	Hit	24-Flat	CMOS	0...+70	180	0,1	<120		TTL
HM 6116 FP-3	Hit	24-Flat	CMOS	0...+70	180	0,1	<150		TTL
HM 6116 FP-4	Hit	24-Flat	CMOS	0...+70	180	0,1	<200		TTL
HM 6116 L-2	Hit	24-Dic	CMOS	0...+70	160	20µ	<120		TTL
HM 6116 L-3	Hit	24-Dic	CMOS	0...+70	160	20µ	<150		TTL
HM 6116 L-4	Hit	24-Dic	CMOS	0...+70	160	20µ	<200		TTL
HM 6116 LFP-2	Hit	24-Flat	CMOS	0...+70	160	10µ	<120		TTL
HM 6116 LFP-3	Hit	24-Flat	CMOS	0...+70	160	10µ	<150		TTL
HM 6116 LFP-4	Hit	24-Flat	CMOS	0...+70	160	10µ	<200		TTL
HM 6116 LP-2	Hit	24-Dip	CMOS	0...+70	160	10µ	<120		TTL
HM 6116 LP-3	Hit	24-Dip	CMOS	0...+70	160	10µ	<150		TTL
HM 6116 LP-4	Hit	24-Dip	CMOS	0...+70	160	10µ	<200		TTL
HM 6116 P-2	Hit	24-DIP	CMOS	0...+70	180	0,1	<120		TTL
HM 6116 P-3	Hit	24-DIP	CMOS	0...+70	180	0,1	<150		TTL
HM 6116 P-4	Hit	24-DIP	CMOS	0...+70	180	0,1	<200		TTL
HM1 6116 -2	Mhs	24-DIC	CMOS	-55...+125	<467,5	<27,5	<120		TTL-TS
HM1 6116 -5	Mhs	24-DIC	CMOS	0...+70	<385	<16,5	<120		TTL-TS
HM1 6116 -9	Mhs	24-DIC	CMOS	-40...+85	<440	<24,75	<120		TTL-TS
HM1 6116 L-2	Mhs	24-DIC	CMOS	-55...+125	<467,5	<24,75	<120		TTL-TS
HM1 6116 L-5	Mhs	24-DIC	CMOS	0...+70	<385	<11	<120		TTL-TS
HM1 6116 L-9	Mhs	24-DIC	CMOS	-40...+85	<440	<22	<120		TTL-TS
HM1 65161 -2	Mhs	24-DIC	CMOS	-55...+125	<467,5	<22	<90		TTL-TS
HM1 65161 -5	Mhs	24-DIC	CMOS	0...+70	<385	<11	<70		TTL-TS
HM1 65161 -9	Mhs	24-DIC	CMOS	-40...+85	<440	<16,5	<80		TTL-TS
HM1 65162 -2	Mhs	24-DIC	CMOS	-55...+125	<385	<27,5	<85		TTL-TS
HM1 65162 -5	Mhs	24-DIC	CMOS	0...+70	<385	<11	<70		TTL-TS
HM1 65162 -9	Mhs	24-DIC	CMOS	-40...+85	<385	<16,5	<85		TTL-TS
HM1 65162 B-2	Mhs	24-DIC	CMOS	-55...+125	<385	<27,5	<70		TTL-TS
HM1 65162 B-5	Mhs	24-DIC	CMOS	0...+70	<385	<11	<55		TTL-TS
HM1 65162 B-9	Mhs	24-DIC	CMOS	-40...+85	<385	<16,5	<70		TTL-TS

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65162 C-2	Mhs	24-DIC	CMOS	-55...+125	<385	<27,5	<85		TTL-TS
HM1 65162 C-5	Mhs	24-DIC	CMOS	0...+70	<385	<11	<70		TTL-TS
HM1 65162 C-9	Mhs	24-DIC	CMOS	-40...+85	<385	<16,5	<85		TTL-TS
HM1 65728 F-5	Mhs	24-DIC	CMOS	0...+70	<550	<55	<20		TTL-TS
HM1 65728 H-2	Mhs	24-DIC	CMOS	-55...+125	<660	<110	<25		TTL-TS
HM1 65728 H-5	Mhs	24-DIC	CMOS	0...+70	<550	<55	<25		TTL-TS
HM1 65728 K-2	Mhs	24-DIC	CMOS	-55...+125	<660	<165	<35		TTL-TS
HM1 65728 K-5	Mhs	24-DIC	CMOS	0...+70	<550	<55	<35		TTL-TS
HM1 65728 M-2	Mhs	24-DIC	CMOS	-55...+125	<715	<165	<45		TTL-TS
HM1 65728 M-5	Mhs	24-DIC	CMOS	0...+70	<550	<55	<45		TTL-TS
HM1 65728 N-2	Mhs	24-DIC	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM1 65728 N-5	Mhs	24-DIC	CMOS	0...+70	<550	<55	<55		TTL-TS
HM3 6116 -2	Mhs	24-DIP	CMOS	-55...+125	<467,5	<27,5	<120		TTL-TS
HM3 6116 -5	Mhs	24-DIP	CMOS	0...+70	<385	<16,5	<120		TTL-TS
HM3 6116 -9	Mhs	24-DIP	CMOS	-40...+85	<440	<24,75	<120		TTL-TS
HM3 6116 L-2	Mhs	24-DIP	CMOS	-55...+125	<467,5	<24,75	<120		TTL-TS
HM3 6116 L-5	Mhs	24-DIP	CMOS	0...+70	<385	<11	<120		TTL-TS
HM3 6116 L-9	Mhs	24-DIP	CMOS	-40...+85	<440	<22	<120		TTL-TS
HM3 65161 -2	Mhs	24-DIP	CMOS	-55...+125	<467,5	<22	<90		TTL-TS
HM3 65161 -5	Mhs	24-DIP	CMOS	0...+70	<385	<11	<70		TTL-TS
HM3 65161 -9	Mhs	24-DIP	CMOS	-40...+85	<440	<16,5	<80		TTL-TS
HM3 65162 -2	Mhs	24-DIP	CMOS	-55...+125	<385	<27,5	<85		TTL-TS
HM3 65162 -5	Mhs	24-DIP	CMOS	0...+70	<385	<11	<70		TTL-TS
HM3 65162 -9	Mhs	24-DIP	CMOS	-40...+85	<385	<16,5	<85		TTL-TS
HM3 65162 B-2	Mhs	24-DIP	CMOS	-55...+125	<385	<27,5	<70		TTL-TS
HM3 65162 B-5	Mhs	24-DIP	CMOS	0...+70	<385	<11	<55		TTL-TS
HM3 65162 B-9	Mhs	24-DIP	CMOS	-40...+85	<385	<16,5	<70		TTL-TS
HM3 65162 C-2	Mhs	24-DIP	CMOS	-55...+125	<385	<27,5	<85		TTL-TS
HM3 65162 C-5	Mhs	24-DIP	CMOS	0...+70	<385	<11	<70		TTL-TS
HM3 65162 C-9	Mhs	24-DIP	CMOS	-40...+85	<385	<16,5	<85		TTL-TS
HM3 65728 F-5	Mhs	24-TDIP	CMOS	0...+70	<550	<55	<20		TTL-TS
HM3 65728 H-2	Mhs	24-TDIP	CMOS	-55...+125	<660	<110	<25		TTL-TS
HM3 65728 H-5	Mhs	24-TDIP	CMOS	0...+70	<550	<55	<25		TTL-TS
HM3 65728 K-2	Mhs	24-TDIP	CMOS	-55...+125	<660	<165	<35		TTL-TS
HM3 65728 K-5	Mhs	24-TDIP	CMOS	0...+70	<550	<55	<35		TTL-TS
HM3 65728 M-2	Mhs	24-TDIP	CMOS	-55...+125	<715	<165	<45		TTL-TS
HM3 65728 M-5	Mhs	24-TDIP	CMOS	0...+70	<550	<55	<45		TTL-TS

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM3 65728 N-2	Mhs	24-TDIP	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM3 65728 N-5	Mhs	24-TDIP	CMOS	0...+70	<550	<55	<55		TTL-TS
HM3E 65728 F-5	Mhs	24-DIP	CMOS	0...+70	<550	<55	<20		TTL-TS
HM3E 65728 H-2	Mhs	24-DIP	CMOS	-55...+125	<660	<110	<25		TTL-TS
HM3E 65728 H-5	Mhs	24-DIP	CMOS	0...+70	<550	<55	<25		TTL-TS
HM3E 65728 K-2	Mhs	24-DIP	CMOS	-55...+125	<660	<165	<35		TTL-TS
HM3E 65728 K-5	Mhs	24-DIP	CMOS	0...+70	<550	<55	<35		TTL-TS
HM3E 65728 M-2	Mhs	24-DIP	CMOS	-55...+125	<715	<165	<45		TTL-TS
HM3E 65728 M-5	Mhs	24-DIP	CMOS	0...+70	<550	<55	<45		TTL-TS
HM3E 65728 N-2	Mhs	24-DIP	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM3E 65728 N-5	Mhs	24-DIP	CMOS	0...+70	<550	<55	<55		TTL-TS
HMT 65728 F-5	Mhs	24-FLAT	CMOS	0...+70	<550	<55	<20		TTL-TS
HMT 65728 H-2	Mhs	24-FLAT	CMOS	-55...+125	<660	<110	<25		TTL-TS
HMT 65728 H-5	Mhs	24-FLAT	CMOS	0...+70	<550	<55	<25		TTL-TS
HMT 65728 K-2	Mhs	24-FLAT	CMOS	-55...+125	<660	<165	<35		TTL-TS
HMT 65728 K-5	Mhs	24-FLAT	CMOS	0...+70	<550	<55	<35		TTL-TS
HMT 65728 M-2	Mhs	24-FLAT	CMOS	-55...+125	<715	<165	<45		TTL-TS
HMT 65728 M-5	Mhs	24-FLAT	CMOS	0...+70	<550	<55	<45		TTL-TS
HMT 65728 N-2	Mhs	24-FLAT	CMOS	-55...+125	<550	<165	<55		TTL-TS
HMT 65728 N-5	Mhs	24-FLAT	CMOS	0...+70	<550	<55	<55		TTL-TS
KM 6816 A-12	Sam	24-DIP	CMOS	0...+70	<165	<550µ	<120		TTL-TS
KM 6816 A-15	Sam	24-DIP	CMOS	0...+70	<165	<550µ	<150		TTL-TS
KM 6816 A-20	Sam	24-DIP	CMOS	0...+70	<165	<550µ	<200		TTL-TS
KM 6816 AL-12	Sam	24-DIP	CMOS	0...+70	<165	<55µ	<120		TTL-TS
KM 6816 AL-15	Sam	24-DIP	CMOS	0...+70	<165	<55µ	<150		TTL-TS
KM 6816 AL-20	Sam	24-DIP	CMOS	0...+70	<165	<55µ	<200		TTL-TS
M5M5116 P	Mit	24-DIP	CMOS		<250	<75µ	<200		TTL-TS
M5M5116 P-12	Mit	24-DIP	CMOS		<250	<75µ	<120		TTL-TS
M5M5116 P-15	Mit	24-DIP	CMOS		<250	<75µ	<150		TTL-TS
MCM 65116 C-12	Mot	24-DIC	CMOS	0...+70	<400	<75	<120		TTL-TS
MCM 65116 C-15	Mot	24-DIC	CMOS	0...+70	<400	<75	<150		TTL-TS
MCM 65116 C-20	Mot	24-DIC	CMOS	0...+70	<400	<75	<200		TTL-TS
MCM 65116 L-12	Mot	24-DIP	CMOS	0...+70	<400	<75	<120		TTL-TS
MCM 65116 L-15	Mot	24-DIC	CMOS	0...+70	<400	<75	<150		TTL-TS
MCM 65116 L-20	Mot	24-DIC	CMOS	0...+70	<400	<75	<200		TTL-TS
MK 48T12 B-25	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<250		TTL-TS
MK 6116L N-15	Sgs	24-DIP	CMOS	0...+70	<385	<16,5	<150		TTL-TS
MK 6116L N-20	Sgs	24-DIP	CMOS	0...+70	<385	<16,5	<200		TTL-TS
MK 6116L N-25	Sgs	24-DIP	CMOS	0...+70	<385	<16,5	<250		TTL-TS
MK 6116 N-15	Sgs	24-DIP	CMOS	0...+70	<385	<16,5	<150		TTL-TS
MK 6116 N-20	Sgs	24-DIP	CMOS	0...+70	<385	<16,5	<200		TTL-TS
MK 6116 N-25	Sgs	24-DIP	CMOS	0...+70	<385	<16,5	<250		TTL-TS
MKB 6116 J-82	Tho	24-DIC	NMOS	-55...+125	<440	<82,5	<150		TTL-TS
MKB 6116 J-83	Tho	24-DIC	NMOS	-55...+125	<440	<82,5	<200		TTL-TS
MKB 6116 J-84	Tho	24-DIC	NMOS	-55...+125	<440	<82,5	<250		TTL-TS
MKB 6116L J-82	Tho	24-DIC	NMOS	-55...+125	<440	<825µ	<150		TTL-TS
MKB 6116L J-83	Tho	24-DIC	NMOS	-55...+125	<440	<825µ	<200		TTL-TS
MKB 6116L J-84	Tho	24-DIC	NMOS	-55...+125	<440	<825µ	<250		TTL-TS
MKB 6116L P-82	Tho	24-DIP	NMOS	-55...+125	<440	<825µ	<150		TTL-TS
MKB 6116L P-83	Tho	24-DIP	NMOS	-55...+125	<440	<825µ	<200		TTL-TS
MKB 6116L P-84	Tho	24-DIP	NMOS	-55...+125	<440	<825µ	<250		TTL-TS
MKB 6116 P-82	Tho	24-DIP	NMOS	-55...+125	<440	<82,5	<150		TTL-TS
MKB 6116 P-83	Tho	24-DIP	NMOS	-55...+125	<440	<82,5	<200		TTL-TS
MKB 6116 P-84	Tho	24-DIP	NMOS	-55...+125	<440	<82,5	<250		TTL-TS
MKI 6116L N-15	Sgs	24-DIP	CMOS	-40...+85	<385	<16,5	<150		TTL-TS
MKI 6116L N-20	Sgs	24-DIP	CMOS	-40...+85	<385	<16,5	<200		TTL-TS
MKI 6116L N-25	Sgs	24-DIP	CMOS	-40...+85	<385	<16,5	<250		TTL-TS
MKI 6116 N-15	Sgs	24-DIP	CMOS	-40...+85	<385	<16,5	<150		TTL-TS
MKI 6116 N-20	Sgs	24-DIP	CMOS	-40...+85	<385	<16,5	<200		TTL-TS
MKI 6116 N-25	Sgs	24-DIP	CMOS	-40...+85	<385	<16,5	<250		TTL-TS
MN 4416-12	Mat	24-DIP	CMOS	0...+70	<165	<16,5	<120		TTL-TS
MN 4416-15	Mat	24-DIP	CMOS	0...+70	<165	<16,5	<150		TTL-TS
MN 4416 S-12	Mat	24-FLAT	CMOS	0...+70	<165	<16,5	<120		TTL-TS
MN 4416 S-15	Mat	24-FLAT	CMOS	0...+70	<165	<16,5	<150		TTL-TS
MSM 5128-12 RS	Oki	24-DIP	CMOS	0...+70	<330	<0,275	<120		TTL-TS
MSM 5128-15 RS	Oki	24-DIP	CMOS	0...+70	<275	<0,275	<150		TTL-TS
MSM 5128-20 RS	Oki	24-DIP	CMOS	0...+70	<275	<0,275	<200		TTL-TS
MSM 5128-25 RS	Oki	24-DIP	CMOS	0...+70	<330	<0,275	<250		TTL-TS
SBB 6116-12	Val	24-DIP	CMOS	0...+70	<275	<11	<120		TTL-TS
TC 5517 AD	Tos	24-DIC	CMOS	-30...+85	<165	<165µ	<250		TTL-TS
TC 5517 AD-2	Tos	24-DIC	CMOS	-30...+85	<165	<165µ	<200		TTL-TS
TC 5517 AP	Tos	24-DIP	CMOS	-30...+85	<165	<165µ	<250		TTL-TS
TC 5517 AP-2	Tos	24-DIP	CMOS	-30...+85	<165	<165µ	<200		TTL-TS
TC 5517 BD	Tos	24-DIC	CMOS	-30...+85	<165	<165µ	<200		TTL-TS

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 5517 BDL	Tos	24-DIC	CMOS	-30...+85	<165	<5,5µ	<200		TTL-TS
TC 5517 BP	Tos	24-DIP	CMOS	-30...+85	<165	<165µ	<200		TTL-TS
TC 5517 BPL	Tos	24-DIP	CMOS	-30...+85	<165	<5,5µ	<200		TTL-TS
TC 5517 CF-15	Tos	24-FLAT	CMOS	0...+70	<247,5	<27,5µ	<150		TTL-TS
TC 5517 CF-20	Tos	24-FLAT	CMOS	0...+70	<165	<27,5µ	<200		TTL-TS
TC 5517 CFL-15	Tos	24-FLAT	CMOS	0...+70	<247,5	<5,5µ	<150		TTL-TS
TC 5517 CFL-20	Tos	24-FLAT	CMOS	0...+70	<165	<5,5µ	<200		TTL-TS
TC 5517 CP-15	Tos	24-DIP	CMOS	0...+70	<247,5	<27,5µ	<150		TTL-TS
TC 5517 CP-20	Tos	24-DIP	CMOS	0...+70	<165	<27,5µ	<200		TTL-TS
TC 5517 CPL-15	Tos	24-DIP	CMOS	0...+70	<247,5	<5,5µ	<150		TTL-TS
TC 5517 CPL-20	Tos	24-DIP	CMOS	0...+70	<165	<5,5µ	<200		TTL-TS
TMM 2015 BP-10	Tos	24-TDIP	NMOS	0...+70	<50	<5	<100		TTL-TS
TMM 2015 BP-12	Tos	24-TDIP	NMOS	0...+70	<50	<5	<120		TTL-TS
TMM 2015 BP-15	Tos	24-TDIP	NMOS	0...+70	<50	<5	<150		TTL-TS
TMM 2015 BP-90	Tos	24-TDIP	NMOS	0...+70	<50	<5	<90		TTL-TS
µPD 446 C	Nip	24-DIP	CMOS	-40...+85	<99	<0,055	<450		TTL-TS
µPD 446 C-1	Nip	24-DIP	CMOS	-40...+85	<143	<0,055	<250		TTL-TS
µPD 446 C-2	Nip	24-DIP	CMOS	-40...+85	<165	<0,055	<200		TTL-TS
µPD 446 C-3	Nip	24-DIP	CMOS	-40...+85	<209	<0,055	<150		TTL-TS
µPD 446 D	Nip	24-DIC	CMOS	-40...+85	<99	<0,055	<450		TTL-TS
µPD 446 D-1	Nip	24-DIC	CMOS	-40...+85	<143	<0,055	<250		TTL-TS
µPD 446 D-2	Nip	24-DIC	CMOS	-40...+85	<165	<0,055	<200		TTL-TS
µPD 446 D-3	Nip	24-DIC	CMOS	-40...+85	<209	<0,055	<150		TTL-TS
µPD 446 G-15	Nip	24-FLAT	CMOS	-40...+85	<209	<0,055	<150		TTL-TS
µPD 446 G-20	Nip	24-FLAT	CMOS	-40...+85	<165	<0,055	<200		TTL-TS
µPD 446 G-25	Nip	24-FLAT	CMOS	-40...+85	<143	<0,055	<250		TTL-TS
µPD 446 G-45	Nip	24-FLAT	CMOS	-40...+85	<99	<0,055	<450		TTL-TS

6116 — 2048x8-Bit static RAM Zeropower



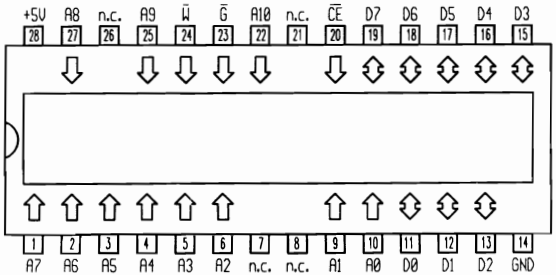
$\overline{CE}$	$\overline{G}$	$\overline{W}$	V_{CC}	D_n	Mode
H	X	X	≧4,75V ≦5,5V*	Hi-Z	deselect
L	X	L	≧4,75V ≦5,5V*	data in	write
L	L	H	≧4,75V ≦5,5V*	data out	read
L	H	H	≧4,75V ≦5,5V*	Hi-Z	read
X	X	X	≦4,5V >3V**	Hi-Z	power fail deselect
X	X	X	≦3V	Hi-Z	Battery backup

* MK 4812 ≧4,5V ≦5,5V ** MK 4812 ≦4,2V >3V

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48T02 B-12	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<120		TTL-TS
MK 48T02 B-15	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<150		TTL-TS
MK 48T02 B-20	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<200		TTL-TS
MK 48T02 B-25	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<250		TTL-TS
MK 48Z02 B-12	Sgs	24-DIP	CMOS	0...+70	<440	<5,5	<120		TTL-TS
MK 48Z02 B-15	Sgs	24-DIP	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48Z02 B-20	Sgs	24-DIP	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48Z02 B-25	Sgs	24-DIP	CMOS	0...+70	<440	<16,5	<250		TTL-TS

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standb mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48T12 B-12	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<120		TTL-TS
MK 48T12 B-15	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<150		TTL-TS
MK 48T12 B-20	Tho	24-DIP	CMOS	0...+70	<440	<27,5	<200		TTL-TS
MK 48Z12 B-12	Sgs	24-DIP	CMOS	0...+70	<440	<16,5	<120		TTL-TS
MK 48Z12 B-15	Sgs	24-DIP	CMOS	0...+70	<440	<16,5	<150		TTL-TS
MK 48Z12 B-20	Sgs	24-DIP	CMOS	0...+70	<440	<16,5	<200		TTL-TS
MK 48Z12 B-25	Sgs	24-DIP	CMOS	0...+70	<440	<16,5	<250		TTL-TS
MKI 48Z02 B-15	Sgs	24-DIP	CMOS	-40...+85	<440	<16,5	<150		TTL-TS
MKI 48Z02 B-20	Sgs	24-DIP	CMOS	-40...+85	<440	<16,5	<200		TTL-TS
MKI 48Z02 B-25	Sgs	24-DIP	CMOS	-40...+85	<440	<16,5	<250		TTL-TS
MKI 48Z12 B-15	Sgs	24-DIP	CMOS	-40...+85	<440	<16,5	<150		TTL-TS
MKI 48Z12 B-20	Sgs	24-DIP	CMOS	-40...+85	<440	<16,5	<200		TTL-TS
MKI 48Z12 B-25	Sgs	24-DIP	CMOS	-40...+85	<440	<16,5	<250		TTL-TS

6116 — 2048x8-Bit static RAM

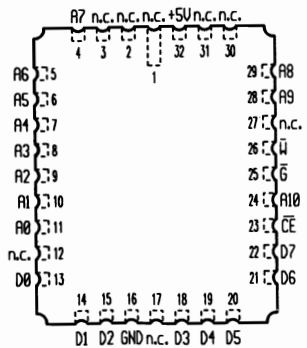


$\overline{CS}$	$\overline{G}$	$\overline{W}$	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	H	data out	read
L	H	L	data in	write (cycle 1)
L	L	L	data in	write (cycle 2)

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 6116L S-15	Sgs	28-FLAT	CMOS	0...+70	<385	<16.5	<150		TTL-TS
MK 6116L S-20	Sgs	28-FLAT	CMOS	0...+70	<385	<16.5	<200		TTL-TS
MK 6116L S-25	Sgs	28-FLAT	CMOS	0...+70	<385	<16,5	<250		TTL-TS
MK 6116 S-15	Sgs	28-FLAT	CMOS	0...+70	<385	<16,5	<150		TTL-TS
MK 6116 S-20	Sgs	28-FLAT	CMOS	0...+70	<385	<16,5	<200		TTL-TS
MK 6116 S-25	Sgs	28-FLAT	CMOS	0...+70	<385	<16,5	<250		TTL-TS
MKI 6116L S-15	Sgs	28-FLAT	CMOS	-40...+85	<385	<16,5	<150		TTL-TS
MKI 6116L S-20	Sgs	28-FLAT	CMOS	-40...+85	<385	<16,5	<200		TTL-TS

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MKI 6116L S-25	Sgs	28-FLAT	CMOS	-40...+85	<385	<16,5	<250		TTL-TS
MKI 6116 S-15	Sgs	28-FLAT	CMOS	-40...+85	<385	<16,5	<150		TTL-TS
MKI 6116 S-20	Sgs	28-FLAT	CMOS	-40...+85	<385	<16,5	<200		TTL-TS
MKI 6116 S-25	Sgs	28-FLAT	CMOS	-40...+85	<385	<16,5	<250		TTL-TS

6116 — 2048x8-Bit static RAM

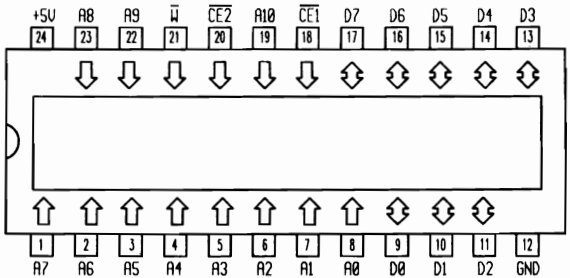


CS	G	W	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	H	data out	read
L	H	L	data in	write (cycle 1)
L	L	L	data in	write (cycle 2)

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 6116 -2	Mhs	32-LCC	CMOS	-55...+125	<467,5	<27,5	<120		TTL-TS
HM4 6116 -5	Mhs	32-LCC	CMOS	0...+70	<385	<16,5	<120		TTL-TS
HM4 6116 -9	Mhs	32-LCC	CMOS	-40...+85	<440	<22	<120		TTL-TS
HM4 6116 L-2	Mhs	32-LCC	CMOS	-55...+125	<467,5	<24,75	<120		TTL-TS
HM4 6116 L-5	Mhs	32-LCC	CMOS	0...+70	<385	<11	<120		TTL-TS
HM4 6116 L-9	Mhs	32-LCC	CMOS	-40...+85	<440	<24,75	<120		TTL-TS
HM4 65161 -2	Mhs	32-LCC	CMOS	-55...+125	<467,5	<22	<90		TTL-TS
HM4 65161 -5	Mhs	32-LCC	CMOS	0...+70	<385	<11	<70		TTL-TS

6116 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65161 -9	Mhs	32-LCC	CMOS	-40...+85	<440	<16,5	<80		TTL-TS
HM4 65162 -2	Mhs	32-LCC	CMOS	-55...+125	<385	<27,5	<85		TTL-TS
HM4 65162 -5	Mhs	32-LCC	CMOS	0...+70	<385	<11	<70		TTL-TS
HM4 65162 -9	Mhs	32-LCC	CMOS	-40...+85	<385	<16,5	<85		TTL-TS
HM4 65162 B-2	Mhs	32-LCC	CMOS	-55...+125	<385	<27,5	<70		TTL-TS
HM4 65162 B-5	Mhs	32-LCC	CMOS	0...+70	<385	<11	<55		TTL-TS
HM4 65162 B-9	Mhs	32-LCC	CMOS	-40...+85	<385	<16,5	<70		TTL-TS
HM4 65162 C-2	Mhs	32-LCC	CMOS	-55...+125	<385	<27,5	<85		TTL-TS
HM4 65162 C-5	Mhs	32-LCC	CMOS	0...+70	<385	<11	<70		TTL-TS
HM4 65162 C-9	Mhs	32-LCC	CMOS	-40...+85	<385	<16,5	<85		TTL-TS
HM4 65728 F-5	Mhs	32-LCC	CMOS	0...+70	<550	<55	<20		TTL-TS
HM4 65728 H-2	Mhs	32-LCC	CMOS	-55...+125	<660	<110	<25		TTL-TS
HM4 65728 H-5	Mhs	32-LCC	CMOS	0...+70	<550	<55	<25		TTL-TS
HM4 65728 K-2	Mhs	32-LCC	CMOS	-55...+125	<660	<165	<35		TTL-TS
HM4 65728 K-5	Mhs	32-LCC	CMOS	0...+70	<550	<55	<35		TTL-TS
HM4 65728 M-2	Mhs	32-LCC	CMOS	-55...+125	<715	<165	<45		TTL-TS
HM4 65728 M-5	Mhs	32-LCC	CMOS	0...+70	<550	<55	<45		TTL-TS
HM4 65728 N-2	Mhs	32-LCC	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM4 65728 N-5	Mhs	32-LCC	CMOS	0...+70	<550	<55	<55		TTL-TS
MKB 6116 E-82	Tho	32-LCC	NMOS	-55...+125	<440	<82,5	<150		TTL-TS
MKB 6116 E-83	Tho	32-LCC	NMOS	-55...+125	<440	<82,5	<200		TTL-TS
MKB 6116 E-84	Tho	32-LCC	NMOS	-55...+125	<440	<82,5	<250		TTL-TS
MKB 6116L E-82	Tho	32-LCC	NMOS	-55...+125	<440	<825µ	<150		TTL-TS
MKB 6116L E-83	Tho	32-LCC	NMOS	-55...+125	<440	<825µ	<200		TTL-TS
MKB 6116L E-84	Tho	32-LCC	NMOS	-55...+125	<440	<825µ	<250		TTL-TS

6117 — 2048x8-Bit static RAM

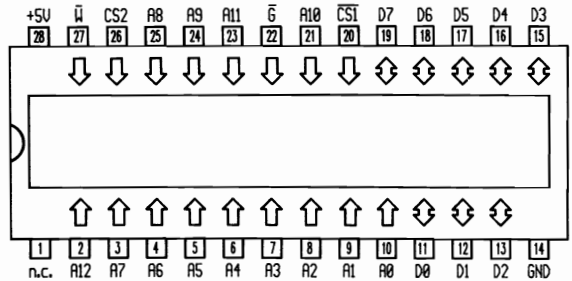


$\overline{CE1}$	$\overline{CE2}$	$\overline{W}$	D_{out}	Mode
H	X	X	Hi-Z	not selected
X	H	X	Hi-Z	not selected
L	L	H	data out	read
L	L	L	data in	write

6117 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6117 FP-3	Hit	24-Flat	CMOS	0...+70	200	0,1	<150		TTL
HM 6117 FP-4	Hit	24-Flat	CMOS	0...+70	200	0,1	<200		TTL
HM 6117 LFP-3	Hit	24-Flat	CMOS	0...+70	180	10µ	<150		TTL
HM 6117 LFP-4	Hit	24-Flat	CMOS	0...+70	180	10µ	<200		TTL
HM 6117 LP-3	Hit	24-Dip	CMOS	0...+70	180	10µ	<150		TTL
HM 6117 LP-4	Hit	24-Dip	CMOS	0...+70	180	10µ	<200		TTL
HM 6117 P-3	Hit	24-Dip	CMOS	0...+70	200	0,1	<150		TTL
HM 6117 P-4	Hit	24-Dip	CMOS	0...+70	200	0,1	<200		TTL

6117 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M5117 P	Mit	24-DIP	CMOS		<250	<75µ	<200		TTL-TS
M5M5117 P-12	Mit	24-DIP	CMOS		<250	<75µ	<120		TTL-TS
M5M5117 P-15	Mit	24-DIP	CMOS		<250	<75µ	<150		TTL-TS
TC 5516 AD-2	Tos	24-DIC	CMOS	-30…+85	<385	<5,5µ	<200		TTL-TS
TC 5516 ADL-2	Tos	24-DIC	CMOS	-30…+85	<165	<165µ	<200		TTL-TS
TC 5516 AP	Tos	24-DIP	CMOS	-30…+85	<385	<16,5	<250		TTL-TS
TC 5516 AP-2	Tos	24-DIP	CMOS	-30…+85	<385	<5,5µ	<200		TTL-TS
TC 5516 APL	Tos	24-DIP	CMOS	-30…+85	<385	<5,5µ	<250		TTL-TS
TC 5516 APL-2	Tos	24-DIP	CMOS	-30…+85	<165	<165µ	<200		TTL-TS
TC 5516 BP	Tos	24-DIP	CMOS	-30…+85	<165	<165µ	<200		TTL-TS
TC 5516 BPL	Tos	24-DIP	CMOS	-30…+85	<165	<5,5µ	<200		TTL-TS
TC 5518 CF-15	Tos	24-FLAT	CMOS	0…+70	<247,5	<27,5µ	<150		TTL-TS
TC 5518 CF-20	Tos	24-FLAT	CMOS	0…+70	<165	<27,5µ	<200		TTL-TS
TC 5518 CFL-15	Tos	24-FLAT	CMOS	0…+70	<247,5	<5,5µ	<150		TTL-TS
TC 5518 CFL-20	Tos	24-FLAT	CMOS	0…+70	<165	<5,5µ	<200		TTL-TS
TC 5518 CP-15	Tos	24-DIP	CMOS	0…+70	<247,5	<27,5µ	<150		TTL-TS
TC 5518 CP-20	Tos	24-DIP	CMOS	0…+70	<165	<27,5µ	<200		TTL-TS
TC 5518 CPL-15	Tos	24-DIP	CMOS	0…+70	<247,5	<5,5µ	<150		TTL-TS
TC 5518 CPL-20	Tos	24-DIP	CMOS	0…+70	<165	<5,5µ	<200		TTL-TS
µPD 449 C	Nip	24-DIP	CMOS	-40…+85	<99	<0,055	<450		TTL-TS
µPD 449 C-1	Nip	24-DIP	CMOS	-40…+85	<143	<0,055	<250		TTL-TS
µPD 449 C-2	Nip	24-DIP	CMOS	-40…+85	<165	<0,055	<200		TTL-TS
µPD 449 C-3	Nip	24-DIP	CMOS	-40…+85	<209	<0,055	<150		TTL-TS
µPD 449 D	Nip	24-DIC	CMOS	-40…+85	<99	<0,055	<450		TTL-TS
µPD 449 D-1	Nip	24-DIC	CMOS	-40…+85	<143	<0,055	<250		TTL-TS
µPD 449 D-2	Nip	24-DIC	CMOS	-40…+85	<165	<0,055	<200		TTL-TS
µPD 449 D-3	Nip	24-DIC	CMOS	-40…+85	<209	<0,055	<150		TTL-TS
µPD 449 G-15	Nip	24-FLAT	CMOS	-40…+85	<209	<0,055	<150		TTL-TS
µPD 449 G-20	Nip	24-FLAT	CMOS	-40…+85	<165	<0,055	<200		TTL-TS
µPD 449 G-25	Nip	24-FLAT	CMOS	-40…+85	<143	<0,055	<250		TTL-TS
µPD 449 G-45	Nip	24-FLAT	CMOS	-40…+85	<99	<0,055	<450		TTL-TS

6164 — 8192x8-Bit static RAM



$\overline{W}$	$\overline{CS1}$	CS2	$\overline{G}$	D_n	Mode
X	H	X	X	Hi-Z	not selected (power down)
X	X	L	X	Hi-Z	not selected (power down)
H	L	H	H	Hi-Z	output disabled
H	L	H	L	data out	read
L	L	H	X	data in	write

6164 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6264 AFP-12	Hit	28-FLAT	CMOS	0…+70	<247,5	<11	<120		TTL-TS
HM 6264 AFP-15	Hit	28-FLAT	CMOS	0…+70	<247,5	<11	<150		TTL-TS
HM 6264 ALFP-12	Hit	28-FLAT	CMOS	0…+70	<247,5	<5,5µ	<120		TTL-TS
HM 6264 ALFP-15	Hit	28-FLAT	CMOS	0…+70	<247,5	<5,5µ	<150		TTL-TS
HM 6264 ALSP-12	Hit	28-TDIP	CMOS	0…+70	<247,5	<5,5µ	<120		TTL-TS
HM 6264 ALSP-15	Hit	28-TDIP	CMOS	0…+70	<247,5	<5,5µ	<150		TTL-TS
HM 6264 ASP-12	Hit	28-TDIP	CMOS	0…+70	<247,5	<11	<120		TTL-TS
HM 6264 ASP-15	Hit	28-TDIP	CMOS	0…+70	<247,5	<11	<150		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 6264 FP-10	Hit	28-FLAT	CMOS	0...+70	<605	<11	<100		TTL-TS
HM 6264 FP-12	Hit	28-FLAT	CMOS	0...+70	<605	<11	<120		TTL-TS
HM 6264 FP-15	Hit	28-FLAT	CMOS	0...+70	<605	<11	<150		TTL-TS
HM 6264 LFP-10	Hit	28-FLAT	CMOS	0...+70	<605	<0,55	<100		TTL-TS
HM 6264 LFP-12	Hit	28-FLAT	CMOS	0...+70	<605	<0,55	<120		TTL-TS
HM 6264 LFP-12L	Hit	28-FLAT	CMOS	0...+70	<605	<0,275	<120		TTL-TS
HM 6264 LFP-15	Hit	28-FLAT	CMOS	0...+70	<605	<0,55	<150		TTL-TS
HM 6264 LFP-15L	Hit	28-FLAT	CMOS	0...+70	<605	<0,275	<150		TTL-TS
HM 6264 LP-10	Hit	28-DIP	CMOS	0...+70	<605	<0,55	<100		TTL-TS
HM 6264 LP-10L	Hit	28-DIP	CMOS	0...+70	<605	<0,275	<100		TTL-TS
HM 6264 LP-12	Hit	28-DIP	CMOS	0...+70	<605	<0,55	<120		TTL-TS
HM 6264 LP-12L	Hit	28-DIP	CMOS	0...+70	<605	<0,275	<120		TTL-TS
HM 6264 LP-15	Hit	28-DIP	CMOS	0...+70	<605	<0,55	<150		TTL-TS
HM 6264 LP-15L	Hit	28-DIP	CMOS	0...+70	<605	<0,275	<150		TTL-TS
HM 6264 P-10	Hit	28-DIP	CMOS	0...+70	<605	<11	<100		TTL-TS
HM 6264 P-12	Hit	28-DIP	CMOS	0...+70	<605	<11	<120		TTL-TS
HM 6264 P-15	Hit	28-DIP	CMOS	0...+70	<605	<11	<150		TTL-TS
HM1 65641 -2	Mhs	28-DIC	CMOS	-55...+125	<687,5	<44	<85		TTL-TS
HM1 65641 -5	Mhs	28-DIC	CMOS	0...+70	<687,5	<44	<70		TTL-TS
HM1 65641 -9	Mhs	28-DIC	CMOS	-40...+85	<687,5	<44	<85		TTL-TS
HM1 65641 B-2	Mhs	28-DIC	CMOS	-55...+125	<742,5	<44	<70		TTL-TS
HM1 65641 B-5	Mhs	28-DIC	CMOS	0...+70	<742,5	<44	<55		TTL-TS
HM1 65641 B-9	Mhs	28-DIC	CMOS	-40...+85	<742,5	<44	<70		TTL-TS
HM1 65641 C-2	Mhs	28-DIC	CMOS	-55...+125	<687,5	<55	<85		TTL-TS
HM1 65641 C-5	Mhs	28-DIC	CMOS	0...+70	<687,5	<55	<70		TTL-TS
HM1 65641 C-9	Mhs	28-DIC	CMOS	-40...+85	<687,5	<55	<85		TTL-TS
HM1 65641 S-2	Mhs	28-DIC	CMOS	-55...+125	<742,5	<55	<70		TTL-TS
HM1 65641 S-5	Mhs	28-DIC	CMOS	0...+70	<742,5	<55	<55		TTL-TS
HM1 65641 S-9	Mhs	28-DIC	CMOS	-40...+85	<742,5	<55	<70		TTL-TS
HM1 65664 -2	Mhs	28-DIC	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HM1 65664 -5	Mhs	28-DIC	CMOS	0...+70	<275	<55	<55		TTL-TS
HM1 65664 -9	Mhs	28-DIC	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HM1 65664 B-2	Mhs	28-DIC	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HM1 65664 B-5	Mhs	28-DIC	CMOS	0...+70	<275	<55	<45		TTL-TS
HM1 65664 B-9	Mhs	28-DIC	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HM1 65664 C-2	Mhs	28-DIC	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM1 65664 C-5	Mhs	28-DIC	CMOS	0...+70	<412	<82,5	<55		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65664 C-9	Mhs	28-DIC	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM1 65664 S-2	Mhs	28-DIC	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM1 65664 S-5	Mhs	28-DIC	CMOS	0...+70	<412	<82,5	<45		TTL-TS
HM1 65664 S-9	Mhs	28-DIC	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM1 65764 K-5	Mhs	28-DIC	CMOS	0...+70	<550	<165	<35		TTL-TS
HM1 65764 M-2	Mhs	28-DIC	CMOS	-55...+125	<550	<165	<45		TTL-TS
HM1 65764 M-5	Mhs	28-DIC	CMOS	0...+70	<550	<165	<45		TTL-TS
HM1 65764 M-9	Mhs	28-DIC	CMOS	-40...+85	<550	<165	<45		TTL-TS
HM1 65764 N-2	Mhs	28-DIC	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM1 65764 N-5	Mhs	28-DIC	CMOS	0...+70	<550	<165	<55		TTL-TS
HM1 65764 N-9	Mhs	28-DIC	CMOS	-40...+85	<550	<165	<55		TTL-TS
HM3 65641 -2	Mhs	28-DIP	CMOS	-55...+125	<687,5	<44	<85		TTL-TS
HM3 65641 -5	Mhs	28-DIP	CMOS	0...+70	<687,5	<44	<70		TTL-TS
HM3 65641 -9	Mhs	28-DIP	CMOS	-40...+85	<687,5	<44	<85		TTL-TS
HM3 65641 B-2	Mhs	28-DIP	CMOS	-55...+125	<742,5	<44	<70		TTL-TS
HM3 65641 B-5	Mhs	28-DIP	CMOS	0...+70	<742,5	<44	<55		TTL-TS
HM3 65641 B-9	Mhs	28-DIP	CMOS	-40...+85	<747,5	<44	<70		TTL-TS
HM3 65641 C-2	Mhs	28-DIP	CMOS	-55...+125	<687,5	<55	<85		TTL-TS
HM3 65641 C-5	Mhs	28-DIP	CMOS	0...+70	<687,5	<55	<70		TTL-TS
HM3 65641 C-9	Mhs	28-DIP	CMOS	-40...+85	<687,5	<55	<85		TTL-TS
HM3 65641 S-2	Mhs	28-DIP	CMOS	-55...+125	<742,5	<55	<70		TTL-TS
HM3 65641 S-5	Mhs	28-DIP	CMOS	0...+70	<742,5	<55	<55		TTL-TS
HM3 65641 S-9	Mhs	28-DIP	CMOS	-40...+85	<747,5	<55	<70		TTL-TS
HM3 65664 -2	Mhs	28-TDIP	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HM3 65664 -5	Mhs	28-TDIP	CMOS	0...+70	<275	<55	<55		TTL-TS
HM3 65664 -9	Mhs	28-TDIP	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HM3 65664 B-2	Mhs	28-TDIP	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HM3 65664 B-5	Mhs	28-TDIP	CMOS	0...+70	<275	<55	<45		TTL-TS
HM3 65664 B-9	Mhs	28-TDIP	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HM3 65664 C-2	Mhs	28-TDIP	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM3 65664 C-5	Mhs	28-TDIP	CMOS	0...+70	<412	<82,5	<55		TTL-TS
HM3 65664 C-9	Mhs	28-TDIP	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM3 65664 S-2	Mhs	28-TDIP	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM3 65664 S-5	Mhs	28-TDIP	CMOS	0...+70	<412	<82,5	<45		TTL-TS
HM3 65664 S-9	Mhs	28-TDIP	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM3 65764 K-5	Mhs	28-TDIP	CMOS	0...+70	<550	<165	<35		TTL-TS
HM3 65764 M-2	Mhs	28-TDIP	CMOS	-55...+125	<550	<165	<45		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM3 65764 M-5	Mhs	28-TDIP	CMOS	0...+70	<550	<165	<45		TTL-TS
HM3 65764 M-9	Mhs	28-TDIP	CMOS	-40...+85	<550	<165	<45		TTL-TS
HM3 65764 N-2	Mhs	28-TDIP	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM3 65764 N-5	Mhs	28-TDIP	CMOS	0...+70	<550	<165	<55		TTL-TS
HM3 65764 N-9	Mhs	28-TDIP	CMOS	-40...+85	<550	<165	<55		TTL-TS
HM3E 65664 -2	Mhs	28-DIP	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HM3E 65664 -5	Mhs	28-DIP	CMOS	0...+70	<275	<55	<55		TTL-TS
HM3E 65664 -9	Mhs	28-DIP	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HM3E 65664 B-2	Mhs	28-DIP	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HM3E 65664 B-5	Mhs	28-DIP	CMOS	0...+70	<275	<55	<45		TTL-TS
HM3E 65664 B-9	Mhs	28-DIP	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HM3E 65664 C-2	Mhs	28-DIP	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM3E 65664 C-5	Mhs	28-DIP	CMOS	0...+70	<412	<82,5	<55		TTL-TS
HM3E 65664 C-9	Mhs	28-DIP	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM3E 65664 S-2	Mhs	28-DIP	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM3E 65664 S-5	Mhs	28-DIP	CMOS	0...+70	<412	<82,5	<45		TTL-TS
HM3E 65664 S-9	Mhs	28-DIP	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM3E 65764 K-5	Mhs	28-DIP	CMOS	0...+70	<550	<165	<35		TTL-TS
HM3E 65764 M-2	Mhs	28-DIP	CMOS	-55...+125	<550	<165	<45		TTL-TS
HM3E 65764 M-5	Mhs	28-DIP	CMOS	0...+70	<550	<165	<45		TTL-TS
HM3E 65764 M-9	Mhs	28-DIP	CMOS	-40...+85	<550	<165	<45		TTL-TS
HM3E 65764 N-2	Mhs	28-DIP	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM3E 65764 N-5	Mhs	28-DIP	CMOS	0...+70	<550	<165	<55		TTL-TS
HM3E 65764 N-9	Mhs	28-DIP	CMOS	-40...+85	<550	<165	<55		TTL-TS
HMT 65664 -2	Mhs	28-FLAT	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HMT 65664 -5	Mhs	28-FLAT	CMOS	0...+70	<412	<82,5	<55		TTL-TS
HMT 65664 -9	Mhs	28-FLAT	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HMT 65664 B-2	Mhs	28-FLAT	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HMT 65664 B-5	Mhs	28-FLAT	CMOS	0...+70	<412	<82,5	<45		TTL-TS
HMT 65664 B-9	Mhs	28-FLAT	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HMT 65664 C-2	Mhs	28-FLAT	CMOS	-55...+125	<550	<110	<55		TTL-TS
HMT 65664 C-5	Mhs	28-FLAT	CMOS	0...+70	<550	<110	<55		TTL-TS
HMT 65664 C-9	Mhs	28-FLAT	CMOS	-40...+85	<550	<110	<55		TTL-TS
HMT 65664 S-2	Mhs	28-FLAT	CMOS	-55...+125	<550	<110	<45		TTL-TS
HMT 65664 S-5	Mhs	28-FLAT	CMOS	0...+70	<550	<110	<45		TTL-TS
HMT 65664 S-9	Mhs	28-FLAT	CMOS	-40...+85	<550	<110	<45		TTL-TS
HMT 65764 K-5	Mhs	28-FLAT	CMOS	0...+70	<550	<165	<35		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HMT 65764 M-2	Mhs	28-FLAT	CMOS	-55...+125	<550	<165	<45		TTL-TS
HMT 65764 M-5	Mhs	28-FLAT	CMOS	0...+70	<550	<165	<45		TTL-TS
HMT 65764 M-9	Mhs	28-FLAT	CMOS	-40...+85	<550	<165	<45		TTL-TS
HMT 65764 N-2	Mhs	28-FLAT	CMOS	-55...+125	<550	<165	<55		TTL-TS
HMT 65764 N-5	Mhs	28-FLAT	CMOS	0...+70	<550	<165	<55		TTL-TS
HMT 65764 N-9	Mhs	28-FLAT	CMOS	-40...+85	<550	<165	<55		TTL-TS
KM 6264 A-10	Sam	28-DIP	CMOS	0...+70	<385	<5,5	<100		TTL-TS
KM 6264 A-12	Sam	28-DIP	CMOS	0...+70	<385	<5,5	<120		TTL-TS
KM 6264 A-15	Sam	28-DIP	CMOS	0...+70	<385	<5,5	<150		TTL-TS
KM 6264 AL-10	Sam	28-DIP	CMOS	0...+70	<385	<550µ	<100		TTL-TS
KM 6264 AL-12	Sam	28-DIP	CMOS	0...+70	<385	<550µ	<120		TTL-TS
KM 6264 AL-15	Sam	28-DIP	CMOS	0...+70	<385	<550µ	<150		TTL-TS
M5M 5165 FP-10	Mit	28-FLAT	CMOS	0...+70	<275	<11	<100		TTL-TS
M5M 5165 FP-10L	Mit	28-FLAT	CMOS	0...+70	<275	<0,11	<100		TTL-TS
M5M 5165 FP-12	Mit	28-FLAT	CMOS	0...+70	<275	<11	<120		TTL-TS
M5M 5165 FP-12L	Mit	28-FLAT	CMOS	0...+70	<275	<0,11	<120		TTL-TS
M5M 5165 FP-15	Mit	28-FLAT	CMOS	0...+70	<275	<11	<150		TTL-TS
M5M 5165 FP-15L	Mit	28-FLAT	CMOS	0...+70	<275	<0,11	<150		TTL-TS
M5M 5165 FP-70	Mit	28-FLAT	CMOS	0...+70	<275	<11	<70		TTL-TS
M5M 5165 FP-70L	Mit	28-FLAT	CMOS	0...+70	<275	<0,11	<70		TTL-TS
M5M 5165 P-10	Mit	28-DIP	CMOS	0...+70	<275	<11	<100		TTL-TS
M5M 5165 P-10L	Mit	28-DIP	CMOS	0...+70	<275	<0,11	<100		TTL-TS
M5M 5165 P-12	Mit	28-DIP	CMOS	0...+70	<275	<11	<120		TTL-TS
M5M 5165 P-12L	Mit	28-DIP	CMOS	0...+70	<275	<0,11	<120		TTL-TS
M5M 5165 P-15	Mit	28-DIP	CMOS	0...+70	<275	<11	<150		TTL-TS
M5M 5165 P-15L	Mit	28-DIP	CMOS	0...+70	<275	<0,11	<150		TTL-TS
M5M 5165 P-70	Mit	28-DIP	CMOS	0...+70	<275	<11	<70		TTL-TS
M5M 5165 P-70L	Mit	28-DIP	CMOS	0...+70	<275	<0,11	<70		TTL-TS
M5M 5178 P-35	Mit	28-TDIP	CMOS	0...+70	<660	<137,5	<35		TTL-TS
M5M 5178 P-45	Mit	28-TDIP	CMOS	0...+70	<660	<137,5	<45		TTL-TS
M5M 5178 P-55	Mit	28-TDIP	CMOS	0...+70	<660	<137,5	<55		TTL-TS
NMC 6164 AN-45	Nsc	28-DIP	CMOS	0...+70	<275	<22	<45		TTL-TS
NMC 6164 AN-45 L	Nsc	28-DIP	CMOS	0...+70	<275	<11	<45		TTL-TS
NMC 6164 AN-55	Nsc	28-DIP	CMOS	0...+70	<275	<22	<55		TTL-TS
NMC 6164 AN-55 L	Nsc	28-DIP	CMOS	0...+70	<275	<11	<55		TTL-TS
NMC 6164 AN-70	Nsc	28-DIP	CMOS	0...+70	<275	<22	<70		TTL-TS
NMC 6164 AN-70 L	Nsc	28-DIP	CMOS	0...+70	<275	<11	<70		TTL-TS

6164 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 6164 J-10	Nsc	28-DIC	CMOS	0...+70	<360	<22	<100		TTL-TS
NMC 6164 J-12	Nsc	28-DIC	CMOS	0...+70	<360	<22	<120		TTL-TS
NMC 6164 J-15	Nsc	28-DIC	CMOS	0...+70	<360	<22	<150		TTL-TS
NMC 6164 LJ-10	Nsc	28-DIC	CMOS	0...+70	<360	<11	<100		TTL-TS
NMC 6164 LJ-12	Nsc	28-DIC	CMOS	0...+70	<360	<11	<120		TTL-TS
NMC 6164 LJ-15	Nsc	28-DIC	CMOS	0...+70	<360	<11	<150		TTL-TS
NMC 6164 N-10	Nsc	28-DIP	CMOS	0...+70	<360	<22	<100		TTL-TS
NMC 6164 N-12	Nsc	28-DIP	CMOS	0...+70	<360	<22	<120		TTL-TS
NMC 6164 N-15	Nsc	28-DIP	CMOS	0...+70	<360	<22	<150		TTL-TS
NMC 6164 LN-10	Nsc	28-DIP	CMOS	0...+70	<360	<11	<100		TTL-TS
NMC 6164 LN-12	Nsc	28-DIP	CMOS	0...+70	<360	<11	<120		TTL-TS
NMC 6164 LN-15	Nsc	28-DIP	CMOS	0...+70	<360	<11	<150		TTL-TS
TMM 2063 P-10	Tos	28-TDIP	NMOS	0...+70	<80	<10	<100		TTL-TS
TMM 2063 P-12	Tos	28-TDIP	NMOS	0...+70	<80	<10	<120		TTL-TS
TMM 2063 P-15	Tos	28-TDIP	NMOS	0...+70	<80	<10	<150		TTL-TS
TMM 2064 P-10	Tos	28-DIP	NMOS	0...+70	<80	<10	<100		TTL-TS
TMM 2064 P-12	Tos	28-DIP	NMOS	0...+70	<80	<10	<120		TTL-TS
TMM 2064 P-15	Tos	28-DIP	NMOS	0...+70	<80	<10	<150		TTL-TS
TMM 2088 P-35	Tos	28-TDIP	NMOS	0...+70	<135	<15	<35		TTL-TS
TMM 2088 P-45	Tos	28-TDIP	NMOS	0...+70	<135	<15	<45		TTL-TS
TMM 2088 P-55	Tos	28-TDIP	NMOS	0...+70	<135	<15	<55		TTL-TS

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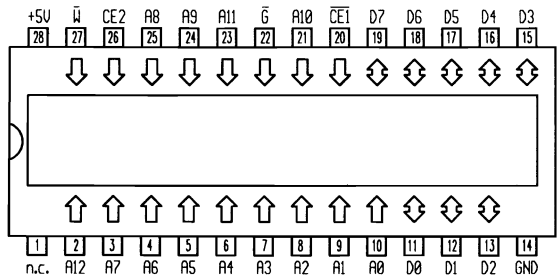


$\overline{W}$	$\overline{CE1}$	CE2	$\overline{G}$	D_n	Power	Mode
X	H	X	X	Hi-Z	standby	deselect
X	X	L	X	Hi-Z	standby	deselect
H	L	H	H	Hi-Z	active	read
H	L	H	L	data out	active	read
L	L	H	X	data in	active	write

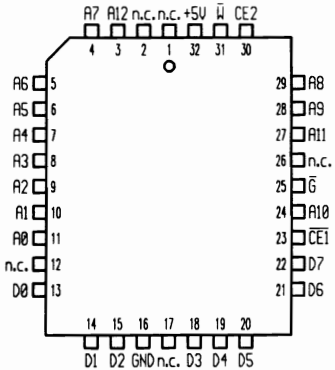
6164 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
FCB 61C65-45 P	Phi	28-DIP	CMOS	0...+70	<385	<16,5	<45		TTL-TS
FCB 61C65-45 T	Phi	28-FLAT	CMOS	0...+70	<385	<16,5	<45		TTL-TS
FCB 61C65-55 P	Phi	28-DIP	CMOS	0...+70	<385	<16,5	<55		TTL-TS
FCB 61C65-55 T	Phi	28-FLAT	CMOS	0...+70	<385	<16,5	<55		TTL-TS
FCB 61C65-70 P	Phi	28-DIP	CMOS	0...+70	<385	<16,5	<70		TTL-TS
FCB 61C65-70 T	Phi	28-FLAT	CMOS	0...+70	<385	<16,5	<70		TTL-TS
FCB 61C65L-45 P	Phi	28-DIP	CMOS	0...+70	<385	<0,55	<45		TTL-TS
FCB 61C65L-45 T	Phi	28-FLAT	CMOS	0...+70	<385	<0,55	<45		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
FCB 61C65L-55 P	Phi	28-DIP	CMOS	0...+70	<385	<0,55	<55		TTL-TS
FCB 61C65L-55 T	Phi	28-FLAT	CMOS	0...+70	<385	<0,55	<55		TTL-TS
FCB 61C65L-70 P	Phi	28-DIP	CMOS	0...+70	<385	<0,55	<70		TTL-TS
FCB 61C65L-70 T	Phi	28-FLAT	CMOS	0...+70	<385	<0,55	<70		TTL-TS
FCB 61C65LL-45 P	Phi	28-DIP	CMOS	0...+70	<385	<5,5µ	<45		TTL-TS
FCB 61C65LL-45 T	Phi	28-FLAT	CMOS	0...+70	<385	<5,5µ	<45		TTL-TS
FCB 61C65LL-55 P	Phi	28-DIP	CMOS	0...+70	<385	<5,5µ	<55		TTL-TS
FCB 61C65LL-55 T	Phi	28-FLAT	CMOS	0...+70	<385	<5,5µ	<55		TTL-TS
FCB 61C65LL-70 P	Phi	28-DIP	CMOS	0...+70	<385	<5,5µ	<70		TTL-TS
FCB 61C65LL-70 T	Phi	28-FLAT	CMOS	0...+70	<385	<5,5µ	<70		TTL-TS
IMS 1630 LH-45	Inm	28-FLAT	CMOS	0...+70	<495	<110	<45		TTL-TS
IMS 1630 LH-55	Inm	28-FLAT	CMOS	0...+70	<495	<110	<55		TTL-TS
IMS 1630 LH-70	Inm	28-FLAT	CMOS	0...+70	<495	<110	<70		TTL-TS
IMS 1630 LH-100	Inm	28-FLAT	CMOS	0...+70	<495	<110	<100		TTL-TS
IMS 1630 LH-120	Inm	28-FLAT	CMOS	0...+70	<495	<110	<120		TTL-TS
IMS 1630 LP-45	Inm	28-DIP	CMOS	0...+70	<495	<110	<45		TTL-TS
IMS 1630 LP-45Z	Inm	28-TDIP	CMOS	0...+70	<495	<110	<45		TTL-TS
IMS 1630 LP-55	Inm	28-DIP	CMOS	0...+70	<495	<110	<55		TTL-TS
IMS 1630 LP-55Z	Inm	28-TDIP	CMOS	0...+70	<495	<110	<55		TTL-TS
IMS 1630 LP-70	Inm	28-DIP	CMOS	0...+70	<495	<110	<70		TTL-TS
IMS 1630 LP-70Z	Inm	28-TDIP	CMOS	0...+70	<495	<110	<70		TTL-TS
IMS 1630 LP-100	Inm	28-DIP	CMOS	0...+70	<495	<110	<100		TTL-TS
IMS 1630 LP-100Z	Inm	28-TDIP	CMOS	0...+70	<495	<110	<100		TTL-TS
IMS 1630 LP-120	Inm	28-DIP	CMOS	0...+70	<495	<110	<120		TTL-TS
IMS 1630 LP-120Z	Inm	28-TDIP	CMOS	0...+70	<495	<110	<120		TTL-TS
IMS 1630 LS-45M	Inm	28-DIC	CMOS	-55...+125	<467,5	<165	<45		TTL-TS
IMS 1630 LS-55M	Inm	28-DIC	CMOS	-55...+125	<467,5	<165	<55		TTL-TS
IMS 1630 LS-70M	Inm	28-DIC	CMOS	-55...+125	<467,5	<165	<70		TTL-TS
IMS 1630 S-45M	Inm	28-DIC	CMOS	-55...+125	<467,5	<165	<45		TTL-TS
IMS 1630 S-55M	Inm	28-DIC	CMOS	-55...+125	<467,5	<165	<55		TTL-TS
IMS 1630 S-70M	Inm	28-DIC	CMOS	-55...+125	<467,5	<165	<70		TTL-TS
MCM 60L64 P-10	Mot	28-DIP	CMOS	0...+70	<192,5	<5,5µ	<100		TTL-TS
MCM 60L64 P-12	Mot	28-DIP	CMOS	0...+70	<192,5	<5,5µ	<120		TTL-TS
MCM 60L64 P-15	Mot	28-DIP	CMOS	0...+70	<192,5	<5,5µ	<150		TTL-TS
MCM 6064 P-10	Mot	28-DIP	CMOS	0...+70	<247,5	<16,5	<100		TTL-TS
MCM 6064 P-12	Mot	28-DIP	CMOS	0...+70	<220	<16,5	<120		TTL-TS
MCM 6064 P-15	Mot	28-DIP	CMOS	0...+70	<192,5	<16,5	<150		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6164 C-45	Mot	28-DIC	CMOS	0...+70	<495	<16,5	<45		TTL-TS
MCM 6164 C-55	Mot	28-DIC	CMOS	0...+70	<495	<16,5	<55		TTL-TS
MCM 6164 CC-45	Mot	28-DIC	CMOS	-40...+85	<495	<16,5	<45		TTL-TS
MCM 6164 CC-55	Mot	28-DIC	CMOS	-40...+85	<495	<16,5	<55		TTL-TS
MCM 61L64 C-45	Mot	28-DIC	CMOS	0...+70	<495	<275µ	<45		TTL-TS
MCM 61L64 C-55	Mot	28-DIC	CMOS	0...+70	<495	<275µ	<55		TTL-TS
MCM 61L64 CC-45	Mot	28-DIC	CMOS	-40...+85	<495	<275µ	<45		TTL-TS
MCM 61L64 CC-55	Mot	28-DIC	CMOS	-40...+85	<495	<275µ	<55		TTL-TS
MCM 6264 J-35	Mot	28-FLAT	CMOS	0...+70	<605	<110	<35		TTL-TS
MCM 6264 J-45	Mot	28-FLAT	CMOS	0...+70	<550	<110	<45		TTL-TS
MCM 6264 P-35	Mot	28-TDIP	CMOS	0...+70	<605	<110	<35		TTL-TS
MCM 6264 P-45	Mot	28-TDIP	CMOS	0...+70	<550	<110	<45		TTL-TS
MK 48H64L N-120	Sgs	28-DIP	CMOS	0...+70	<495	<27,5	<120		TTL-TS
MK 48H64L N-70	Sgs	28-DIP	CMOS	0...+70	<550	<27,5	<70		TTL-TS
MK 48H64L S-120	Sgs	28-FLAT	CMOS	0...+70	<495	<27,5	<120		TTL-TS
MK 48H64L S-70	Sgs	28-FLAT	CMOS	0...+70	<550	<27,5	<70		TTL-TS
MK 48H64 N-120	Sgs	28-DIP	CMOS	0...+70	<495	<27,5	<120		TTL-TS
MK 48H64 N-35	Sgs	28-DIP	CMOS	0...+70	<495	<55	<35		TTL-TS
MK 48H64 N-45	Sgs	28-DIP	CMOS	0...+70	<495	<55	<45		TTL-TS
MK 48H64 N-55	Sgs	28-DIP	CMOS	0...+70	<495	<55	<55		TTL-TS
MK 48H64 N-70	Sgs	28-DIP	CMOS	0...+70	<495	<55	<70		TTL-TS
MK 48H64 P-35	Sgs	28-DIC	CMOS	0...+70	<495	<55	<35		TTL-TS
MK 48H64 P-45	Sgs	28-DIC	CMOS	0...+70	<495	<55	<45		TTL-TS
MK 48H64 P-55	Sgs	28-DIC	CMOS	0...+70	<495	<55	<55		TTL-TS
MK 48H64 P-70	Sgs	28-DIC	CMOS	0...+70	<495	<55	<70		TTL-TS
MK 48H64 S-120	Sgs	28-FLAT	CMOS	0...+70	<495	<27,5	<120		TTL-TS
MK 48H64 S-70	Sgs	28-FLAT	CMOS	0...+70	<550	<27,5	<70		TTL-TS
MK 48H65 N-35	Sgs	28-TDIP	CMOS	0...+70	<495	<55	<35		TTL-TS
MK 48H65 N-45	Sgs	28-TDIP	CMOS	0...+70	<495	<55	<45		TTL-TS
MK 48H65 N-55	Sgs	28-TDIP	CMOS	0...+70	<495	<55	<55		TTL-TS
MK 48H65 N-70	Sgs	28-TDIP	CMOS	0...+70	<495	<55	<70		TTL-TS
MN 4464-08 L	Mat	28-DIP	CMOS	0...+70	<165	<16,5	<80		TTL-TS
MN 4464-08 LL	Mat	28-DIP	CMOS	0...+70	<165	<16,5	<80		TTL-TS
MN 4464 S-08 L	Mat	28-FLAT	CMOS	0...+70	<165	<16,5	<80		TTL-TS
MN 4464 S-08 LL	Mat	28-FLAT	CMOS	0...+70	<165	<16,5	<80		TTL-TS
TC 5563 APL-10	Tos	28-TDIP	CMOS	0...+70	<27,5	<0,55	<100		TTL-TS
TC 5563 APL-10L	Tos	28-TDIP	CMOS	0...+70	<27,5	<5,5µ	<100		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 5563 APL-12	Tos	28-TDIP	CMOS	0...+70	<27,5	<0,55	<120		TTL-TS
TC 5563 APL-12L	Tos	28-TDIP	CMOS	0...+70	<27,5	<5,5µ	<120		TTL-TS
TC 5563 APL-15	Tos	28-TDIP	CMOS	0...+70	<27,5	<0,55	<150		TTL-TS
TC 5563 APL-15L	Tos	28-TDIP	CMOS	0...+70	<27,5	<5,5µ	<150		TTL-TS
TC 5564 AFL-15	Tos	28-FLAT	CMOS	0...+70	<27,5	<5,5µ	<150		TTL-TS
TC 5564 AFL-20	Tos	28-FLAT	CMOS	0...+70	<27,5	<5,5µ	<200		TTL-TS
TC 5564 APL-15	Tos	28-DIP	CMOS	0...+70	<27,5	<5,5µ	<150		TTL-TS
TC 5564 APL-20	Tos	28-DIP	CMOS	0...+70	<27,5	<5,5µ	<200		TTL-TS
TC 5565 AFL-10	Tos	28-FLAT	CMOS	0...+70	<27,5	<0,55	<100		TTL-TS
TC 5565 AFL-10L	Tos	28-FLAT	CMOS	0...+70	<27,5	<5,5µ	<100		TTL-TS
TC 5565 AFL-12	Tos	28-FLAT	CMOS	0...+70	<27,5	<0,55	<120		TTL-TS
TC 5565 AFL-12L	Tos	28-FLAT	CMOS	0...+70	<27,5	<5,5µ	<120		TTL-TS
TC 5565 AFL-15	Tos	28-FLAT	CMOS	0...+70	<27,5	<0,55	<150		TTL-TS
TC 5565 AFL-15L	Tos	28-FLAT	CMOS	0...+70	<27,5	<5,5µ	<150		TTL-TS
TC 5565 APL-10	Tos	28-DIP	CMOS	0...+70	<27,5	<0,55	<100		TTL-TS
TC 5565 APL-10L	Tos	28-DIP	CMOS	0...+70	<27,5	<5,5µ	<100		TTL-TS
TC 5565 APL-12	Tos	28-DIP	CMOS	0...+70	<27,5	<0,55	<120		TTL-TS
TC 5565 APL-12L	Tos	28-DIP	CMOS	0...+70	<27,5	<5,5µ	<120		TTL-TS
TC 5565 APL-15	Tos	28-DIP	CMOS	0...+70	<27,5	<0,55	<150		TTL-TS
TC 5565 APL-15L	Tos	28-DIP	CMOS	0...+70	<27,5	<5,5µ	<150		TTL-TS
6164-55 BXAJC	Mot	28-DIC	CMOS	-55...+125	<660	<16,5	<55		TTL-TS
6164-70 BXAJC	Mot	28-DIC	CMOS	-55...+125	<660	<16,5	<70		TTL-TS

6164 — 8192x8-Bit static RAM

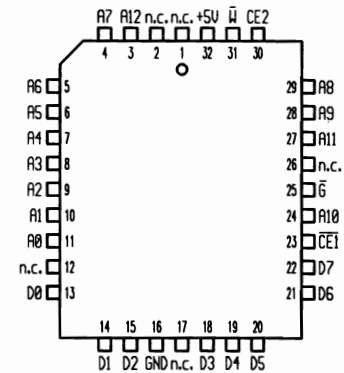


$\overline{W}$	$\overline{CS1}$	CS2	$\overline{G}$	D_n	Mode
X	H	X	X	Hi-Z	not selected (power down)
X	X	L	X	Hi-Z	not selected (power down)
H	L	H	H	Hi-Z	output disabled
H	L	H	L	data out	read
L	L	H	X	data in	write

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65641 -2	Mhs	32-LCC	CMOS	-55...+125	<687,5	<44	<85		TTL-TS
HM4 65641 -5	Mhs	32-LCC	CMOS	0...+70	<687,5	<44	<70		TTL-TS
HM4 65641 -9	Mhs	32-LCC	CMOS	-40...+85	<687,5	<44	<85		TTL-TS
HM4 65641 B-2	Mhs	32-LCC	CMOS	-55...+125	<742,5	<44	<70		TTL-TS
HM4 65641 B-5	Mhs	32-LCC	CMOS	0...+70	<742,5	<44	<55		TTL-TS
HM4 65641 B-9	Mhs	32-LCC	CMOS	-40...+85	<747,5	<44	<70		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM4 65641 C-2	Mhs	32-LCC	CMOS	-55...+125	<687,5	<55	<85		TTL-TS
HM4 65641 C-5	Mhs	32-LCC	CMOS	0...+70	<687,5	<55	<70		TTL-TS
HM4 65641 C-9	Mhs	32-LCC	CMOS	-40...+85	<687,5	<55	<85		TTL-TS
HM4 65641 S-2	Mhs	32-LCC	CMOS	-55...+125	<742,5	<55	<70		TTL-TS
HM4 65641 S-5	Mhs	32-LCC	CMOS	0...+70	<742,5	<55	<55		TTL-TS
HM4 65641 S-9	Mhs	32-LCC	CMOS	-40...+85	<747,5	<55	<70		TTL-TS
HM4 65664 -2	Mhs	32-LCC	CMOS	-55...+125	<412	<82,5	<55		TTL-TS
HM4 65664 -5	Mhs	32-LCC	CMOS	0...+70	<275	<55	<55		TTL-TS
HM4 65664 -9	Mhs	32-LCC	CMOS	-40...+85	<412	<82,5	<55		TTL-TS
HM4 65664 B-2	Mhs	32-LCC	CMOS	-55...+125	<412	<82,5	<45		TTL-TS
HM4 65664 B-5	Mhs	32-LCC	CMOS	0...+70	<275	<55	<45		TTL-TS
HM4 65664 B-9	Mhs	32-LCC	CMOS	-40...+85	<412	<82,5	<45		TTL-TS
HM4 65664 C-2	Mhs	32-LCC	CMOS	-55...+125	<550	<110	<55		TTL-TS
HM4 65664 C-5	Mhs	32-LCC	CMOS	0...+70	<412	<82,5	<55		TTL-TS
HM4 65664 C-9	Mhs	32-LCC	CMOS	-40...+85	<550	<110	<55		TTL-TS
HM4 65664 S-2	Mhs	32-LCC	CMOS	-55...+125	<550	<110	<45		TTL-TS
HM4 65664 S-5	Mhs	32-LCC	CMOS	0...+70	<412	<82,5	<55		TTL-TS
HM4 65664 S-9	Mhs	32-LCC	CMOS	-40...+85	<550	<110	<45		TTL-TS
HM4 65764 K-5	Mhs	32-LCC	CMOS	0...+70	<550	<165	<35		TTL-TS
HM4 65764 M-2	Mhs	32-LCC	CMOS	-55...+125	<550	<165	<45		TTL-TS
HM4 65764 M-5	Mhs	32-LCC	CMOS	0...+70	<550	<165	<45		TTL-TS
HM4 65764 M-9	Mhs	32-LCC	CMOS	-40...+85	<550	<165	<45		TTL-TS
HM4 65764 N-2	Mhs	32-LCC	CMOS	-55...+125	<550	<165	<55		TTL-TS
HM4 65764 N-5	Mhs	32-LCC	CMOS	0...+70	<550	<165	<55		TTL-TS
HM4 65764 N-9	Mhs	32-LCC	CMOS	-40...+85	<550	<165	<55		TTL-TS

6164 — 8192x8-Bit static RAM



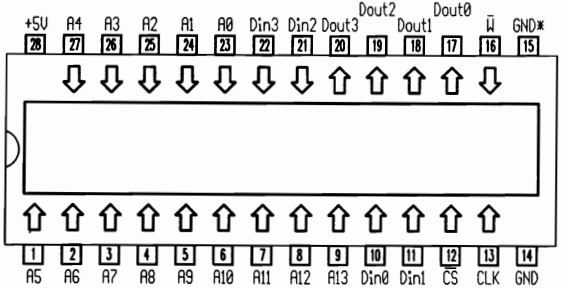
$\overline{W}$	$\overline{CE1}$	CE2	$\overline{G}$	D_n	Power	Mode
X	H	X	X	HI-Z	standby	deselect
X	X	L	X	HI-Z	standby	deselect
H	L	H	H	HI-Z	active	read
H	L	H	L	data out	active	read
L	L	H	X	data in	active	write

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IMS 1630 LN-45M	Inm	32-LCC	CMOS	-55...+125	<467,5	<165	<45		TTL-TS
IMS 1630 LN-55M	Inm	32-LCC	CMOS	-55...+125	<467,5	<165	<55		TTL-TS
IMS 1630 LN-70M	Inm	32-LCC	CMOS	-55...+125	<467,5	<165	<70		TTL-TS
IMS 1630 N-45M	Inm	32-LCC	CMOS	-55...+125	<467,5	<165	<45		TTL-TS
IMS 1630 N-55M	Inm	32-LCC	CMOS	-55...+125	<467,5	<165	<55		TTL-TS
IMS 1630 N-70M	Inm	32-LCC	CMOS	-55...+125	<467,5	<165	<70		TTL-TS

6164 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
6164-55 BUAJC	Mot	32-LCC	CMOS	-55...+125	<660	<16,5	<55		TTL-TS
6164-70 BUAJC	Mot	32-LCC	CMOS	-55...+125	<660	<16,5	<70		TTL-TS

6292 — 16384x4-Bit synch. stat.RAM with Latch

* for minimum cycle/low noise applications, GND* should be isolated from GND

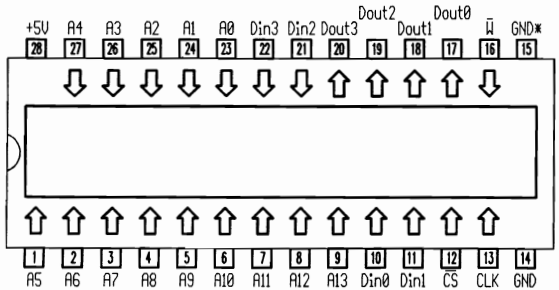


CS	W	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

6292 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6292 C-25	Mot	28-TDIC	CMOS	0...+70	<660		<25		LATCH
MCM 6292 C-30	Mot	28-TDIC	CMOS	0...+70	<660		<30		LATCH
MCM 6292 C-35	Mot	28-TDIC	CMOS	0...+70	<660		<35		LATCH
MCM 6292 J-25	Mot	28-FLAT	CMOS	0...+70	<660		<25		LATCH
MCM 6292 J-30	Mot	28-FLAT	CMOS	0...+70	<660		<30		LATCH
MCM 6292 J-35	Mot	28-FLAT	CMOS	0...+70	<660		<35		LATCH

6293 — 16384x4-Bit synch. stat. RAM w. Latch

* for minimum cycle/low noise applications, GND* should be isolated from GND

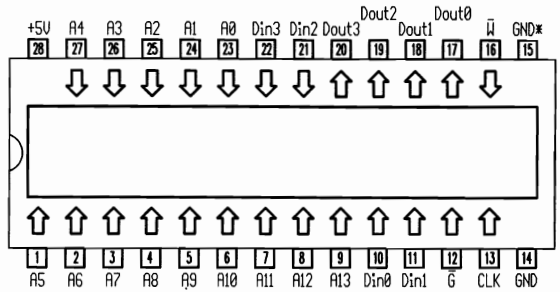


$\overline{CS}$	$\overline{W}$	D_n	Mode
H	X	Hi-Z	standby
L	H	data out	read
L	L	data in	write

6293 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6293 C-25	Mot	28-TDIP	CMOS	0...+70	<660		<25		Register
MCM 6293 C-30	Mot	28-TDIP	CMOS	0...+70	<660		<30		Register
MCM 6293 C-35	Mot	28-TDIP	CMOS	0...+70	<660		<35		Register
MCM 6293 J-25	Mot	28-FLAT	CMOS	0...+70	<660		<25		Register
MCM 6293 J-30	Mot	28-FLAT	CMOS	0...+70	<660		<30		Register
MCM 6293 J-35	Mot	28-FLAT	CMOS	0...+70	<660		<35		Register

6294 — 16384x4-Bit synch. stat. RAM w. Register

* for minimum cycle/low noise applications, GND* should be isolated from GND

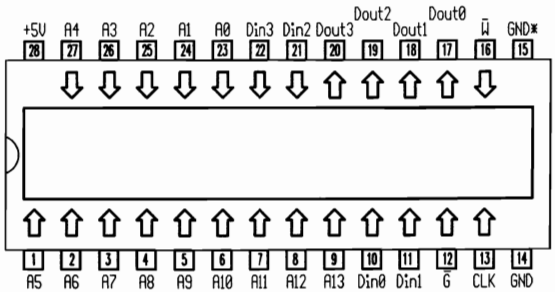


$\overline{W}$	$\overline{G}$	D_n	Mode
H	H	Hi-Z	output disable
H	L	data out	read
L	X	data in	write

6294 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6294 C-25	Mot	28-TDIP	CMOS	0...+70	<660		<25		Register
MCM 6294 C-30	Mot	28-TDIP	CMOS	0...+70	<660		<30		Register
MCM 6294 C-35	Mot	28-TDIP	CMOS	0...+70	<660		<35		Register
MCM 6294 J-25	Mot	28-FLAT	CMOS	0...+70	<660		<25		Register
MCM 6294 J-30	Mot	28-FLAT	CMOS	0...+70	<660		<30		Register
MCM 6294 J-35	Mot	28-FLAT	CMOS	0...+70	<660		<35		Register

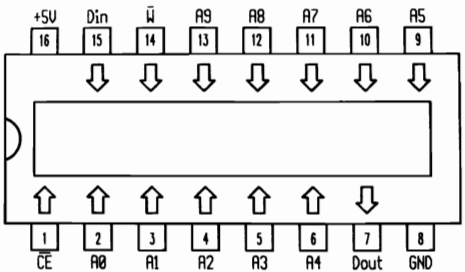
6295 — 16384x4-Bit synch. stat. RAM with Latch

* for minimum cycle/low noise applications, GND* should be isolated from GND



W	G	D_n	Mode
H	H	Hi-Z	output disable
H	L	data out	read
L	X	data in	write

6508 — 1024x1-Bit static RAM

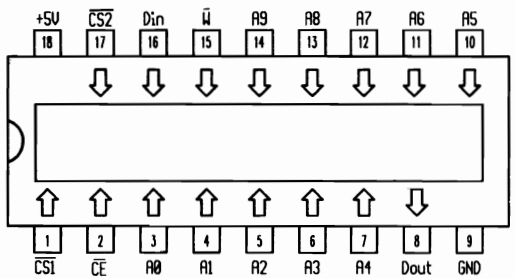


6295 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6295 J-25	Mot	28-FLAT	CMOS	0...+70	<660		<25		Latch
MCM 6295 J-30	Mot	28-FLAT	CMOS	0...+70	<660		<30		Latch
MCM 6295 J-35	Mot	28-FLAT	CMOS	0...+70	<660		<35		Latch
MCM 6295 P-25	Mot	28-TDIP	CMOS	0...+70	<660		<25		Latch
MCM 6295 P-30	Mot	28-TDIP	CMOS	0...+70	<660		<30		Latch
MCM 6295 P-35	Mot	28-TDIP	CMOS	0...+70	<660		<35		Latch

6508 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IM 6508	Isi	16-DIP	CMOS	-40...+85	<0,55	<55µ	<475		TTL-TS
IM 6508-1	Isi	16-DIP	CMOS	-40...+85	<0,55	<5,5µ	<310		TTL-TS
IM 6508 A	Isi	16-DIP	CMOS	-40...+85	<5,5	<1,1	<360		TTL-TS
IM 6508 A-1	Isi	16-DIP	CMOS	-40...+85	<1,1	<11µ	<205		TTL-TS
IM 65X08 CD	Isi	16-DIC	CMOS	0...+75	<21	<5,25	<450		TTL-TS
IM 65X08 CJ	Isi	16-DIC	CMOS	0...+75	<21	<5,25	<450		TTL-TS
MB 8401 E	Fui	16-DIP	CMOS	-40...+85	<16,5	<55µ	<290		TTL-TS
MB 8401 H	Fui	16-DIP	CMOS	-40...+85	<16,5	<0,55	<165		TTL-TS

6508 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MB 8401 N	Fui	16-DIP	CMOS	-40...+85	<16,5	<0,55	<450		TTL-TS
MCM 6508 C-25	Mot	16-DIC	CMOS	0...+70		<50µ	<250		TTL-TS
MCM 6508 C-30	Mot	16-DIC	CMOS	0...+70		<0,5	<300		TTL-TS
MCM 6508 C-46	Mot	16-DIC	CMOS	0...+70		<0,5	<460		TTL-TS
MCM 146508-1 L	Mot	16-DIC	CMOS	-40...+85		<5,5µ	<300		TTL-TS
MCM 146508-1 P	Mot	16-DIP	CMOS	-40...+85		<5,5µ	<300		TTL-TS
MCM 146508-2 L	Mot	16-DIC	CMOS	-55...+125		<55µ	<300		TTL-TS
MCM 146508-2 P	Mot	16-DIP	CMOS	-55...+125		<55µ	<300		TTL-TS
MCM 146508 L	Mot	16-DIC	CMOS	-40...+85		<55µ	<460		TTL-TS
MCM 146508 P	Mot	16-DIP	CMOS	-40...+85		<55µ	<460		TTL-TS
MM 74C929-3 J	Nsc	16-DIC	CMOS	-40...+85			<315		TTL-TS
MM 74C929-3 N	Nsc	16-DIP	CMOS	-40...+85			<315		TTL-TS
MM 74C929 J	Nsc	16-DIC	CMOS	-40...+85			<240		TTL-TS
MM 74C929 N	Nsc	16-DIP	CMOS	-40...+85			<240		TTL-TS
NMC 6508-5 J	Nsc	16-DIC	CMOS	0...+70	<21	<5,25	<450		TTL-TS
NMC 6508-5 N	Nsc	16-DIP	CMOS	0...+70	<21	<5,25	<450		TTL-TS
TC 5508 P	Tos	16-DIP	CMOS	-30...+85	<55	<0,55	<450		TTL-TS
TC 5508 P-1	Tos	16-DIP	CMOS	-30...+85	<55	<0,55	<700		TTL-TS
TC 5508 P-4	Tos	16-DIP	CMOS	-30...+85	<55	<55µ	<450		TTL-TS
µPD 443	Nec	16-DIP	CMOS	-40...+85	<55		<465		TTL-TS
µPD 443-1	Nec	16-DIP	CMOS	-40...+85	<55		<307		TTL-TS
µPD 443-2	Nec	16-DIP	CMOS	-40...+85	<55		<255		TTL-TS
µPD 443-3	Nec	16-DIP	CMOS	-40...+85	<55		<205		TTL-TS

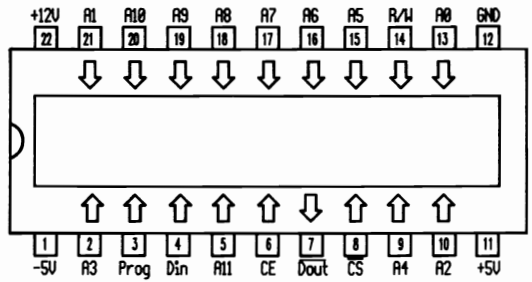
6518 — 1024x1-Bit static RAM



6518 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IM 6518	Isi	18-DIP	CMOS	-40...+85	<0,55	<0,55	<475		TTL-TS
IM 6518-1	Isi	18-DIP	CMOS	-40...+85	<0,055	<5,5µ	<310		TTL-TS
IM 6518 A	Isi	18-DIP	CMOS	-40...+85	<5,5	<0,11	<360		CMOS
IM 6518 A-1	Isi	18-DIP	CMOS	-40...+85	<1,1	<0,011	<205		CMOS
IM 65X18 CD	Isi	18-DIC	CMOS	0...+75	<21	<0,5	<300		TTL-TS
IM 65X18 CJ	Isi	18-DIC	CMOS	0...+75	<21	<0,5	<300		TTL-TS
MB 8411 E	Fui	18-DIP	CMOS	-40...+85		<55µ	<290		TTL-TS
MB 8411 H	Fui	18-DIP	CMOS	-40...+85		<55µ	<165		TTL-TS

6518 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MB 8411 N	Fui	18-DIP	CMOS	-40...+85		<55µ	<450		TTL-TS
MCM 6518 C-25	Mot	18-DIC	CMOS	0...+70		<50µ	<250		TTL-TS
MCM 6518 C-30	Mot	18-DIC	CMOS	0...+70		<0,5	<300		TTL-TS
MCM 6518 C-46	Mot	18-DIC	CMOS	0...+70		<0,5	<460		TTL-TS
MCM 146518-1 L	Mot	18-DIC	CMOS	-40...+85		<5,5µ	<300		TTL-TS
MCM 146518-1 P	Mot	18-DIP	CMOS	-40...+85		<5,5µ	<300		TTL-TS
MCM 146518 L	Mot	18-DIC	CMOS	-40...+85		<0,055	<460		TTL-TS
MCM 146518 P	Mot	18-DIP	CMOS	-40...+85		<0,055	<460		TTL-TS
MM 74C930-3 J	Nsc	18-DIC	CMOS	-40...+85	<0,55		<315		TTL-TS
MM 74C930-3 N	Nsc	18-DIP	CMOS	0...+70	<0,55		<315		TTL-TS
MM 74C930 J	Nsc	18-DIC	CMOS	-40...+85	<0,055		<240		TTL-TS
MM 74C930 N	Nsc	18-DIP	CMOS	-40...+85	<0,055		<240		TTL-TS
NMC 6518-5 J	Nsc	18-DIC	CMOS	0...+75	<21	<0,5	<310		TTL-TS
NMC 6518-5 N	Nsc	18-DIP	CMOS	0...+75	<21	<0,5	<310		TTL-TS

6605 — 4096x1-Bit dynamic RAM

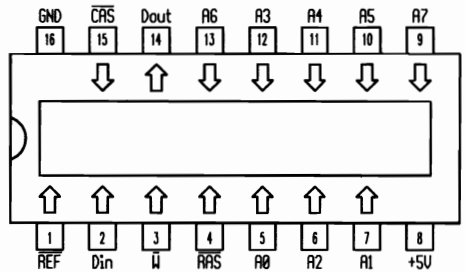


R/W	$\overline{CS}$	CE	D_{out}	Mode
H	L	H	data out	read only
H⌝⌞L	L	H	valid	read/write
L	L	H	valid	write only
H⌝⌞L	L⌟⌜H	H	valid→floating	read refresh
L	H	H	floating	refresh only
H	H	H	floating	not selected
X	X	L	floating	standby

6605 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6605A L	Mot	22-DIC	NMOS	0...+70	335	2,6	<300	<2	TTL-TS
MCM 6605A L1	Mot	22-DIC	NMOS	0...+70	335	2,6	<150	<2	TTL-TS
MCM 6605A L2	Mot	22-DIC	NMOS	0...+70	335	2,6	<200	<2	TTL-TS
MCM 6605A P	Mot	22-DIP	NMOS	0...+70	335	2,6	<300	<2	TTL-TS
MCM 6605A P1	Mot	22-DIP	NMOS	0...+70	335	2,6	<150	<2	TTL-TS
MCM 6605A P2	Mot	22-DIP	NMOS	0...+70	335	2,6	<200	<2	TTL-TS
MCM 6815A L	Mot	22-DIC	NMOS	0...+70	335	0,55	<300	<2	TTL-TS
MCM 6815A L2	Mot	22-DIC	NMOS	0...+70	335	0,55	<200	<2	TTL-TS

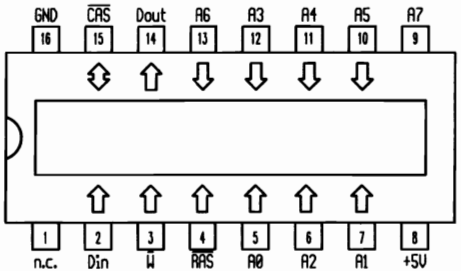
6605 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6815A P	Mot	22-DIP	NMOS	0...+70	335	0,55	<300	<2	TTL-TS
MCM 6815A P2	Mot	22-DIP	NMOS	0...+70	335	0,55	<200	<2	TTL-TS

6632 — 32768x1-Bit dynamic RAM

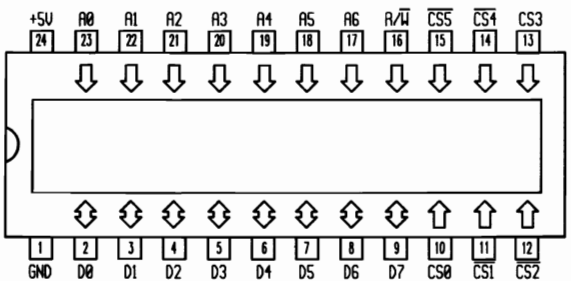


6632 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6632-15	Mot	16-DIC	NMOS	0...+70	<275	<30	<150	<2	TTL-TS
MCM 6632-20	Mot	16-DIC	NMOS	0...+70	<275	<30	<200	<2	TTL-TS
MCM 6632 A-12	Mot	16-DIC	NMOS	0...+70	<330	<22	<120	<2	TTL-TS
MCM 6632 A-15	Mot	16-DIC	NMOS	0...+70	<302	<22	<150	<2	TTL-TS
MCM 6632 A-20	Mot	16-DIC	NMOS	0...+70	<275	<22	<200	<2	TTL-TS

6633 — 32768x1-Bit dynamic RAM



6810 — 128x8-Bit static RAM

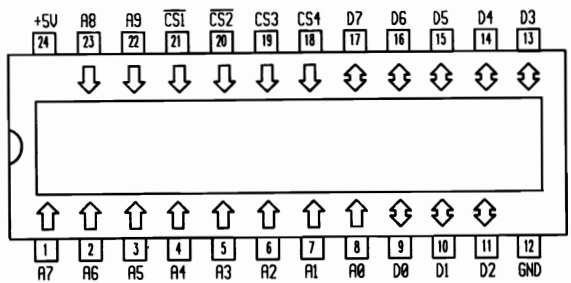


6633 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 6633-15	Mot	16-DIC	NMOS	0...+70	<275	<30	<150	<2	TTL-TS
MCM 6633-20	Mot	16-DIC	NMOS	0...+70	<275	<30	<200	<2	TTL-TS
MCM 6633 A-12	Mot	16-DIC	NMOS	0...+70	<330	<22	<120	<2	TTL-TS
MCM 6633 A-15	Mot	16-DIC	NMOS	0...+70	<302	<22	<150	<2	TTL-TS
MCM 6633 A-20	Mot	16-DIC	NMOS	0...+70	<275	<22	<200	<2	TTL-TS

6810 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 46810	Hit	24-DIC	NMOS	-20...+75	<367		<450		TTL-TS
HM 468A10	Hit	24-DIC	NMOS	-20...+75	<367		<360		TTL-TS
HM 468A10 P	Hit	24-DIP	NMOS	-20...+75	<367		<360		TTL-TS
HM 46810 P	Hit	24-DIP	NMOS	-20...+75	<367		<450		TTL-TS
MCM 6810 AL	Mot	24-DIC	NMOS	0...+70	<683		<500		TTL-TS
MCM 6810 BJCS	Mot	24-DIC	NMOS	-55...+125	<420		<450		TTL-TS
MCM 6810 CJCS	Mot	24-DIC	NMOS	-55...+125	<420		<450		TTL-TS
MCM 6810 CL	Mot	24-DIC	NMOS	-40...+85	<420		<450		TTL-TS

6810 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 68A10 CL	Mot	24-DIC	NMOS	-40...+85	<550		<360		TTL-TS
MCM 6810 CP	Mot	24-DIP	NMOS	-40...+85	<420		<450		TTL-TS
MCM 68A10 CP	Mot	24-DIP	NMOS	-40...+85	<550		<360		TTL-TS
MCM 6810 L	Mot	24-DIC	NMOS	0...+70	<420		<450		TTL-TS
MCM 68A10 L	Mot	24-DIC	NMOS	0...+70	<550		<360		TTL-TS
MCM 68B10 L	Mot	24-DIP	NMOS	0...+70	<550		<250		TTL-TS
MCM 6810 P	Mot	24-DIP	NMOS	0...+70	<420		<450		TTL-TS
MCM 68A10 P	Mot	24-DIP	NMOS	0...+70	<550		<360		TTL-TS
MCM 68B10 P	Mot	24-DIP	NMOS	0...+70	<550		<250		TTL-TS

7680 — 1024x8-Bit PROM



7680 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S180 A	Amd	24-DIP	TTL	0...+60	<971		<35		TTL-OC
Am 27S181 A	Amd	24-DIP	TTL	0...+60	<971		<35		TTL-TS
DM 77S180 J	Nsc	24-DIC	TTL	-55...+125	<935		<75		TTL-OC
DM 77S181 AJ	Nsc	24-DIC	TTL	-55...+125	<935		<65		TTL-TS
DM 77S181 J	Nsc	24-DIC	TTL	-55...+125	<935		<75		TTL-TS
DM 77S280 J	Nsc	24-TDIC	TTL	-55...+125	<935		<75		TTL-OC
DM 77S281 AJ	Nsc	24-TDIC	TTL	-55...+125	<935		<65		TTL-TS
DM 77S281 J	Nsc	24-TDIC	TTL	-55...+125	<935		<75		TTL-TS

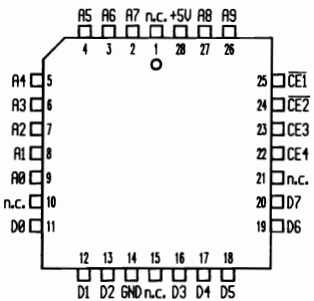
7680 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87S180 J	Nsc	24-DIC	TTL	0...+70	<935		<55		TTL-OC
DM 87S180 N	Nsc	24-DIP	TTL	0...+70	<935		<55		TTL-OC
DM 87LS181 AJ	Nsc	24-DIC	TTL	0...+70	<525		<100		TTL-TS
DM 87LS181 AN	Nsc	24-DIP	TTL	0...+70	<525		<100		TTL-TS
DM 87S181 AJ	Nsc	24-DIC	TTL	0...+70	<935		<45		TTL-TS
DM 87S181 AN	Nsc	24-DIP	TTL	0...+70	<935		<45		TTL-TS
DM 87S181 J	Nsc	24-DIC	TTL	0...+70	<935		<55		TTL-TS
DM 87S181 N	Nsc	24-DIP	TTL	0...+70	<935		<55		TTL-TS
DM 87S228 N	Nsc	24-DIP	TTL	0...+70	<892		<70		TTL-TS
DM 87S229 N	Nsc	24-DIP	TTL	0...+70	<892		<70		TTL-OC
DM 87S280 J	Nsc	24-TDIC	TTL	0...+70	<935		<55		TTL-OC
DM 87S280 N	Nsc	24-TDIP	TTL	0...+70	<935		<55		TTL-OC
DM 87S281 AJ	Nsc	24-TDIC	TTL	0...+70	<935		<45		TTL-TS
DM 87S281 AN	Nsc	24-TDIP	TTL	0...+70	<935		<45		TTL-TS
DM 87S281 J	Nsc	24-TDIC	TTL	0...+70	<935		<55		TTL-TS
DM 87S281 N	Nsc	24-TDIP	TTL	0...+70	<935		<55		TTL-TS
HN 25088	Hit	24-DIC	TTL	-25...+75	600		<60		TTL-OC
HN 25088 S	Hit	24-DIP	TTL	0...+75	<840		<50		TTL-OC
HN 25089	Hit	24-DIC	TTL	-25...+75	600		<60		TTL-TS
HN 25089 S	Hit	24-DIP	TTL	0...+75	<840		<50		TTL-TS
MCM 7680 DC	Mot	24-DIC	TTL	0...+70	<750		<70		TTL-OC
MCM 7680 DM	Mot	24-DIC	TTL	-55...+125	<750		<85		TTL-OC
MCM 7681 DC	Mot	24-DIC	TTL	0...+70	<750		<70		TTL-TS
MCM 7681 DM	Mot	24-DIC	TTL	-55...+125	<750		<85		TTL-TS
N 82S180 F	Sig	24-DIC	TTL	0...+75	<919		<70		TTL-OC
N 82S180 N	Sig	24-DIP	TTL	0...+75	<919		<70		TTL-OC
N 82LS181 N	Val	24-DIP	TTL	0...+75	<420		<120		TTL-TS
N 82S181A N	Val	24-DIP	TTL	0...+75	<919		<55		TTL-TS
N 82S181C N	Val	24-DIP	TTL	0...+75	<919		<30		TTL-TS
N 82S181C N3	Val	24-TDIP	TTL	0...+75	<919		<30		TTL-TS
N 82S181 F	Sig	24-DIC	TTL	0...+75	<919		<70		TTL-TS
N 82S181 N	Val	24-DIP	TTL	0...+75	<919		<70		TTL-TS
S 82S180 F	Sig	24-DIC	TTL	-55...+125	<1017		<90		TTL-OC
S 82S181 F	Sig	24-DIC	TTL	-55...+125	<1017		<90		TTL-TS
SN 74LS478 J	Tix	24-DIC	TTL	0...+70	<289		<130		TTL-TS
SN 74LS478 N	Tix	24-DIP	TTL	0...+70	<289		<130		TTL-TS
SN 74S478 J	Tix	24-DIC	TTL	0...+70	<919		<70		TTL-TS

7680 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74S478 N	Tix	24-DIP	TTL	0...+70	<919		<70		TTL-TS
SN 74S479 J	Tix	24-DIC	TTL	0...+70	<919		<70		TTL-OC
SN 74S479 N	Tix	24-DIP	TTL	0...+70	<919		<70		TTL-OC
TBP 28L85 J	Tix	24-TDIC	TTL	0...+70	<289		65		TTL-TS
TBP 28L85 MJ	Tix	24-TDIC	TTL	-55...+125	<302		65		TTL-TS
TBP 28L85 N	Tix	24-TDIP	TTL	0...+70	<289		65		TTL-TS
TBP 28P85 J	Tix	24-TDIC	TTL	0...+70	<577	<63	35		TTL-TS
TBP 28P85 MJ	Tix	24-TDIC	TTL	-55...+125	<605	<66	35		TTL-TS
TBP 28P85 N	Tix	24-TDIP	TTL	0...+70	<577	<63	35		TTL-TS
TBP 28S85 J	Tix	24-TDIC	TTL	0...+70	<577		35		TTL-TS
TBP 28S85 MJ	Tix	24-TDIC	TTL	-55...+125	<605		35		TTL-TS
TBP 28S85 N	Tix	24-TDIP	TTL	0...+70	<577		35		TTL-TS
TBP 28L86 J	Tix	24-DIC	TTL	0...+70	<289		<130		TTL-TS
TBP 28L86 MJ	Tix	24-DIC	TTL	-55...+125	<302		<175		TTL-TS
TBP 28L86 N	Tix	24-DIP	TTL	0...+70	<289		<130		TTL-TS
TBP 28SA86 J	Tix	24-DIC	TTL	0...+70	<919		<70		TTL-OC
TBP 28SA86 MJ	Tix	24-DIC	TTL	-55...+125	<962		<70		TTL-OC
TBP 28SA86 N	Tix	24-DIP	TTL	0...+70	<919		<70		TTL-OC
TBP 28S86 J	Tix	24-DIC	TTL	0...+70	<919		<70		TTL-TS
TBP 28S86 MJ	Tix	24-DIC	TTL	-55...+125	<962		<70		TTL-TS
TBP 28S86 N	Tix	24-DIP	TTL	0...+70	<919		<70		TTL-TS
TS 71180A CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<45		TTL-OC
TS 71180A CP	Tho	24-DIP	NMOS	0...+70	<962,5		<45		TTL-OC
TS 71180B CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<35		TTL-OC
TS 71180B CP	Tho	24-DIP	NMOS	0...+70	<962,5		<35		TTL-OC
TS 71180C CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<25		TTL-OC
TS 71180C CP	Tho	24-DIP	NMOS	0...+70	<962,5		<25		TTL-OC
TS 71181A CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<45		TTL-TS
TS 71181A CP	Tho	24-DIP	NMOS	0...+70	<962,5		<45		TTL-TS
TS 71181B CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71181B CP	Tho	24-DIP	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71181C CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<25		TTL-TS
TS 71181C CP	Tho	24-DIP	NMOS	0...+70	<962,5		<25		TTL-TS
TS 71280A CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<45		TTL-OC
TS 71280A CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<45		TTL-OC
TS 71280B CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<35		TTL-OC
TS 71280B CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<35		TTL-OC

7680 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TS 71280C CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<25		TTL-OC
TS 71280C CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<25		TTL-OC
TS 71281A CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<45		TTL-TS
TS 71281A CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<45		TTL-TS
TS 71281B CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71281B CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71281C CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<25		TTL-TS
TS 71281C CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<25		TTL-TS
3608	Int	24-DIP	TTL	0...+75	<997		<80		TTL-OC
3608-4	Int	24-DIP	TTL	0...+75	<997		<100		TTL-OC
3628	Int	24-DIP	TTL	0...+75	<997		<80		TTL-TS
3628-4	Int	24-DIP	TTL	0...+75	<997		<100		TTL-TS
3628 A	Int	24-DIC	TTL	0...+75	<930		<60		TTL-TS
3628 A-1	Int	24-DIC	TTL	0...+75	<930		<50		TTL-TS
3628 A-3	Int	24-DIP	TTL	0...+75	<935		<70		TTL-TS
3628 A-4	Int	24-DIP	TTL	0...+75	<935		<90		TTL-TS
6380-1	Mmi	24-DIC	TTL	0...+70	<945		<90		TTL-OC
6380-2	Mmi	24-DIP	TTL	0...+75	<892		<70		TTL-OC
6381-1	Mmi	24-DIC	TTL	0...+70	<945		<90		TTL-TS
6381-2	Mmi	24-DIP	TTL	0...+75	<892		<55		TTL-OC
63LS880	Mmi	24-DIP	TTL	0...+75	331		55		TTL-OC
63PS880	Mmi	24-DIP	TTL	0...+75	641	131	39		TTL-OC
63S880	Mmi	24-DIP	TTL	0...+75	614		34		TTL-OC
63LS881	Mmi	24-DIP	TTL	0...+75	331		55		TTL-TS
63PS881	Mmi	24-DIP	TTL	0...+75	641	157	39		TTL-TS
63S881	Mmi	24-DIP	TTL	0...+75	614		34		TTL-TS
93L450	Fch	24-DIP	TTL	0...+70	<325		<50		TTL-OC
93Z450 ADC	Fch	24-DIC	TTL	0...+75	<709		<35		TTL-OC
93Z450 ADM	Fch	24-DIC	TTL	-55...+125	<742		<45		TTL-OC
93Z450 AFC	Fch	24-FLAT	TTL	0...+75	<709		<35		TTL-OC
93Z450 AFC	Fch	24-FLAT	TTL	0...+75	<709		<35		TTL-OC
93Z450 AFM	Fch	24-FLAT	TTL	-55...+125	<742		<45		TTL-OC
93Z450 APC	Fch	24-DIP	TTL	0...+75	<709		<35		TTL-OC
93Z450 ASDC	Fch	24-TDIC	TTL	0...+75	<709		<35		TTL-OC
93Z450 ASDM	Fch	24-TDIC	TTL	-55...+125	<742		<45		TTL-OC
93Z450 DC	Fch	24-DIC	TTL	0...+75	<709		<40		TTL-OC
93Z450 DM	Fch	24-DIC	TTL	-55...+125	<742		<55		TTL-OC

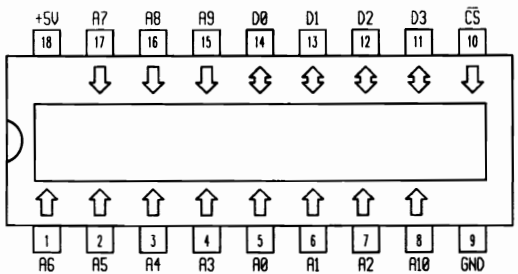
7680 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93Z450 FC	Fch	24-FLAT	TTL	0...+75	<709		<40		TTL-OC
93Z450 FM	Fch	24-FLAT	TTL	-55...+125	<742		<55		TTL-OC
93Z450 PC	Fch	24-DIP	TTL	0...+75	<709		<40		TTL-OC
93Z450 SDC	Fch	24-TDIC	TTL	0...+75	<709		<40		TTL-OC
93Z450 SDM	Fch	24-TDIC	TTL	-55...+125	<742		<55		TTL-OC
93L451	Fch	24-DIP	TTL	0...+70	<325		<50		TTL-TS
93Z451 ADC	Fch	24-DIC	TTL	0...+75	<709		<35		TTL-TS
93Z451 ADM	Fch	24-DIC	TTL	-55...+125	<742		<45		TTL-TS
93Z451 AFC	Fch	24-FLAT	TTL	0...+75	<709		<35		TTL-TS
93Z451 AFM	Fch	24-FLAT	TTL	-55...+125	<742		<45		TTL-TS
93Z451 APC	Fch	24-DIP	TTL	0...+75	<709		<35		TTL-TS
93Z451 ASDC	Fch	24-TDIC	TTL	0...+75	<709		<35		TTL-TS
93Z451 ASDM	Fch	24-TDIC	TTL	-55...+125	<742		<45		TTL-TS
93Z451 DC	Fch	24-DIC	TTL	0...+75	<709		<40		TTL-TS
93Z451 DM	Fch	24-DIC	TTL	-55...+125	<742		<55		TTL-TS
93Z451 FC	Fch	24-FLAT	TTL	0...+75	<709		<40		TTL-TS
93Z451 FM	Fch	24-FLAT	TTL	-55...+125	<742		<55		TTL-TS
93Z451 PC	Fch	24-DIP	TTL	0...+75	<709		<40		TTL-TS
93Z451 SDC	Fch	24-TDIC	TTL	0...+75	<709		<40		TTL-TS
93Z451 SDM	Fch	24-TDIC	TTL	-55...+125	<742		<55		TTL-TS
µPB 408 C	Nip	24-DIP	TTL	-25...+75	<880		<60		TTL-OC
µPB 408 C-1	Nip	24-DIP	TTL	-25...+75	<880		<50		TTL-OC
µPB 408 D	Nip	24-DIC	TTL	-25...+75	<880		<60		TTL-OC
µPB 408 D-1	Nip	24-DIC	TTL	-25...+75	<880		<50		TTL-OC
µPB 428 C	Nip	24-DIP	TTL	-25...+75	<880		<60		TTL-TS
µPB 428 C-1	Nip	24-DIP	TTL	-25...+75	<880		<50		TTL-TS
µPB 428 D	Nip	24-DIC	TTL	-25...+75	<880		<60		TTL-TS
µPB 428 D-1	Nip	24-DIC	TTL	-25...+75	<880		<50		TTL-TS

7680 — 1024x8-Bit PROM



7680 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87S180 V	Nsc	28-FLAT	TTL	0...+70	<935		<55		TTL-OC
DM 87S181 AV	Nsc	28-FLAT	TTL	0...+70	<935		<45		TTL-TS
DM 87S181 V	Nsc	28-FLAT	TTL	0...+70	<935		<55		TTL-TS
N 82S181 A	Val	28-PLCC	TTL	0...+75	<919		<70		TTL-TS
N 82S181A A	Val	28-PLCC	TTL	0...+75	<919		<55		TTL-TS
N 82S181C A	Val	28-PLCC	TTL	0...+75	<919		<30		TTL-TS
93Z450 ALC	Fch	28-LCC	TTL	0...+75	<709		<35		TTL-OC
93Z450 ALM	Fch	28-LCC	TTL	-55...+125	<742		<45		TTL-OC
93Z450 LC	Fch	28-LCC	TTL	0...+75	<709		<40		TTL-OC
93Z450 LM	Fch	28-LCC	TTL	-55...+125	<742		<55		TTL-OC
93Z451 ALC	Fch	28-LCC	TTL	0...+75	<709		<35		TTL-TS
93Z451 ALM	Fch	28-LCC	TTL	-55...+125	<742		<45		TTL-TS
93Z451 LC	Fch	28-LCC	TTL	0...+75	<709		<40		TTL-TS
93Z451 LM	Fch	28-LCC	TTL	-55...+125	<742		<55		TTL-TS

7684 — 2048x4-Bit PROM

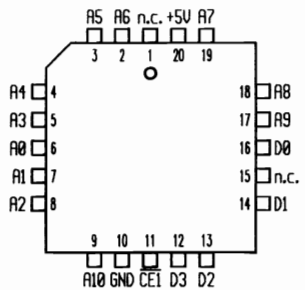


7684 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27LS184	Amd	18-DIP	TTL	0...+75	<656		<60		TTL-OC
Am 27S184	Amd	18-DIP	TTL	0...+75	<787		<50		TTL-OC
Am 27S184 A	Amd	18-DIP	TTL	0...+70	<787		<35		TTL-OC
Am 27LS185	Amd	18-DIP	TTL	0...+75	<656		<60		TTL-TS
Am 27S185	Amd	18-DIP	TTL	0...+75	<787		<50		TTL-TS
Am 27S185 A	Amd	18-DIP	TTL	0...+70	<787		<35		TTL-TS
DM 77S185 AJ	Nsc	18-DIC	TTL	-55...+125	<770		<60		TTL-TS
DM 77S185 BJ	Nsc	18-DIC	TTL	-55...+125	<770		<50		TTL-TS

7684 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77S184 J	Nsc	18-DIC	TTL	-55...+125	<770		<70		TTL-OC
DM 77S185 J	Nsc	18-DIC	TTL	-55...+125	<770		<70		TTL-TS
DM 87S184 J	Nsc	18-DIC	TTL	0...+70	<770		<55		TTL-OC
DM 87S184 N	Nsc	18-DIP	TTL	0...+70	<770		<55		TTL-OC
DM 87S185 AJ	Nsc	18-DIC	TTL	0...+70	<770		<45		TTL-TS
DM 87S185 AN	Nsc	18-DIP	TTL	0...+70	<770		<45		TTL-TS
DM 87S185 BJ	Nsc	18-DIC	TTL	0...+70	<770		<35		TTL-TS
DM 87S185 BN	Nsc	18-DIP	TTL	0...+70	<770		<35		TTL-TS
DM 87S185 J	Nsc	18-DIC	TTL	0...+70	<770		<55		TTL-TS
DM 87S185 N	Nsc	18-DIP	TTL	0...+70	<770		<55		TTL-TS
HN 25084	Hit	18-DIC	TTL	-20...+75	550		<60		TTL-OC
HN 25084 S	Hit	18-DIC	TTL	0...+75	<787		<50		TTL-OC
HN 25085	Hit	18-DIC	TTL	-20...+75	550		<60		TTL-TS
HN 25085 S	Hit	18-DIC	TTL	0...+75	<787		<50		TTL-TS
MCM 7684 DC	Mot	18-DIC	TTL	0...+70	<600		<70		TTL-OC
MCM 7684 DM	Mot	18-DIC	TTL	-55...+125	<700		<85		TTL-OC
MCM 7685 DC	Mot	18-DIC	TTL	0...+70	<600		<70		TTL-TS
MCM 7685 DM	Mot	18-DIC	TTL	-55...+125	<700		<85		TTL-TS
N 82S184 I	Sig	18-DIC	TTL	0...+75	<630		<100		TTL-OC
N 82S185C N	Val	18-DIP	TTL	0...+75	<814		<25		TTL-TS
N 82S185 I	Sig	18-DIC	TTL	0...+75	<630		<100		TTL-TS
N 82S185 N	Val	18-DIP	TTL	0...+75	<630		<100		TTL-TS
N 82S185A N	Val	18-DIP	TTL	0...+75	<814		<50		TTL-TS
N 82S185B N	Val	18-DIP	TTL	0...+75	<814		<45		TTL-TS
S 82S184 I	Sig	18-DIC	TTL	-55...+125	<715		<120		TTL-OC
S 82S185 I	Sig	18-DIC	TTL	-55...+125	<715		<120		TTL-TS
SN 74S454 J	Tix	18-DIC	TTL	0...+70	<919		<70		TTL-TS
SN 74S454 N	Tix	18-DIP	TTL	0...+70	<919		<70		TTL-TS
SN 74S455 J	Tix	18-DIC	TTL	0...+70	<919		<70		TTL-OC
SN 74S455 N	Tix	18-DIP	TTL	0...+70	<919		<70		TTL-OC
TBP 24SA81 J	Tix	18-DIC	TTL	0...+70	<919		<70		TTL-OC
TBP 24SA81 MJ	Tix	18-DIC	TTL	-55...+125	<962		<95		TTL-OC
TBP 24SA81 N	Tix	18-DIP	TTL	0...+70	<919		<70		TTL-OC
TBP 24S81 J	Tix	18-DIC	TTL	0...+70	<919		<70		TTL-TS
TBP 24S81 MJ	Tix	18-DIC	TTL	-55...+125	<962		<85		TTL-TS
TBP 24S81 N	Tix	18-DIP	TTL	0...+70	<919		<70		TTL-TS
µPB 427 C	Nec	18-DIP	TTL	-25...+75	<770		<55		TTL-TS

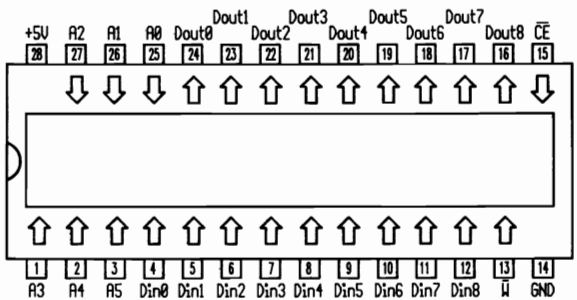
7684 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $ / mW/bit	t_{aa} ns	t_{ref} ms	Output
µPB 427 C-1	Nec	18-DIP	TTL	-25...+75	<770	<45		TTL-TS
µPB 427 D	Nec	18-DIC	TTL	-25...+75	<770	<55		TTL-TS
µPB 427 D-1	Nec	18-DIC	TTL	-25...+75	<770	<45		TTL-TS

7684 — 2048x4-Bit PROM



7684 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $ / mW/bit	t_{aa} ns	t_{ref} ms	Output
DM 87S184 V	Nsc	20-FLAT	TTL	0...+70	<770	<55		TTL-OC
DM 87S185 AV	Nsc	20-FLAT	TTL	0...+70	<770	<45		TTL-TS
DM 87S185 BV	Nsc	20-FLAT	TTL	0...+70	<770	<35		TTL-TS
DM 87S185 V	Nsc	20-FLAT	TTL	0...+70	<770	<55		TTL-TS

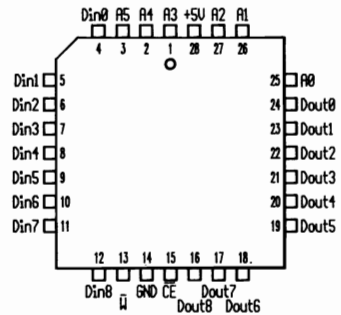
8209 — 64x9-Bit RAM (bipolar)



$\overline{CE}_1$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	Hi-Z	disabled

8209 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S09 I	Sig	28-DIC	TTL	0...+75	<997		<45		TTL-OC
N 82S09 N	Val	28-DIP	TTL	0...+75	<997		<45		TTL-OC
S 82S09 I	Sig	28-DIC	TTL	-55...+125	<1100		<80		TTL-OC
S 82S09 N	Sig	28-DIP	TTL	-55...+125	<1100		<80		TTL-OC
93419 DC	Fch	28-DIC	TTL	0...+75	725		<45		TTL-OC
93419 DM	Fch	28-DIC	TTL	-55...+125	725		<60		TTL-OC

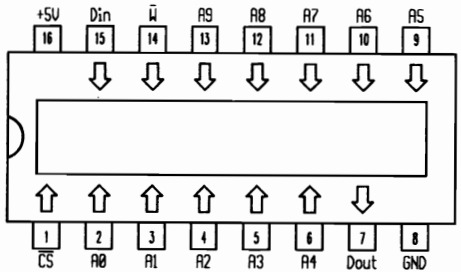
8209 — 64x9-Bit RAM (bipolar)



$\overline{CE}_1$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	Hi-Z	disabled

8209 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S09 A	Val	28-PLCC	TTL	0...+75	<997		<35		TTL-OC

8210 — 1024x1-Bit RAM (bipolar)



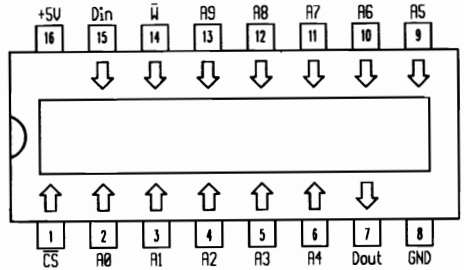
$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	H	not selected
L	L	L	H	write 0
L	L	H	H	write 1
L	H	X	data out	read

8210 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $ mW/bit	t_{aa} ns	t_{ref} ms	Output
HM 2510	Hit	16-DIC	TTL	0...+75	$0,5	<70		TTL-OC
HM 2510-1	Hit	16-DIC	TTL	0...+75	$0,5	<45		TTL-OC
HM 2510-2	Hit	16-DIC	TTL	0...+75	$0,5	<35		TTL-OC
IM 5508	Isi	16-DIC	TTL	0...+75	<630	<100		TTL-OC
MCM 93415 DC-35	Mot	16-DIC	TTL	0...+75	$0,5	35		TTL-OC
MCM 93415 DM-35	Mot	16-DIC	TTL	-55...+125	$0,5	35		TTL-OC
MCM 93415 FM-35	Mot	16-FLAT	TTL	-55...+125	$0,5	35		TTL-OC
MCM 93415 PC-35	Mot	16-DIP	TTL	0...+75	$0,5	35		TTL-OC

8210 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $ mW/bit	t_{aa} ns	t_{ref} ms	Output
N 82S10 F	Sig	16-DIC	TTL	0...+75	<814	<45		TTL-OC
N 82S10 N	Sig	16-DIP	TTL	0...+75	<814	<45		TTL-OC
N 82S110 F	Sig	16-DIC	TTL	0...+75	<814	<35		TTL-OC
N 82S110 N	Sig	16-DIP	TTL	0...+75	<814	<35		TTL-OC
N 93415A F	Sig	16-DIC	TTL	0...+75	<814	<45		TTL-OC
N 93415A N	Sig	16-DIP	TTL	0...+75	<814	<45		TTL-OC
S 82S10 F	Sig	16-DIC	TTL	-55...+125	<852	<70		TTL-OC
S 82S10 N	Sig	16-DIP	TTL	-55...+125	<852	<70		TTL-OC
SN 74S309 N	Tix	16-DIP	TTL	0...+70	<735	<100		TTL-OC
93415 AC	Mmi	16-DIP	TTL	0...+75	<814	<30		TTL-OC
93415A DC	Fch	16-DIC	TTL	0...+75	475	<30		TTL-OC
93415A FC	Fch	16-FLAT	TTL	0...+75	475	<30		TTL-OC
93415A PC	Fch	16-DIP	TTL	0...+75	475	<30		TTL-OC
93415 DC	Fch	16-DIC	TTL	0...+75	475	<45		TTL-OC
93415 DC-25	Fch	16-DIC	TTL	0...+75	<656	<25		TTL-OC
93415 DC-30	Fch	16-DIC	TTL	0...+75	<656	<30		TTL-OC
93415 DM	Fch	16-DIC	TTL	-55...+125	475	<60		TTL-OC
93415 DM-30	Fch	16-DIC	TTL	-55...+125	<742	<30		TTL-OC
93415 DM-40	Fch	16-DIC	TTL	-55...+125	<742	<40		TTL-OC
93415 FC	Fch	16-FLAT	TTL	0...+75	475	<45		TTL-OC
93415 FC-25	Fch	16-FLAT	TTL	0...+75	<656	<25		TTL-OC
93415 FC-30	Fch	16-FLAT	TTL	0...+75	<656	<30		TTL-OC
93415 FM	Fch	16-FLAT	TTL	-55...+125	475	<60		TTL-OC
93415 FM-30	Fch	16-FLAT	TTL	-55...+125	<742	<30		TTL-OC
93415 FM-40	Fch	16-FLAT	TTL	-55...+125	<742	<40		TTL-OC
93L415 C	Mmi	16-DIP	TTL	0...+75	<341	<60		TTL-OC
93L415 DC	Fch	16-DIC	TTL	0...+75	200	<60		TTL-OC
93L415 DC-35	Fch	16-DIC	TTL	0...+75	<341	<35		TTL-OC
93L415 DC-45	Fch	16-DIC	TTL	0...+75	<341	<45		TTL-OC
93L415 DM	Fch	16-DIC	TTL	-55...+125	200	<70		TTL-OC
93L415 DM-40	Fch	16-DIC	TTL	-55...+125	<412	<40		TTL-OC
93L415 DM-50	Fch	16-DIC	TTL	-55...+125	<412	<50		TTL-OC
93L415 FC	Fch	16-FLAT	TTL	0...+75	200	<60		TTL-OC
93L415 FC-35	Fch	16-FLAT	TTL	0...+75	<341	<35		TTL-OC
93L415 FC-45	Fch	16-FLAT	TTL	0...+75	<341	<45		TTL-OC
93L415 FM	Fch	16-FLAT	TTL	-55...+125	200	<70		TTL-OC
93L415 FM-40	Fch	16-FLAT	TTL	-55...+125	<412	<40		TTL-OC

8210 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93L415 FM-50	Fch	16-FLAT	TTL	-55...+125	<412		<50		TTL-OC
93L415 PC	Fch	16-DIP	TTL	0...+75	200		<60		TTL-OC
93L415 PC-35	Fch	16-DIP	TTL	0...+75	<341		<35		TTL-OC
93L415 PC-45	Fch	16-DIP	TTL	0...+75	<341		<45		TTL-OC
93415 PC	Fch	16-DIP	TTL	0...+75	475		<45		TTL-OC
93415 PC-25	Fch	16-DIP	TTL	0...+75	<656		<25		TTL-OC
93415 PC-30	Fch	16-DIP	TTL	0...+75	<656		<30		TTL-OC
µPB 2205 D	Nip	16-DIP	TTL	0...+75	<814		<50		TTL-OC

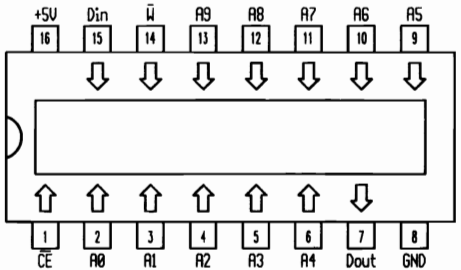
8211 — 1024x1-Bit RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{In}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

8211 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 2511	Hit	16-DIC	TTL	0...+75	$0,5		<70		TTL-TS
HM 2511-1	Hit	16-DIC	TTL	0...+75	$0,5		<45		TTL-TS

8211 — 1024x1-Bit RAM (bipolar)

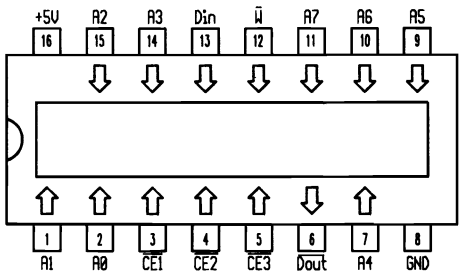


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

8211 Type	Man	Case	Techn.	TU°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
IM 5518	Isi	16-DIC	TTL	0...+75	<630		<100		TTL-TS
N 82S11 F	Sig	16-DIC	TTL	0...+75	<814		<45		TTL-TS
N 82S11 N	Sig	16-DIP	TTL	0...+75	<814		<45		TTL-TS
N 82S111 F	Sig	16-DIC	TTL	0...+75	<814		<35		TTL-TS
N 82S111 N	Sig	16-DIP	TTL	0...+75	<814		<35		TTL-TS
S 82S11 F	Sig	16-DIC	TTL	-55...+125	<852		<70		TTL-TS
S 82S11 N	Sig	16-DIP	TTL	-55...+125	<852		<70		TTL-TS
SN 74S209 N	Tix	16-DIP	TTL	0...+70	<735		<100		TTL-TS

8211 Type	Man	Case	Techn.	TU°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93425 AC	Mmi	16-DIP	TTL	0...+75	<814		<30		TTL-TS
93425A DC	Fch	16-DIC	TTL	0...+75	<814		<30		TTL-TS
93425A FC	Fch	16-FLAT	TTL	0...+75	<814		<30		TTL-TS
93425A PC	Fch	16-DIP	TTL	0...+75	<814		<30		TTL-TS
93425 DC	Fch	16-DIC	TTL	0...+75	<814		<45		TTL-TS
93425 DM	Fch	16-DIC	TTL	-55...+125	<935		<60		TTL-TS
93425 FC	Fch	16-FLAT	TTL	0...+75	<814		<45		TTL-TS
93425 FM	Fch	16-FLAT	TTL	-55...+125	<935		<60		TTL-TS
93L425 C	Mmi	16-DIP	TTL	0...+75	<341		<60		TTL-TS
93L425 DC	Fch	16-DIC	TTL	0...+75	<341		<60		TTL-TS
93L425 DM	Fch	16-DIC	TTL	-55...+125	<412		<70		TTL-TS
93L425 FC	Fch	16-FLAT	TTL	0...+75	<341		<60		TTL-TS
93L425 FM	Fch	16-FLAT	TTL	-55...+125	<412		<70		TTL-TS
93L425 PC	Fch	16-DIP	TTL	0...+75	<341		<60		TTL-TS
93425 PC	Fch	16-DIP	TTL	0...+75	<814		<45		TTL-TS

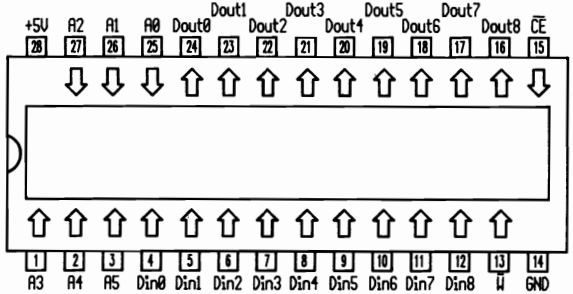
8216 — 256x1-Bit RAM (bipolar)



$\overline{CE}_{1...3}$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	Hi-Z	disabled

8216 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82LS16 D	Val	16-FLAT	TTL	0...+75	<368		<40		TTL-TS
N 82LS16 N	Val	16-DIP	TTL	0...+75	<368		<40		TTL-TS
N 82S16 D	Val	16-FLAT	TTL	0...+75	<604		<50		TTL-TS
N 82S16 F	Sig	16-DIC	TTL	0...+75	<604		<50		TTL-TS
N 82S16 N	Sig	16-DIP	TTL	0...+75	<604		<50		TTL-TS
N 82S17 F	Sig	16-DIC	TTL	0...+75	<604		<50		TTL-OC
N 82S17 N	Sig	16-DIP	TTL	0...+75	<604		<50		TTL-OC
N 82S116 F	Sig	16-DIC	TTL	0...+75	<604		<40		TTL-TS
N 82S116 N	Sig	16-DIP	TTL	0...+75	<604		<40		TTL-TS
N 82S117 F	Sig	16-DIC	TTL	0...+75	<604		<50		TTL-OC
N 82S117 N	Sig	16-DIP	TTL	0...+75	<604		<50		TTL-OC
S 82S16 F	Sig	16-DIC	TTL	-55...+125	<660		<70		TTL-TS
S 82S16 N	Sig	16-DIP	TTL	-55...+125	<660		<70		TTL-TS
S 82S17 F	Sig	16-DIC	TTL	-55...+125	<660		<70		TTL-OC
S 82S17 N	Sig	16-DIP	TTL	-55...+125	<660		<70		TTL-OC
93L420 DC	Fch	16-DIC	TTL	0...+75	275		<45		TTL-TS
93L420 DM	Fch	16-DIC	TTL	-55...+125	275		<55		TTL-TS
93L420 FC	Fch	16-FLAT	TTL	0...+75	275		<45		TTL-TS
93L420 FM	Fch	16-FLAT	TTL	-55...+125	275		<55		TTL-TS
93L420 PC	Fch	16-DIP	TTL	0...+75	275		<45		TTL-TS
93421A DC	Fch	16-DIC	TTL	0...+75	475		<40		TTL-TS
93421A PC	Fch	16-DIP	TTL	0...+75	475		<40		TTL-TS
93421 DC	Fch	16-DIC	TTL	0...+75	475		<50		TTL-TS
93L421 DM	Fch	16-DIC	TTL	-55...+125	275		<100		TTL-TS
93421 DM	Fch	16-DIC	TTL	-55...+125	475		<60		TTL-TS
93421A FC	Fch	16-FLAT	TTL	0...+75	475		<40		TTL-TS
93421 FC	Fch	16-FLAT	TTL	0...+75	475		<50		TTL-TS
93L421 FC	Fch	16-FLAT	TTL	0...+75	275		<90		TTL-TS
93L421 FM	Fch	16-FLAT	TTL	-55...+125	275		<100		TTL-TS
93421 FM	Fch	16-FLAT	TTL	-55...+125	475		<60		TTL-TS
93L421 DC	Fch	16-DIC	TTL	0...+75	275		<90		TTL-TS
93L421 PC	Fch	16-DIP	TTL	0...+75	275		<90		TTL-TS
93421 PC	Fch	16-DIP	TTL	0...+75	475		<50		TTL-TS

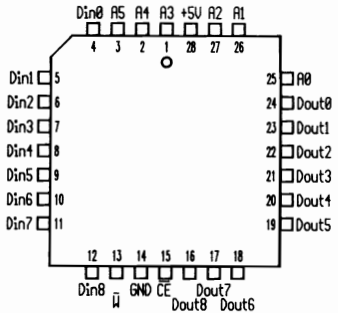
8219 — 64x9-Bit RAM (bipolar)



$\overline{CE}$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	H	disabled

8219 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S19 N	Val	28-DIP	TTL	0...+75	<997		<35		TTL-OC

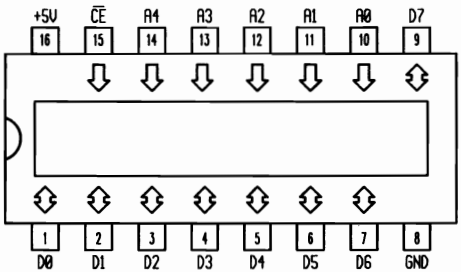
8219 — 64x9-Bit RAM (bipolar)



$\overline{CE}$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	H	disabled

8219 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S19 A	Val	28-PLCC	TTL	0...+75	<997		<35		TTL-OC

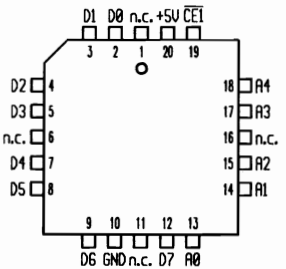
8223 — 32x8-Bit PROM



8223 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S08	Amd	16-DIC	TTL	0...+75	<525		<55		TTL-OC
Am 27S09	Amd	16-DIC	TTL	0...+75	<525		<55		TTL-TS
Am 27S18 A	Amd	16-DIP	TTL	0...+75	<604		<25		TTL-OC
Am 27S19 A	Amd	16-DIP	TTL	0...+75	<604		<25		TTL-TS
DM 8577	Nsc	16-DIP	TTL	0...+70	<577		<50		TTL-OC
DM 8578	Nsc	16-DIP	TTL	0...+70	<577		<50		TTL-TS
DM 54S188 AJ	Nsc	16-DIC	TTL	-55...+125	<605		<35		TTL-OC
DM 54S188 J	Nsc	16-DIC	TTL	-55...+125	<605		<45		TTL-OC
DM 54S288 AJ	Nsc	16-DIC	TTL	-55...+125	<605		<35		TTL-TS
DM 54S288 J	Nsc	16-DIC	TTL	-55...+125	<605		<45		TTL-TS
DM 74S188 AJ	Nsc	16-DIC	TTL	0...+70	<605		<25		TTL-OC
DM 74S188 AN	Nsc	16-DIP	TTL	0...+70	<605		<25		TTL-OC
DM 74S188 J	Nsc	16-DIC	TTL	0...+70	<605		<35		TTL-OC
DM 74S188 N	Nsc	16-DIP	TTL	0...+70	<605		<35		TTL-OC
DM 74S288	Nsc	16-DIP	TTL	0...+70	<577		<30		TTL-TS
DM 74S288 AJ	Nsc	16-DIC	TTL	0...+70	<605		<25		TTL-TS
DM 74S288 AN	Nsc	16-DIP	TTL	0...+70	<605		<25		TTL-TS
DM 74S288 J	Nsc	16-DIP	TTL	0...+70	<605		<35		TTL-TS
DM 87S188 J	Nsc	16-DIC	TTL	0...+70	630		<15		TTL-OC
DM 87S188 N	Nsc	16-DIP	TTL	0...+70	630		<15		TTL-OC
DM 87S288 J	Nsc	16-DIC	TTL	0...+70	630		<15		TTL-TS
DM 87S288 N	Nsc	16-DIP	TTL	0...+70	630		<15		TTL-TS
IM 5600	Isi	16-DIP	TTL	0...+75	<525		<50		TTL-OC
IM 5610	Isi	16-DIP	TTL	0...+75	<525		<50		TTL-TS
M 54730 K	Mit	16-DIC	TTL	0...+75	<656		<50		TTL-OC
M 54730 P	Mit	16-DIP	TTL	0...+75	<656		<50		TTL-OC
M 54730 S	Mit	16-DIC	TTL	0...+75	<656		<50		TTL-OC
MB 7051	Fui	16-DIC	TTL	0...+75	<525		<75		TTL-TS
MB 7051	Fui	16-DIC	TTL	0...+75	<525		<75		TTL-OC
MSL 8515	Oki	16-DIC	TTL	0...+70	<420		<80		TTL-OC
MSL 8516	Oki	16-DIC	TTL	0...+70	<525		<80		TTL-TS
N 82S23 D	Val	16-FLAT	TTL	0...+75	<504		<50		TTL-OC
N 82S23A D	Val	16-FLAT	TTL	0...+75	<504		<25		TTL-OC
N 82S23 F	Sig	16-DIC	TTL	0...+75	<404		<50		TTL-OC
N 82S23 N	Val	16-DIP	TTL	0...+75	<504		<50		TTL-OC
N 82S23A N	Val	16-DIP	TTL	0...+75	<504		<25		TTL-OC
N 82US23 N	Val	16-DIP	TTL	0...+75	<604		<13		TTL-OC
N 82S123 D	Val	16-FLAT	TTL	0...+75	<504		<50		TTL-TS
N 82S123A D	Val	16-FLAT	TTL	0...+75	<504		<25		TTL-TS
N 82S123 F	Sig	16-DIC	TTL	0...+75	<404		<50		TTL-TS
N 82S123 N	Val	16-DIP	TTL	0...+75	<504		<50		TTL-TS
N 82S123A N	Val	16-DIP	TTL	0...+75	<504		<25		TTL-TS
N 82US123 N	Val	16-DIP	TTL	0...+75	<604		<10		TTL-TS
S 82S23 F	Sig	16-DIC	TTL	-55...+125	<468		<65		TTL-OC
S 82S23 N	Sig	16-DIP	TTL	-55...+125	<468		<65		TTL-OC

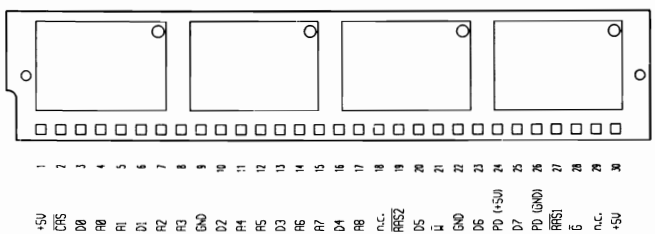
8223 — 32x8-Bit PROM

8223 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $/bit	t_{aa} ns	t_{ref} ms	Output
S 82S123 F	Sig	16-DIC	TTL	-55...+125	<468	<65		TTL-TS
S 82S123 N	Sig	16-DIP	TTL	-55...+125	<468	<65		TTL-TS
SN 74S188 J	Tix	16-DIC	TTL	0...+70	<577	<40		TTL-OC
SN 74S188 N	Tix	16-DIP	TTL	0...+70	<577	<40		TTL-OC
SN 74S288 J	Tix	16-DIC	TTL	0...+70	<577	<40		TTL-TS
SN 74S288 N	Tix	16-DIP	TTL	0...+70	<577	<40		TTL-TS
TBP 18SA030 J	Tix	16-DIC	TTL	0...+70	<577	<40		TTL-OC
TBP 18SA030 MJ	Tix	16-DIC	TTL	-55...+125	<577	<50		TTL-TS
TBP 18SA030 N	Tix	16-DIP	TTL	0...+70	<577	<40		TTL-OC
TBP 18S030 J	Tix	16-DIC	TTL	0...+70	<577	<40		TTL-TS
TBP 18S030 MJ	Tix	16-DIC	TTL	-55...+125	<577	<50		TTL-OC
TBP 18S030 N	Tix	16-DIP	TTL	0...+70	<577	<40		TTL-TS
6330-1	Mmi	16-DIC	TTL	0...+70	<656	<50		TTL-OC
6331-1	Mmi	16-DIC	TTL	0...+70	<656	<50		TTL-TS
63LS080	Mmi	16-DIC	TTL	0...+75	184	24		TTL-OC
63S080	Mmi	16-DIC	TTL	0...+75	341	13		TTL-OC
63LS081	Mmi	16-DIC	TTL	0...+75	184	24		TTL-TS
63S081	Mmi	16-DIC	TTL	0...+75	341	13		TTL-TS
µPB 400 C	Nec	16-DIC	TTL	-25...+75	<550	<35		TTL-OC
µPB 400 C-1	Nec	16-DIC	TTL	-25...+75	<550	<30		TTL-OC
µPB 400 D	Nec	16-DIP	TTL	-25...+75	<550	<35		TTL-OC
µPB 400 D-1	Nec	16-DIP	TTL	-25...+75	<550	<30		TTL-OC
µPB 410 C	Nec	16-DIC	TTL	-25...+75	<550	<35		TTL-TS
µPB 410 C-1	Nec	16-DIC	TTL	-25...+75	<550	<30		TTL-TS
µPB 410 D	Nec	16-DIP	TTL	-25...+75	<550	<35		TTL-TS
µPB 410 D-1	Nec	16-DIP	TTL	-25...+75	<550	<30		TTL-TS



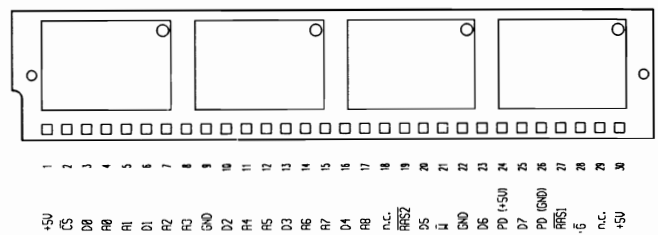
8223 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $/bit	t_{aa} ns	t_{ref} ms	Output
DM 74S188 V	Nsc	20-FLAT	TTL	0...+70	<605	<35		TTL-OC
DM 74S288 V	Nsc	20-FLAT	TTL	0...+70	<605	<35		TTL-TS
N 82S23 A	Val	20-PLCC	TTL	0...+75	<504	<50		TTL-OC
N 82S23A A	Val	20-PLCC	TTL	0...+75	<504	<25		TTL-OC
N 82US23 A	Val	20-PLCC	TTL	0...+75	<604	<13		TTL-OC
N 82S123 A	Val	20-PLCC	TTL	0...+75	<504	<50		TTL-TS
N 82S123A A	Val	20-PLCC	TTL	0...+75	<504	<25		TTL-TS
N 82US123 A	Val	20-PLCC	TTL	0...+75	<604	<10		TTL-TS

8512 — 524288x8-Bit dyn. RAM-Modul (page mode)



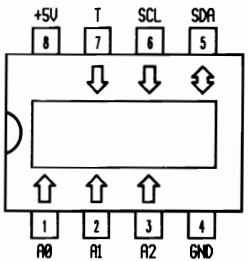
8512 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 8512 L-10	Tos	30-SIP	CMOS	0...+70	<737	<22	<100	<8	TTL-TS
THM 8512 L-12	Tos	30-SIP	CMOS	0...+70	<627	<22	<120	<8	TTL-TS
THM 8512 S-10	Tos	30-SIC	CMOS	0...+70	<737	<22	<100	<8	TTL-TS
THM 8512 S-12	Tos	30-SIC	CMOS	0...+70	<627	<22	<120	<8	TTL-TS

8514 — 524288x8-Bit dyn. RAM-Modul (static col)



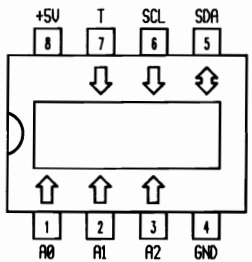
8514 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 8514 L-10	Tos	30-SIP	CMOS	0...+70	<737	<22	<100	<8	TTL-TS
THM 8514 L-12	Tos	30-SIP	CMOS	0...+70	<627	<22	<120	<8	TTL-TS
THM 8514 S-10	Tos	30-SIC	CMOS	0...+70	<737	<22	<100	<8	TTL-TS
THM 8514 S-12	Tos	30-SIC	CMOS	0...+70	<627	<22	<120	<8	TTL-TS

8570 — 256x8-Bit static RAM for I²C-BUS



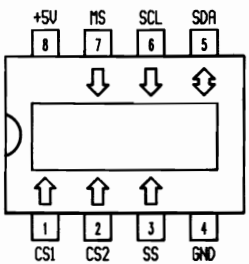
8570 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCF 8570 CP	Phi	8-DIP	CMOS	-40...+85	<50				I²C-BUS
PCF 8570 CT	Phi	8-FLAT	CMOS	-40...+85	<50				I²C-BUS
PCF 8570 P	Phi	8-DIP	CMOS	-40...+70	<50	<75µ			I²C-BUS
PCF 8570 T	Phi	8-FLAT	CMOS	-40...+70	<50	<75µ			I²C-BUS

8571 — 128x8-Bit static RAM for I²C-BUS

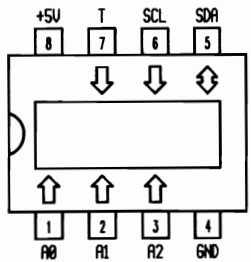


8571 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCD 8571 D	Phi	8-DIC	CMOS	-25...+70	<50	<25µ			I²C-BUS
PCD 8571 P	Phi	8-DIP	CMOS	-25...+70	<50	<25µ			I²C-BUS
PCD 8571 T	Phi	8-FLAT	CMOS	-25...+70	<50	<25µ			I²C-BUS
PCF 8571 CP	Phi	8-DIP	CMOS	-40...+85	<50				I²C-BUS
PCF 8571 CT	Phi	8-FLAT	CMOS	-40...+85	<50				I²C-BUS

8571 — 128x8-Bit serial EEPROM for 1²C-BUS



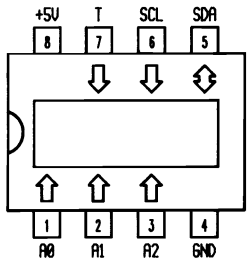
8581 — 128x8-Bit EEPROM for 1²C-BUS



8571 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 8571 B1	Sgs	8-DIP	NMOS	0...+70	<105	<42	<3,5µ		I²C-BUS
M 8571 B6	Sgs	8-DIP	NMOS	-40...+85	<110				I²C-BUS
M 8571 F1	Sgs	8-DIC	NMOS	0...+70	<105	<42			I²C-BUS

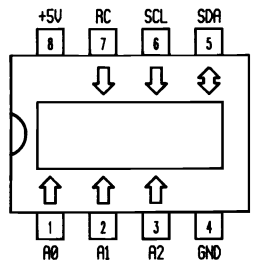
8581 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCF 8581 CP	Phi	8-DIP	CMOS	-40...+85	<50				I²C-BUS
PCF 8581 CT	Phi	8-FLAT	CMOS	-40...+85	<50				I²C-BUS
PCF 8581 P	Phi	8-DIP	CMOS	-40...+85	<50				I²C-BUS
PCF 8581 T	Phi	8-FLAT	CMOS	-40...+85	<50				I²C-BUS

8582 — 256x8-Bit EEPROM for 1²C-BUS



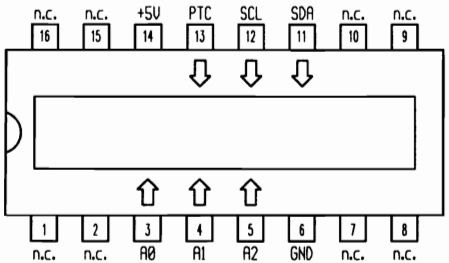
8582 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCF 8582 CP	Phi	8-DIP	CMOS	-40...+85	<15	<60µ			I²C-BUS

8582 — 256x8-Bit EEPROM for 1²C-BUS



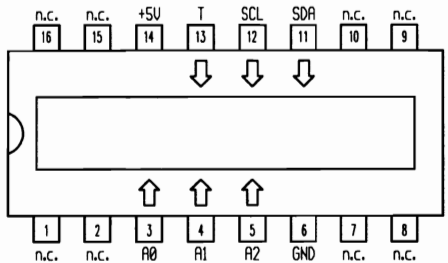
8582 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCF 8582 AP	Phi	8-DIP	CMOS	-40...+85	<11	<55µ			I²C-BUS
PCF 8582 BP	Phi	8-DIP	CMOS	-40...+125	<11	<110µ			I²C-BUS
PCF 8582 P	Val	8-DIP	CMOS	-40...+85	<11	<55µ			I²C-BUS

8582 — 256x8-Bit EEPROM for 1²C-BUS



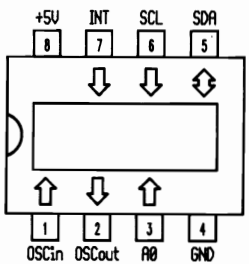
8582 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCF 8582 AT	Phi	16-FLAT	CMOS	-40…+85	<11	<55µ			I²C-BUS
PCF 8582 BT	Phi	16-FLAT	CMOS	-40…+125	<11	<110µ			I²C-BUS

8582 — 256x8-Bit EEPROM for 1²C-BUS



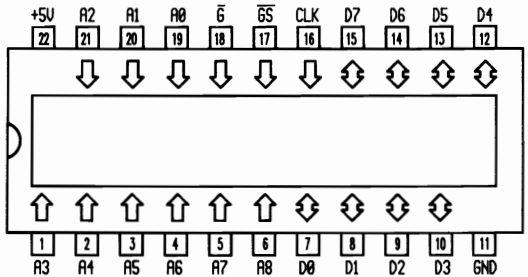
8582 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCF 8582 CT	Phi	16-FLAT	CMOS	-40…+85	<15	<60µ			I²C-BUS

8583 — 256x8-Bit static RAM for I²C-BUS



8583 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PCF 8583 P	Val	8-DIP	CMOS	0...+70	<300				I²C-BUS
PCF 8583 T	Val	8-FLAT	CMOS	0...+70	<300				I²C-BUS

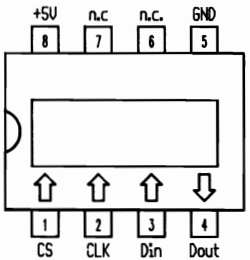
8727 — 512x8-Bit Register PROM



8727 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77SR27 BJ	Nsc	22-TDIC	TTL	-55...+125	<1017		<40		TTL-TS
DM 77SR27 J	Nsc	22-TDIC	TTL	-55...+125	<1017		<55		TTL-TS
DM 87SR27 BJ	Nsc	22-TDIC	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR27 BN	Nsc	22-TDIP	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR27 J	Nsc	22-TDIC	TTL	0...+70	<1017		<50		TTL-TS
DM 87SR27 N	Nsc	22-TDIP	TTL	0...+70	<1017		<50		TTL-TS

9306

256x1-Bit serial EEPROM

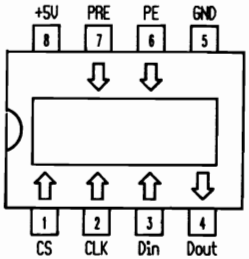


Start-Bit*	Operation-Code	Address	Data	Mode
1	10XX	A3A2A1A0		read register A3A2A1A0
1	01XX	A3A2A1A0	$D_{15}...D_0$	write register A3A2A1A0
1	11XX	A3A2A1A0		erase register A3A2A1A0
1	0011	XXXX		erase/write enable
1	0000	XXXX		erase/write disable
1	0010	XXXX		erase all registers
1	0001	XXXX	$D_{15}...D_0$	write all registers

* Eine »1« als MSB ist das Startbit für die Interface-Sequence. Die nächsten 8 Bit beinhalten den Operations-Code und die 4-Bit-Adresse für eines von sechzehn 16-Bit-Registern.
* A "1" as MSB is the starting bit for the interface sequence. The next 8 bits contain the operations code and the 4-bit address for one of sixteen 16-bit registers.
* Un «1» en tant que MSB représente le bit initial pour la séquence d'interface. Les 8 bits suivants comportent le code opération et l'adresse à 4 bits pour un registre de 16 bits parmi 16 registres.
* Un «1» come MSB è il bit di avviamento per la sequenza d'interfaccia. I seguenti 8 bit contengono il codice di operazione e l'indirizzo 4-bit per uno dei 16 registri 16-bit.
* Un «1» en el MSB es el bit de partida para la secuencia de interfase. Los siguientes 8 bits contienen el código de operación y la dirección de 4 bits de uno de los 16 registros de 16 bits.

9306 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{sa} ns	t_{ref} ms	Output
					$mW/bit				
M 9306 B1	Sgs	8-DIP	NMOS	0...+70	<27,5	<16,5			TTL-TS
M 9306 B6	Sgs	8-DIP	NMOS	-40...+85	<27,5	<16,5			TTL-TS
M 9306 F1	Sgs	8-DIC	NMOS	0...+70	<27,5	<16,5			TTL-TS
M 9306 F6	Sgs	8-DIC	NMOS	-40...+85	<27,5	<16,5			TTL-TS
M 9306 M1	Sgs	8-FLAT	NMOS	0...+70	<27,5	<16,5			TTL-TS
M 9306 M6	Sgs	8-FLAT	NMOS	-40...+85	<27,5	<16,5			TTL-TS
NMC 9306 EN	Nsc	8-DIP	NMOS	-40...+85	<66	<22			TTL-TS
NMC 9306 MN	Nsc	8-DIP	NMOS	-55...+125	<77	<27,5			TTL-TS
NMC 9306 N	Nsc	8-DIP	NMOS	0...+70	<55	<16,5			TTL-TS

9306 — 256x1-Bit serial EEPROM



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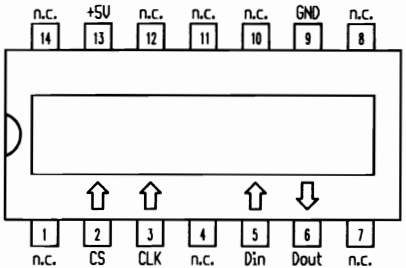
Function table see page 2-236
Tableau logique voir page 2-236
Per tavola di logica vedi pagina 2-236
Tabla de verdad, ver página 2-236

9306 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS06 EN	Nsc	8-DIP	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS06 MN	Nsc	8-DIP	CMOS	-55...+125	<22	<0,55			TTL-TS
NMC 93CS06 N	Nsc	8-DIP	CMOS	0...+70	<11	<0,275			TTL-TS

Start-Bit	OP-Code	Address	Data	PRE	PE	Mode
1	10	A5...A0		0	X	Daten lesen, Start bei einer beliebigen Adresse. Reads data stored in memory, starting at specified address. Lecture données, démarrage à une adresse quelconque. Lettura dati, avviamento ad un qualsiasi indirizzo. Lectura de datos de memoria empezando por la dirección indicada.
1	00	11XXXX	$D_{15}...D_0$	0	1	Schreiben möglich, nötig vor jeder Programmierung. Write enable must precede all programming modes. Ecriture possible, nécessaire avant chaque programmation. Possibilità di scrittura, necessario prima di ogni programmazione. El desbloqueo de escritura debe preceder a todos los modos de programación.
1	01	A5...A0	$D_{15}...D_0$	0	1	Schreibt in ein Register, sofern die Adresse nicht geschützt ist. Writes register if address is unprotected. Ecriture dans un registre, si l'adresse n'est pas protégée. Scrive in un registro qualora l'indirizzo non sia protetto. Escribir en un registro si la dirección no está protegida.
1	00	01XXXX		0	1	Schreibt in alle Register. Nur möglich, wenn alle »geschützten Register« gelöscht sind. Write all registers. Valid only when "protected register" is cleared. Ecrit dans tous les registres. Seulement possible, lorsque tous «les registres protégés» ont été effacés. Scrive in tutti i registri. Possibile solo se tutti i «registri protetti» sono cancellati. Escribir en todos los registros. Sólo es válida si se borró el «registro protegido».
1	00	00XXXX		0	X	Macht alle Programmierungen unmöglich. Disables all programming instructions. Rend toutes les programmations impossibles. Rende impossibile tutte le programmazioni. Bloquear todas las instrucciones de programación.
1	10	XXXXXX		1	X	Liest die Adressen der »geschützten Register«. Reads address stored in "protected register". Lit les adresses des «registres protégés». Legge gli indirizzi dei «registri protetti». Leer la dirección almacenada en el «registro protegido».
1	00	11XXXX		1	1	Nötig vor jedem PRCLEAR, PRWRITE und PRDS. Must immediately precede PRCLEAR, PRWRITE and PRDS instructions. Nécessaire avant chaque instruction PRCLEAR. PRWRITE et PRDS. Necessario prima di ogni PRCLEAR, PRWRITE e PRDS. Debe preceder directamente a las instrucciones PRCLEAR, PRWRITE y PRDS.
1	11	111111		1	1	Löscht alle »geschützten Register«, so daß jedes Register beschrieben werden kann (PRCLEAR). Clears the "protect register" so that no register are protected from WRITE (PRCLEAR). Efface tous les «registres protégés», de manière à ce qu'une écriture soit possible dans chaque registre. Cancella tutti i «Registri protetti» di modo che ogni registro può venir provvisto di scrittura (PRCLEAR). Borrar el «registro protegido», con lo que puede escribirse en todos los registros (PRCLEAR).
1	01	A5...A0		1	1	Programmiert die Adresse als »geschütztes Register«. Danach ist jede Adresse die ⩾ als diese Adresse ist, schreibgeschützt (PRWRITE). Programs address into "protect register". Thereafter, memory addresses ⩾ the addresses in "protect register" are protected from WRITE (PRWRITE). Programme l'adresse sous forme d'un «registre protégé». Par la suite, chaque adresse qui est ⩾ à cette adresse, est protégée contre l'écriture (PRWRITE). Programma di indirizzi come «registro protetto». Successivamente ogni indirizzo che sia ⩾ a questo indirizzo è protetto di scrittura (PRWRITE). Prog. la dirección indicada como «reg. prot.». Tras esta instrucción todas las direcciones de memoria ⩾ que la dirección en el «reg. prot.» quedan protegidas contra escritura (PRWRITE)
1	00	000000		1	1	Danach wird die Adresse in ein »geschütztes Register« übernommen. Nur einmal möglich! Kann danach nicht mehr geändert werden (PRDS). One time only instruction after which the address in the "protect register" cannot be altered (PRDS). Par la suite, l'adresse est prise en charge dans un «registre protégé». Cette opération n'est possible qu'une seule fois! Une modification ultérieure n'est plus possible (PRDS). Successivamente l'indirizzo viene accolto in un «registro protetto». Possibile solo una volta! Successivamente non può più venir cambiato (PRDS). Instrucción que puede ejecutarse una sola vez, y tras la cual no puede modificarse más la dirección contenida en el «registro protegido» (PRDS).

9306 — 256x1-Bit serial EEPROM



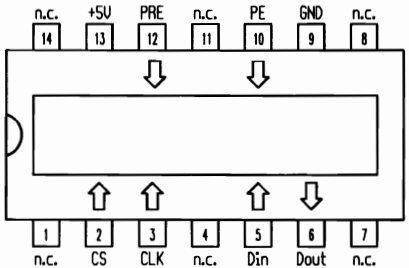
Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

Start-Bit*	Operation-Code	Address	Data	Mode
1	10XX	A3A2A1A0		read register A3A2A1A0
1	01XX	A3A2A1A0	$D_{15}...D_0$	write register A3A2A1A0
1	11XX	A3A2A1A0		erase register A3A2A1A0
1	0011	XXXX		erase/write enable
1	0000	XXXX		erase/write disable
1	0010	XXXX		erase all registers
1	0001	XXXX	$D_{15}...D_0$	write all registers

* Eine »1« als MSB ist das Startbit für die Interface-Sequence. Die nächsten 8 Bit beinhalten den Operations-Code und die 4-Bit-Adresse für eines von sechzehn 16-Bit-Registern.
* A "1" as MSB is the starting bit for the interface sequence. The next 8 bits contain the operations code and the 4-bit address for one of sixteen 16-bit registers.
* Un «1» en tant que MSB représente le bit initial pour la séquence d'interface. Les 8 bits suivants comportent le code opération et l'adresse à 4 bits pour un registre de 16 bits parmi 16 registres.
* Un «1» come MSB è il bit di avviamento per la sequenza d'interfaccia. I seguenti 8 bit contengono il codice di operazione e l'indirizzo 4-bit per uno dei 16 registri 16-bit.
* Un «1» en el MSB es el bit de partida para la secuencia de interfase. Los siguientes 8 bits contienen el código de operación y la dirección de 4 bits de uno de los 16 registros de 16 bits.

9306 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 9306 EM	Nsc	14-FLAT	NMOS	-40...+85	<66	<22			TTL-TS
NMC 9306 M	Nsc	14-FLAT	NMOS	0...+70	<55	<16,5			TTL-TS

9306 — 256x1-Bit serial EEPROM



Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

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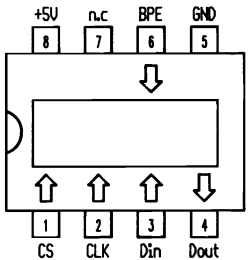
9306 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS06 EM	Nsc	14-FLAT	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS06 M	Nsc	14-FLAT	CMOS	0...+70	<11	<0,275			TTL-TS
NMC 93CS06 MM	Nsc	14-FLAT	CMOS	-55...+125	<22	<0,55			TTL-TS

9307 — 256x1-Bit serial EEPROM



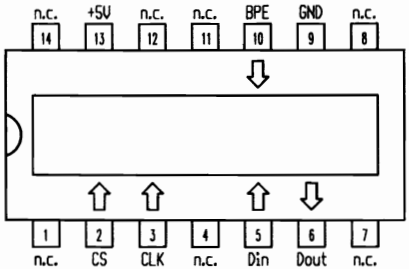
Start-Bit*	Operation-Code	Address	Data	BPE	Mode
1	10XX	A3A2A1A0		X	read register A3A2A1A0
1	01XX	A3A2A1A0	$D_{15}...D_0$	X	write register A3A2A1A0
1	11XX	A3A2A1A0		X	erase register A3A2A1A0
1	0011	XXXX		X	erase/write enable
1	0000	XXXX		X	erase/write disable
1	0010	XXXX		V_{iH}/open	erase all registers
1	0001	XXXX	$D_{15}...D_0$	V_{iH}/open	write all registers

* Eine »1« als MSB ist das Startbit für die Interface-Sequence. Die nächsten 8 Bit beinhalten den Operations-Code und die 4-Bit-Adresse für eines von sechzehn 16-Bit-Registern.
* A "1" as MSB is the starting bit for the interface sequence. The next 8 bits contain the operations code and the 4-bit address for one of sixteen 16-bit registers.
* Un «1» en tant que MSB représente le bit initial pour la séquence d'interface. Les 8 bits suivants comportent le code opération et l'adresse à 4 bits pour un registre de 16 bits parmi 16 registres.
* Un «1» come MSB è il bit di avviamento per la sequenza d'interfaccia. I seguenti 8 bit contengono il codice di operazione e l'indirizzo 4-bit per uno dei 16 registri 16-bit.
* Un «1» en el MSB es el bit de partida para la secuencia de interfase. Los siguientes 8 bits contienen el código de operación y la dirección de 4 bits de uno de los 16 registros de 16 bits.

9307 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 9307 EN	Nsc	8-DIP	NMOS	-40...+85	<66	<22			TTL-TS
NMC 9307 N	Nsc	8-DIP	NMOS	0...+70	<55	<16,5			TTL-TS

9307

256x1-Bit serial EEPROM



Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

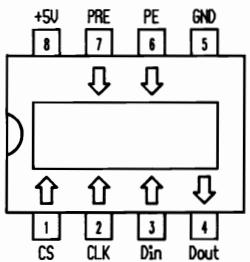
Start-Bit*	Operation-Code	Address	Data	BPE	Mode
1	10XX	A3A2A1A0		X	read register A3A2A1A0
1	01XX	A3A2A1A0	$D_{15}...D_0$	X	write register A3A2A1A0
1	11XX	A3A2A1A0		X	erase register A3A2A1A0
1	0011	XXXX		X	erase/write enable
1	0000	XXXX		X	erase/write disable
1	0010	XXXX		V_{IH}/open	erase all registers
1	0001	XXXX	$D_{15}...D_0$	V_{IH}/open	write all registers

Eine »1« als MSB ist das Startbit für die Interface-Sequence. Die nächsten 8 Bit beinhalten den Operations-Code und die 4-Bit-Adresse für eines von sechzehn 16-Bit-Registern.

* A "1" as MSB is the starting bit for the interface sequence. The next 8 bits contain the operations code and the 4-bit address for one of sixteen 16-bit registers.
* Un «1» en tant que MSB représente le bit initial pour la séquence d'interface. Les 8 bits suivants comportent le code opération et l'adresse à 4 bits pour un registre de 16 bits parmi 16 registres.
* Un «1» come MSB è il bit di avviamento per la sequenza d'interfaccia. I seguenti 8 bit contengono il codice di operazione e l'indirizzo 4-bit per uno dei 16 registri 16-bit.
* Un «1» en el MSB es el bit de partida para la secuencia de interfase. Los siguientes 8 bits contienen el código de operación y la dirección de 4 bits de uno de los 16 registros de 16 bits.

9307 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 9307 EM	Nsc	14-FLAT	NMOS	-40...+85	<66	<22			TTL-TS
NMC 9307 M	Nsc	14-FLAT	NMOS	0...+70	<55	<16,5			TTL-TS

9326 — 512x1-Bit serial EEPROM



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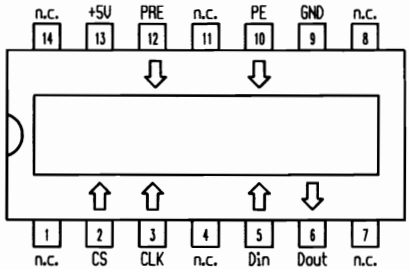
9326 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS26 EN	Nsc	8-DIP	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS26 MN	Nsc	8-DIP	CMOS	-55...+125	<22	<0,55			TTL-TS
NMC 93CS26 N	Nsc	8-DIP	CMOS	0...+70	<11	<0,275			TTL-TS

9326 — 512x1-Bit serial EEPROM



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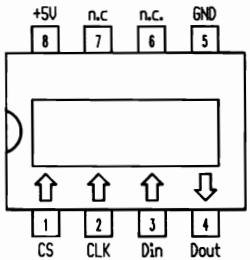
Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

9326 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS26 EM	Nsc	14-FLAT	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS26 M	Nsc	14-FLAT	CMOS	0...+70	<11	<0,275			TTL-TS
NMC 93CS26 MM	Nsc	14-FLAT	CMOS	-55...+125	<22	<0,55			TTL-TS

9346

1024x1-Bit serial EEPROM

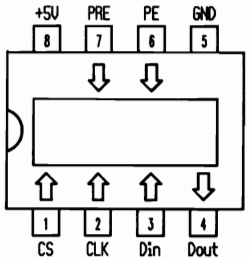


Start-Bit*	Operation-Code	Address	Data	Mode
1	10	A5A4A3A2A1A0		read register A5A4A3A2A1A0
1	01	A5A4A3A2A1A0	$D_{15}...D_0$	write register A5A4A3A2A1A0
1	11	A5A4A3A2A1A0		erase register A5A4A3A2A1A0
1	00	11XXXX		erase/write enable
1	00	00XXXX		erase/write disable
1	00	10XXXX		erase all registers
1	00	01XXXX	$D_{15}...D_0$	write all registers

* Eine »1« als MSB ist das Startbit für die Interface-Sequence. Die nächsten 8 Bit beinhalten den Operations-Code und die 6-Bit-Adresse für eines von 64 16-Bit-Registern.
* A "1" as MSB is the starting bit for the interface sequence. The next 8 bits contain the operations code and the 6-bit address for one of 64 16-bit registers.
* Un «1» en tant que MSB représente le bit initial pour la séquence d'interface. Les 8 bits suivants comportent le code opération et l'adresse à 6 bits pour un registre de 16 bits parmi 64 registres.
* Un «1» come MSB è il bit di avviamento per la sequenza d'interfaccia. I seguenti 8 bit contengono il codice di operazione e l'indirizzo di 6 bit per uno dei 64 registri 16-bit.
* Un «1» en el MSB es el bit de partida para la secuencia de interfase. Los siguientes 8 bits contienen el código de operación y la dirección de 6 bits de uno de los 64 registros de 16 bits.

9346 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 9346 B1	Sgs	8-DIP	NMOS	0...+70	<66	<16,5			TTL-TS
M 9346 B6	Sgs	8-DIP	NMOS	-40...+85	<66	<16,5			TTL-TS
M 9346 F1	Sgs	8-DIC	NMOS	0...+70	<66	<16,5			TTL-TS
M 9346 F6	Sgs	8-DIC	NMOS	-40...+85	<66	<16,5			TTL-TS
M 9346 M1	Sgs	8-FLAT	NMOS	0...+70	<66	<16,5			TTL-TS
M 9346 M6	Sgs	8-FLAT	NMOS	-40...+85	<66	<16,5			TTL-TS
NMC 9346 EN	Nsc	8-DIP	NMOS	-40...+85	<77	<22			TTL-TS
NMC 9346 MN	Nsc	8-DIP	NMOS	-55...+125	<82,5	<27,5			TTL-TS
NMC 9346 N	Nsc	8-DIP	NMOS	0...+70	<66	<16,5			TTL-TS
XLE 93C46 C	Exl	8-DIC	CMOS	-40...+85	<16,5	<5,5			TTL-TS
XLE 93C46 J	Exl	8-TDIC	CMOS	-40...+85	<16,5	<5,5			TTL-TS
XLE 93C46 P	Exl	8-DIP	CMOS	-40...+85	<16,5	<5,5			TTL-TS
XLS 93C46 C	Exl	8-DIC	CMOS	0...+70	<16,5	<5,5			TTL-TS
XLS 93C46 J	Exl	8-TDIC	CMOS	0...+70	<16,5	<5,5			TTL-TS
XLS 93C46 P	Exl	8-DIP	CMOS	0...+70	<16,5	<5,5			TTL-TS

9346 — 1024x1-Bit serial EEPROM



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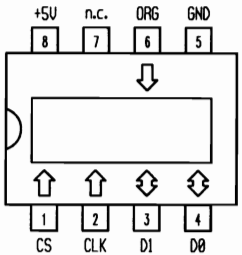
9346 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS46 EN	Nsc	8-DIP	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS46 MN	Nsc	8-DIP	CMOS	-55...+125	<22	<0,55			TTL-TS
NMC 93CS46 N	Nsc	8-DIP	CMOS	0...+70	<11	<0,275			TTL-TS

9346 — 1024x1-Bit serial EEPROM

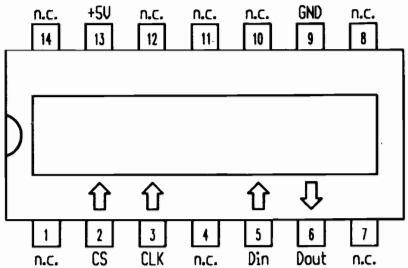


Start-Bit	Operation-Code	Address 128x8	Address 64x16	Data 128x8	Data 64x16	Mode
1	10	A6...A0	A5...A0			read address
1	11	A6...A0	A5...A0			erase address
1	01	A6...A0	A5...A0	$D_7...D_0$	$D_{15}...D_0$	write address*
1	00	11xxxxx	11xxxx			program enable (EWEN)
1	00	00xxxxx	00xxxx			program disable (EWDS)
1	00	10xxxxx	10xxxx			erase all addresses (ERAL)
1	00	01xxxxx	01xxxx	$D_7...D_0$	$D_{15}...D_0$	program all addresses (WRAL)

* Write instruction is a self timed program instruction. The selected byte (word) gets erased before being written.

9346 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TS 93C46 CP	Sgs	8-DIP	CMOS	0...+70	<22	<0,55			
TS 93C46 VP	Sgs	8-DIP	CMOS	-40...+85	<22	<0,55			

9346 — 1024x1-Bit serial EEPROM



Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

Start-Bit*	Operation-Code	Address	Data	Mode
1	10	A5A4A3A2A1A0		read register A5A4A3A2A1A0
1	01	A5A4A3A2A1A0	$D_{15}...D_0$	write register A5A4A3A2A1A0
1	11	A5A4A3A2A1A0		erase register A5A4A3A2A1A0
1	00	11XXXX		erase/write enable
1	00	00XXXX		erase/write disable
1	00	10XXXX		erase all registers
1	00	01XXXX	$D_{15}...D_0$	write all registers

* Eine »1« als MSB ist das Startbit für die Interface-Sequence. Die nächsten 8 Bit beinhalten den Operations-Code und die 6-Bit-Adresse für eines von 64 16-Bit-Registern.
* A "1" as MSB is the starting bit for the interface sequence. The next 8 bits contain the operations code and the 6-bit address for one of 64 16-bit registers.
* Un «1» en tant que MSB représente le bit initial pour la séquence d'interface. Les 8 bits suivants comportent le code opération et l'adresse à 6 bits pour un registre de 16 bits parmi 64 registres.
* Un «1» come MSB è il bit di avviamento per la sequenza d'interfaccia. I seguenti 8 bit contengono il codice di operazione e l'indirizzo di 6 bit per uno dei 64 registri 16-bit.
* Un «1» en el MSB es el bit de partida para la secuencia de interfase. Los siguientes 8 bits contienen el código de operación y la dirección de 6 bits de uno de los 64 registros de 16 bits.

9346 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 9346 M1	Sgs	14-FLAT	NMOS	0...+70	<42				TTL-TS
M 9346 M6	Sgs	14-FLAT	NMOS	-40...+85	<42				TTL-TS
NMC 9346 EM	Nsc	14-FLAT	NMOS	-40...+85	<77	<22			TTL-TS
NMC 9346 M	Nsc	14-FLAT	NMOS	0...+70	<66	<16,5			TTL-TS

9346 — 1024x1-Bit serial EEPROM

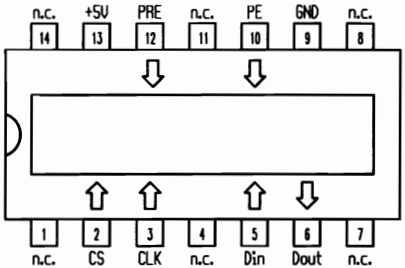


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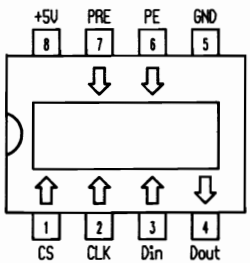
Tabla de verdad, ver página 2-236

Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

9356 — 2048x1-Bit serial EEPROM



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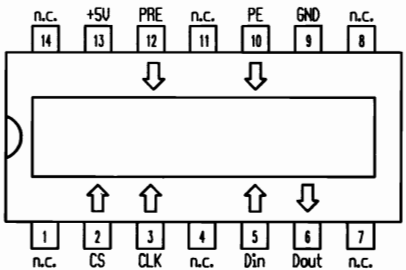
9346 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS46 EM	Nsc	14-FLAT	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS46 M	Nsc	14-FLAT	CMOS	0...+70	<11	<0,275			TTL-TS
NMC 93CS46 MM	Nsc	14-FLAT	CMOS	-55...+125	<22	<0,55			TTL-TS

9356 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS56 EN	Nsc	8-DIP	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS56 MN	Nsc	8-DIP	CMOS	-55...+125	<22	<0,55			TTL-TS
NMC 93CS56 N	Nsc	8-DIP	CMOS	0...+70	<11	<0,275			TTL-TS
ST 93C56 CP	Sgs	8-DIP	CMOS	0...+70	<16,5	<0,55			

Start-Bit	OP-Code	Address	Data	PRE	PE	Mode
1	10	A7...A0		0	X	Daten lesen, Start bei einer beliebigen Adresse. Reads data stored in memory, starting at specified address. Lecture données, démarrage à une adresse quelconque. Lettura dati, avviamento ad un qualsiasi indirizzo. Lectura de datos de memoria empezando por la dirección indicada.
1	00	11XXXXXX	$D_{15}...D_0$	0	1	Schreiben möglich, nötig vor jeder Programmierung. Write enable must precede all programming modes. Ecriture possible, nécessaire avant chaque programmation. Possibilità di scrittura, necessario prima di ogni programmazione. El desbloqueo de escritura debe preceder a todos los modos de programación.
1	01	A7...A0	$D_{15}...D_0$	0	1	Schreibt in ein Register, sofern die Adresse nicht geschützt ist. Writes register if address is unprotected. Ecriture dans un registre, si l'adresse n'est pas protégée. Scrive in un registro qualora l'indirizzo non sia protetto. Escribir en un registro si la dirección no está protegida.
1	00	01XXXXXX		0	1	Schreibt in alle Register. Nur möglich, wenn alle »geschützten Register« gelöscht sind. Write all registers. Valid only when "protected register" is cleared. Ecrit dans tous les registres. Seulement possible, lorsque tous «les registres protégés» ont été effacés. Scrive in tutti i registri. Possibile solo se tutti i «registri protetti» sono cancellati. Escribir en todos los registros. Sólo es válida si se borró el «registro protegido».
1	00	00XXXXXX		0	X	Macht alle Programmierungen unmöglich. Disables all programming instructions. Rend toutes les programmations impossibles. Rende impossibile tutte le programmazioni. Bloquear todas las instrucciones de programación.
1	10	XXXXXXXX		1	X	Liest die Adressen der »geschützten Register«. Reads address stored in "protected register". Lit les adresses des «registres protégés». Legge gli indirizzi dei «registri protetti». Leer la dirección almacenada en el «registro protegido».
1	00	11XXXXXX		1	1	Nötig vor jedem PRCLEAR, PRWRITE und PRDS. Must immediately precede PRCLEAR, PRWRITE and PRDS instructions. Nécessaire avant chaque instruction PRCLEAR, PRWRITE et PRDS. Necessario prima di ogni PRCLEAR, PRWRITE e PRDS. Debe preceder directamente a las instrucciones PRCLEAR, PRWRITE y PRDS.
1	11	11111111		1	1	Löscht alle »geschützten Register«, so daß jedes Register beschrieben werden kann (PRCLEAR). Clears the "protect register" so that no register are protected from WRITE (PRCLEAR). Efface tous les «registres protégés», de manière à ce qu'une écriture soit possible dans chaque registre. Cancella tutti i «Registri protetti» di modo che ogni registro può venir provvisto di scrittura (PRCLEAR). Borrar el «registro protegido», con lo que puede escribirse en todos los registros (PRCLEAR).
1	01	A7...A0		1	1	Programmiert die Adresse als »geschütztes Register«. Danach ist jede Adresse die ⩾ als diese Adresse ist, schreibgeschützt (PRWRITE). Programs address into "protect register". Thereafter, memory addresses ⩾ the addresses in "protect register" are protected from WRITE (PRWRITE). Programme l'adresse sous forme d'un «registre protégé». Par la suite, chaque adresse qui est ⩾ à cette adresse, est protégée contre l'écriture (PRWRITE). Programma di indirizzi come «registro protetto». Successivamente ogni indirizzo che sia ⩾ a questo indirizzo è protetto di scrittura (PRWRITE). Prog. la dirección indicada como «reg. prot.». Tras esta instrucción todas las direcciones de memoria ⩾ que la dirección en el «reg. prot.» quedan protegidas contra escritura (PRWRITE)
1	00	00000000		1	1	Danach wird die Adresse in ein »geschütztes Register« übernommen. Nur einmal möglich! Kann danach nicht mehr geändert werden (PRDS). One time only instruction after which the address in the "protect register" cannot be altered (PRDS). Par la suite, l'adresse est prise en charge dans un «registre protégé». Cette opération n'est possible qu'une seule fois! Une modification ultérieure n'est plus possible (PRDS). Successivamente l'indirizzo viene accolto in un «registro protetto». Possibile solo una volta! Successivamente non può più venir cambiato (PRDS). Instrucción que puede ejecutarse una sola vez, y tras la cual no puede modificarse más la dirección contenida en el «registro protegido» (PRDS).

9356 — 2048x1-Bit serial EEPROM



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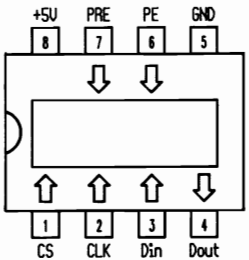
Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

9356 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS56 EM	Nsc	14-FLAT	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS56 M	Nsc	14-FLAT	CMOS	0...+70	<11	<0,275			TTL-TS
NMC 93CS56 MM	Nsc	14-FLAT	CMOS	-55...+125	<22	<0,55			TTL-TS
ST 93C56 CM	Sgs	14-FLAT	CMOS	0...+70	<16,5	<0,55			TTL-TS

9366 — 4096x1-Bit serial EEPROM



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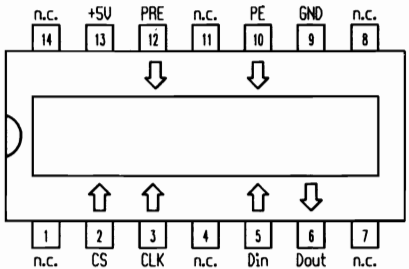
9366 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS66 EN	Nsc	8-DIP	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS66 MN	Nsc	8-DIP	CMOS	-55...+125	<22	<0,55			TTL-TS
NMC 93CS66 N	Nsc	8-DIP	CMOS	0...+70	<11	<0,275			TTL-TS

9366 — 4096x1-Bit serial EEPROM



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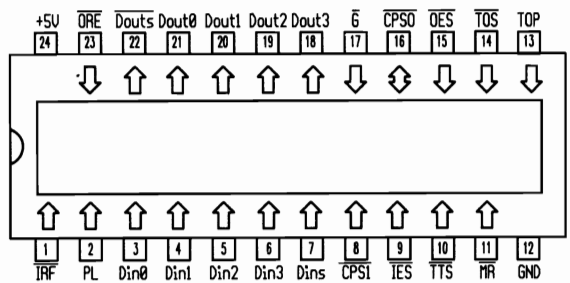
Pinabstand 1,27mm
Pin spacing 1.27mm
Espacement des broches: 1,27mm
Distanza pin 1,27mm
Distancia entre pins 1,27mm

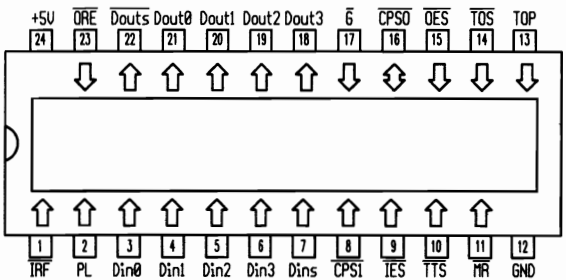
9403 — 16 words x 4-Bit FIFO



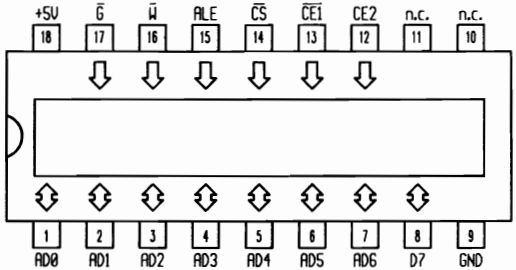
9366 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 93CS66 EM	Nsc	14-FLAT	CMOS	-40...+85	<22	<0,55			TTL-TS
NMC 93CS66 M	Nsc	14-FLAT	CMOS	0...+70	<11	<0,275			TTL-TS
NMC 93CS66 MM	Nsc	14-FLAT	CMOS	-55...+125	<22	<0,55			TTL-TS

9403 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
9403 DC	Fch	24-DIC	TTL	0...+70	<775				TTL-TS
9403 DM	Fch	24-DIC	TTL	-55...+125	<850				TTL-TS

9423 — 64 words x 4-Bit FIFO



9810 — 128x8-Bit EEPROM

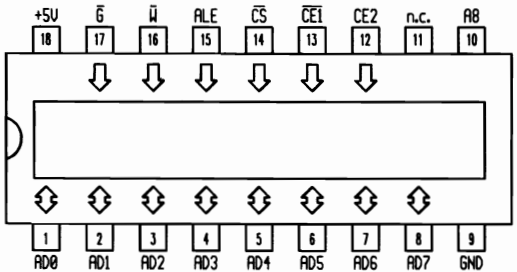


CE1	CE2	CS	G	W	$AD_0 \ldots AD_7$	Mode
H	X	X	X	X	Hi-Z	standby
X	L	X	X	X	Hi-Z	standby
L	H	H	X	X	Hi-Z	standby/power on
L	H	L	L	H	data out	read
L	H	L	H	L	data in	write
L	H	L	H	H	Hi-Z	inhibit
L	H	L	L	L	Hi-Z	inhibit

9423 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
9423 DC	Fch	24-DIC	TTL	0...+75	750				TTL-TS
9423 DM	Fch	24-DIC	TTL	-55...+125	750				TTL-TS
9423 FC	Fch	24-FLAT	TTL	0...+75	750				TTL-TS
9423 PC	Fch	24-DIP	TTL	0...+75	750				TTL-TS

9810 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 98C10 N	Nsc	18-DIP	CMOS	0...+70	<55	<0,55	<170		TTL-TS
NMC 98C10 N-1	Nsc	18-DIP	CMOS	0...+70	<55	<0,55	<120		TTL-TS

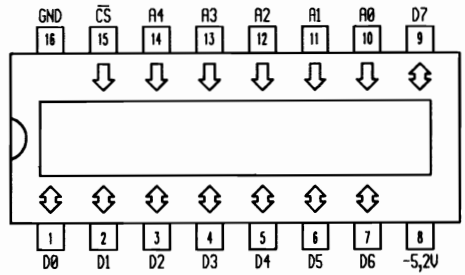
9840 — 512x8-Bit EEPROM



CE1	CE2	CS	G	W	$AD_0...AD_7$	Mode
H	X	X	X	X	Hi-Z	standby
X	L	X	X	X	Hi-Z	standby
L	H	H	X	X	Hi-Z	standby/power on
L	H	L	L	H	data out	read
L	H	L	H	L	data in	write
L	H	L	H	H	Hi-Z	inhibit
L	H	L	L	L	Hi-Z	inhibit

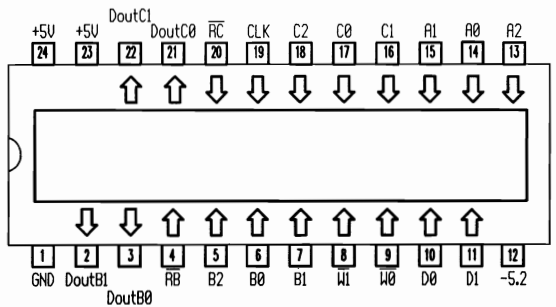
9840 Type	Man	Case	Techn.	Tu°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 98C40 N	Nsc	18-DIP	CMOS	0...+70	<55	<0,55	<170		TTL-TS
NMC 98C40 N-1	Nsc	18-DIP	CMOS	0...+70	<55	<0,55	<120		TTL-TS

10139 — 32x8-Bit PROM



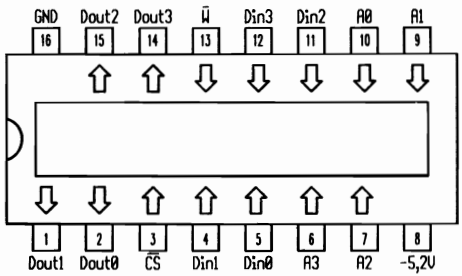
10139 Type	Man	Case	Techn.	Tu°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 10139 F	Mot	16-FLAT	ECL	0...+75	<750		<15		ECL
MCM 10139 L	Mot	16-DIC	ECL	0...+75	<750		<15		ECL
MCM 10539 F	Mot	16-FLAT	ECL	-55...+125	<750				ECL
MCM 10539 L	Mot	16-DIC	ECL	-55...+125	<750				ECL
N 10139 F	Sig	16-DIC	ECL	-30...+85	<754		<15		ECL
N 10139 N	Sig	16-DIP	ECL	-30...+85	<754		<15		ECL

10143 — 8x2-Bit Multiport Register RAM



Clock	$\overline{W0}$	$\overline{W1}$	Din0	Din1	$\overline{REB}$	$\overline{REC}$	QB0	QB1	QC0	QC1	Mode
L→H	L	L	H	H	H	H	L	L	L	L	write
H	X	X	X	X	L	L	H	H	H	H	read
H→L	X	X	X	X	L	L	H	H	H	H	read
L→H→L	H	H	X	X	L	L	H	H	H	H	read
L→H	L	L	L	H	H	H	L	L	L	L	write
H	X	X	X	X	L	L	L	H	L	H	read

10145 — 16x4-Bit Register RAM



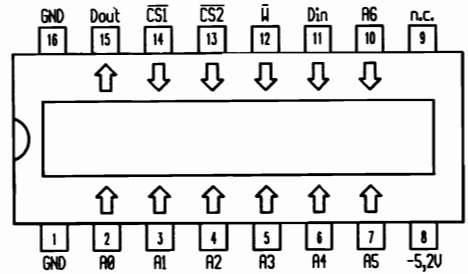
$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

10143 Type	Man	Case	Techn.	T°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 10143 F	Mot	24-FLAT	ECL	0...+75	<780		<10		ECL
MCM 10143 L	Mot	24-DIC	ECL	0...+75	<780		<10		ECL

10145 Type	Man	Case	Techn.	T°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 10145A DC	Fch	16-DIC	ECL	0...+75	<780		<9		ECL
F 10145A FC	Fch	16-FLAT	ECL	0...+75	<780		<9		ECL
F 10145A PC	Fch	16-DIP	ECL	0...+75	<780		<9		ECL
F 100402 DC	Fch	16-DIC	ECL	0...+85	<884		<6		ECL
F 100402 FC	Fch	16-FLAT	ECL	0...+85	<884		<6		ECL
MC 10H145 L	Mot	16-DIC	ECL	0...+75	<858		<3,5		ECL
MC 10H145 P	Mot	16-DIP	ECL	0...+75	<858		<3,5		ECL
MCM 10145 F	Mot	16-FLAT	ECL	0...+75	<650		<8		ECL

10145 Typ · Type · Tipo	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 10145 L	Mot	16-DIC	ECL	0...+75	<650		<8		ECL
MCM 10545 F	Mot	16-FLAT	ECL	-55...+125	<650		<10		ECL
MCM 10545 L	Mot	16-DIC	ECL	-55...+125	<650		<10		ECL

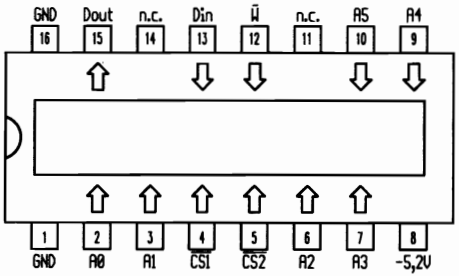
10147 — 128x1-Bit RAM (bipolar)



$\overline{CS1...3}$	$\overline{W}$	D_{in}	D_{out}	Mode
one H	X	X	L	not selected
all L	L	L	L	write 0
all L	L	H	L	write 1
all L	H	X	data out	read

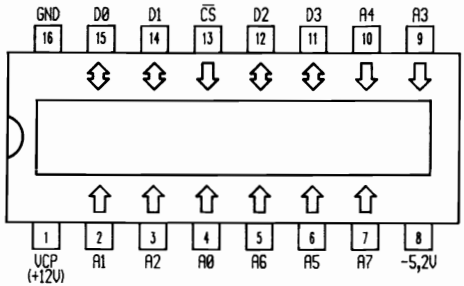
10147 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 10405 DC	Fch	16-DIC	ECL	0...+75	<780		<15		ECL
F 10405 FC	Fch	16-FLAT	ECL	0...+75	470		<15		ECL
MCM 10147 F	Mot	16-FLAT	ECL	0...+75	<520		<8		ECL
MCM 10147 L	Mot	16-DIC	ECL	0...+75	<520		<8		ECL
MCM 10547 F	Mot	16-FLAT	ECL	-55...+125	<520				ECL
MCM 10547 L	Mot	16-DIC	ECL	-55...+125	<520				ECL

10148 — 64x1-Bit RAM (bipolar)



CS1...3	W	D_{in}	D_{out}	Mode
one H	X	X	L	not selected
all L	L	L	L	write 0
all L	L	H	L	write 1
all L	H	X	data out	read

10149 — 256x4-Bit PROM

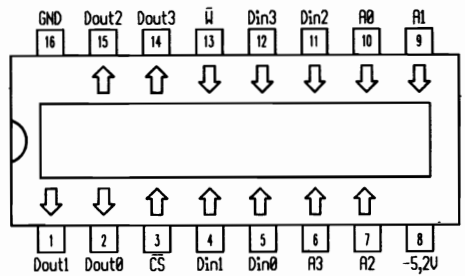


10148 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 10148 F	Mot	16-FLAT	ECL	0...+75	<520		<7,5		ECL
MCM 10148 L	Mot	16-DIC	ECL	0...+75	<520		<7,5		ECL
MCM 10548 F	Mot	16-FLAT	ECL	-55...+125	<520				ECL
MCM 10548 L	Mot	16-DIC	ECL	-55...+125	<520				ECL
µPB 10142 D	Nip	16-DIC	ECL	0...+65	<624		<25		ECL
µPB 10148 D	Nip	16-DIC	ECL	0...+65	<624		<25		ECL

10149 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 10416 DC	Fch	16-DIC	ECL	-30...+85	<780		<20		ECL
MCM 10149 F	Mot	16-FLAT	ECL	0...+75	<670		<10		ECL
MCM 10149 F-10	Mot	16-FLAT	ECL	0...+75	<910		<10		ECL
MCM 10149 F-25	Mot	16-FLAT	ECL	0...+75	<780		<25		ECL
MCM 10149 L	Mot	16-DIC	ECL	0...+75	<670		<10		ECL
MCM 10149 L-10	Mot	16-DIC	ECL	0...+75	<910		<10		ECL
MCM 10149 L-25	Mot	16-DIC	ECL	0...+75	<780		<25		ECL
MCM 10549 F	Mot	16-FLAT	ECL	-55...+125	<670				ECL

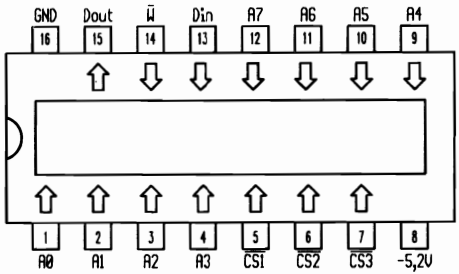
10149 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 10549 L	Mot	16-DIC	ECL	-55...+125	<670				ECL
10149A F	Val	16-DIC	ECL	-30...+85	<832		<10		ECL
10149 F	Val	16-DIC	ECL	-30...+85	<832		<20		ECL

10402 — 16x4-Bit Register RAM



10402 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 10402 DC	Fch	16-DIC	ECL	0...+85	<884		<6		ECL
F 10402 FC	Fch	16-FLAT	ECL	0...+85	<884		<6		ECL

10414 — 256x1-Bit RAM (bipolar)

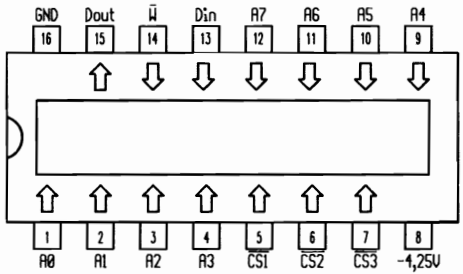


$\overline{CS}$1...3	$\overline{W}$	D_{in}	D_{out}	Mode
one H	X	X	L	not selected
all L	L	L	L	write 0
all L	L	H	L	write 1
all L	H	X	data out	read

10414 Type	Herst. Manuf. Fabr. Prod. Fabr.	Gehäuse Case Boîtier Carcassa Cápsula	Techn. Techn. Techn. Tecn. Tecn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 10414 AJ	Nsc	16-DIC	ECL	0...+75	<780		<10		ECL
DM 10414 J	Nsc	16-DIC	ECL	0...+75	<780		<15		ECL
F 10410 DC	Fch	16-DIC	ECL	0...+75	475		<30		ECL
F 10410 FC	Fch	16-FLAT	ECL	0...+75	475		<30		ECL
F 10410 PC	Fch	16-DIP	ECL	0...+75	475		<30		ECL
F 10414 DC	Fch	16-DIC	ECL	0...+75	<728		<10		ECL
F 10414 FC	Fch	16-FLAT	ECL	0...+75	<728		<10		ECL
HM 2105	Hit	16-DIC	ECL	0...+75	$1,8		<35		ECL

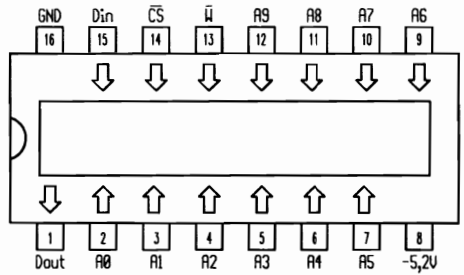
10414 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 2106	Hit	16-DIC	ECL	0...+75	$1,8		<15		ECL
HM 10414	Hit	16-DIC	ECL	0...+75	$2,8		<10		ECL
HM 10414-1	Hit	16-DIC	ECL	0...+75	$2,8		<8		ECL
MCM 10144 F	Mot	16-FLAT	ECL	0...+75	<670		<10		ECL
MCM 10144 L	Mot	16-DIC	ECL	0...+75	<670		<10		ECL
MCM 10152 F	Mot	16-FLAT	ECL	0...+75	<670		<7,5		ECL
MCM 10152 L	Mot	16-DIC	ECL	0...+75	<670		<7,5		ECL
MCM 10544 F	Mot	16-FLAT	ECL	-55...+125	<670		<10		ECL
MCM 10544 L	Mot	16-FLAT	ECL	-55...+125	<670		<10		ECL
MCM 10552 F	Mot	16-FLAT	ECL	-55...+125	<670				ECL
MCM 10552 L	Mot	16-DIC	ECL	-55...+125	<670				ECL
µPB 10144 D	Nip	16-DIC	ECL	0...+75	<520		<25		ECL

10414 — 256x1-Bit RAM (bipolar)



CS1...3	W	D_{in}	D_{out}	Mode
one H	X	X	L	not selected
all L	L	L	L	write 0
all L	L	H	L	write 1
all L	H	X	data out	read

10415 — 1024x1-Bit RAM (bipolar)



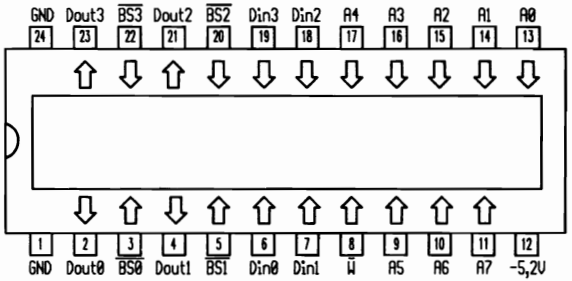
CS	W	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

10414 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 10411 DC	Fch	16-DIC	ECL	0...+75	360		<35		ECL
F 10411 FC	Fch	16-FLAT	ECL	0...+75	360		<35		ECL
F 10411 PC	Fch	16-DIP	ECL	0...+75	360		<35		ECL

10415 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 10415 AJ	Nsc	16-DIC	ECL	0...+75	<780		<20		ECL
DM 10415 J	Nsc	16-DIC	ECL	0...+75	<780		<35		ECL
F 10415A DC	Fch	16-DIC	ECL	0...+75	475		<35		ECL
F 10415A FC	Fch	16-FLAT	ECL	0...+75	475		<35		ECL
F 10415 DC	Fch	16-DIC	ECL	0...+75	475		<60		ECL
F 10415 DC	Fch	16-DIC	ECL	0...+75	<1040		<10		ECL
F 10415 FC	Fch	16-FLAT	ECL	0...+75	475		<60		ECL
F 10415 FC	Fch	16-FLAT	ECL	0...+75	<1040		<10		ECL

10415 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 2110	Hit	16-DIC	ECL	0...+75	$0,5		<35		ECL
HM 2110-1	Hit	16-DIC	ECL	0...+75	$0,5		<25		ECL
HM 2110-2	Hit	16-DIC	ECL	0...+75	$0,5		<20		ECL
HM 2112	Hit	16-DIC	ECL	0...+75	$0,8		<10		ECL
HM 2112-1	Hit	16-DIC	ECL	0...+75	$0,8		<5		ECL
MCM 10146 F	Mot	16-FLAT	ECL	0...+75	<750		<7		ECL
MCM 10146 L	Mot	16-DIC	ECL	0...+75	<750		<7		ECL
MCM 10415 F-15	Mot	16-FLAT	ECL	0...+75	<780		<15		ECL
MCM 10415 F-20	Mot	16-FLAT	ECL	0...+75	<780		<20		ECL
MCM 10415 L-15	Mot	16-DIC	ECL	0...+75	<780		<15		ECL
MCM 10415 L-20	Mot	16-DIC	ECL	0...+75	<780		<20		ECL
MCM 10546 F	Mot	16-FLAT	ECL	0...+75	<750		<10		ECL
MCM 10546 L	Mot	16-DIC	ECL	0...+75	<750		<10		ECL
10415 B	Val	16-DIP	ECL	0...+75	600		<10		ECL

10422 — 256x4-Bit RAM (bipolar)

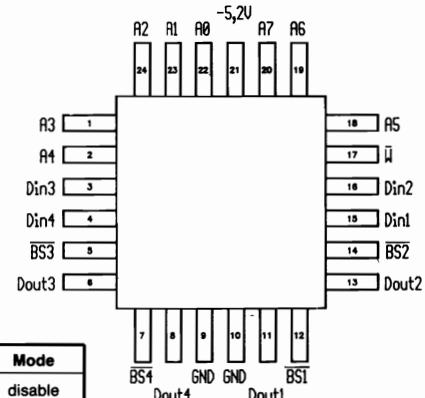


$\overline{CS}$	$\overline{W}$	D_{In}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

10422 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 10422 A-7	Nsc	24-DIC	ECL	0...+75	<1040		<7		ECL
DM 10422 AJ	Nsc	24-DIC	ECL	0...+75	<1040		<10		ECL
DM 10422 J	Nsc	24-DIC	ECL	0...+75	<1040		<12		ECL
F 10422 DC	Fch	24-DIC	ECL	0...+75	<1196		<10		ECL
F 10422 DC	Fch	24-DIC	ECL	0...+75	$1,2		<5		ECL
HM 10422	Hit	24-DIC	ECL	0...+75	$0,8		<10		ECL
HM 10422-7	Hit	24-DIC	ECL	0...+75	$1		<7		ECL
10422 B	Val	24-DIC	ECL	0...+75	980		<10		ECL

10422 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
10422 C	Val	24-DIC	ECL	0...+75	980		<7		ECL
µPB 10422 D-10	Nec	24-DIC	ECL	0...+75	<1200		<10		ECL
µPB 10422 D-7	Nec	24-DIC	ECL	0...+75	<1200		<7		ECL

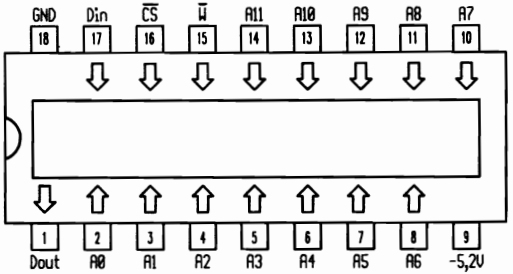
10422 — 256x4-Bit RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

10422 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 10422 AW	Nsc	24-PLCC	ECL	0...+75	<1040		<10		ECL
DM 10422 W	Nsc	24-PLCC	ECL	0...+75	<1040		<12		ECL
DM 10422 W-7	Nsc	24-PLCC	ECL	0...+75	<1040		<7		ECL
F 10422 FC	Fch	24-PLCC	ECL	0...+75	<1196		<10		ECL
F 10422 FC	Fch	24-PLCC	ECL	0...+75	$1,2		<5		ECL

10470 — 4096x1-Bit RAM (bipolar)

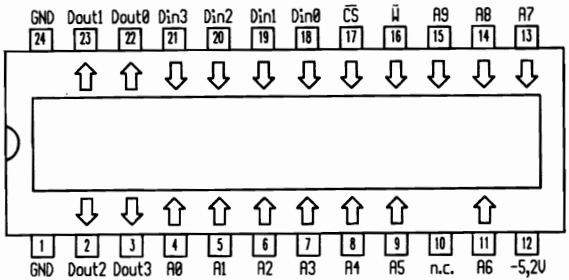


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

10470 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 10470 AJ	Nsc	18-DIC	ECL	0...+75	<1040		<15		ECL
DM 10470 J	Nsc	18-DIC	ECL	0...+75	<1040		<25		ECL
F 10470 DC	Fch	18-DIC	ECL	0...+75	<1040		<35		ECL
F 10470 FC	Fch	18-FLAT	ECL	0...+75	<1040		<35		ECL
HM 10470	Hit	18-DIC	ECL	0...+75	$0,2		<25		ECL
HM 10470-1	Hit	18-DIC	ECL	0...+75	$0,2		<15		ECL
HM 10470-20	Hit	18-DIC	ECL	0...+75	$0,25		<20		ECL
10470 A	Val	18-DIC	ECL	0...+75	<780		<15		ECL

10470 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPB 10470 D-10	Nec	18-DIC	ECL	0...+75	<1200		<10		ECL
µPB 10470 D-15	Nec	18-DIC	ECL	0...+75	<1200		<15		ECL

10474 — 1024x4-Bit RAM (bipolar)

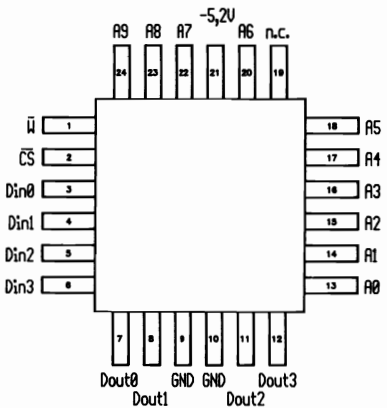


$\overline{CS}$	$\overline{W}$	D_{In}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

10474 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 10474 A-10 J	Nsc	24-DIC	ECL	0...+75	<1248		<10		ECL
DM 10474 A-8 J	Nsc	24-DIC	ECL	0...+75	<1248		<8		ECL
DM 10474 AJ	Nsc	24-DIC	ECL	0...+75	<1144		<15		ECL
F 10474 DC	Fch	24-DIC	ECL	0...+75	$0,29		<10		ECL
HM 10474	Hit	24-DIC	ECL	0...+75	$0,2		<25		ECL
HM 10474-10	Hit	24-DIC	ECL	0...+75	$0,3		<10		ECL
HM 10474-8	Hit	24-DIC	ECL	0...+75	$0,3		<8		ECL
10474 A	Val	24-DIC	ECL	0...+75	<1092		<15		ECL

10474 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPB 10474 D-10	Nec	24-DIC	ECL	0...+75	<1200		<10		ECL
µPB 10474 D-15	Nec	24-DIC	ECL	0...+75	<1200		<15		ECL
µPB 10474 D-8	Nec	24-DIC	ECL	0...+75	<1200		<8		ECL
µPB 10474 D-9	Nec	24-DIC	ECL	0...+75	<1200		<9		ECL

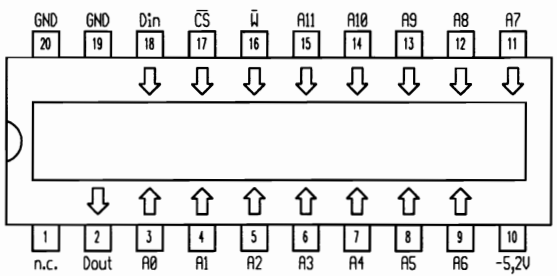
10474 — 1024x4-Bit RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

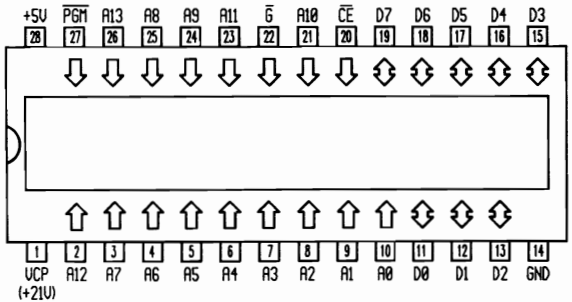
10474 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $	t_{aa} ns	t_{ref} ms	Output
DM 10474 A-10 W	Nsc	24-PLCC	ECL	0...+75	<1248	<10		ECL
DM 10474 A-8 W	Nsc	24-PLCC	ECL	0...+75	<1248	<8		ECL
DM 10474 AW	Nsc	24-PLCC	ECL	0...+75	<1144	<15		ECL
F 10474 FC	Fch	24-PLCC	ECL	0...+75	$0,29	<10		ECL

10480 — 16384x1-Bit ECL RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

27128 — 16384x8-Bit EPROM



$\overline{CE}$	$\overline{G}$	$\overline{Prog}$	VCP	D_{out}	Mode
L	L	H	+5V	data out	read
H	X	X	+5V	Hi-Z	standby
L	X	L	+21V	data in	program
L	L	H	+21V	data out	program verify
H	X	X	+21V	Hi-Z	program inhibit

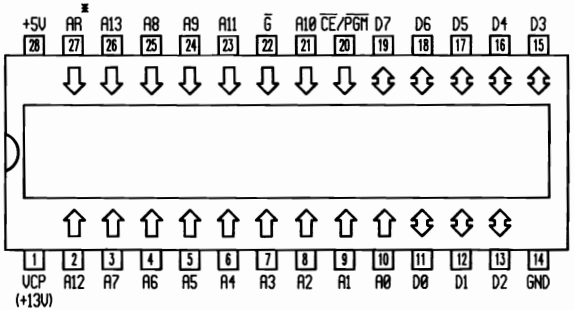
L = −0,1...+0,8V
H = +2...+6V

10480 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 10480	Hit	20-DIC	ECL	0...+75	<676		<25		ECL
HM 10480-15	Hit	20-DIC	ECL	0...+75	<1040		<15		ECL
HM 10480 F	Hit	20-FLAT	ECL	0...+75	<676		<25		ECL
HM 10480 F-15	Hit	20-FLAT	ECL	0...+75	<1040		<15		ECL
HM 10480 L	Hit	20-DIC	ECL	0...+75	<624		<25		ECL

27128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27128 DC	Amd	28-DIC	NMOS	0...+70	<525	<131	<250		TTL-TS
Am 27128-1 DC	Amd	28-DIC	NMOS	0...+70	<525	<131	<150		TTL-TS
Am 27128-15 DC	Amd	28-DIC	NMOS	0...+70	<550	<137	<150		TTL-TS
Am 27128-2 DC	Amd	28-DIC	NMOS	0...+70	<525	<131	<200		TTL-TS
Am 27128-20 DC	Amd	28-DIC	NMOS	0...+70	<550	<137	<200		TTL-TS
Am 27128-25 DC	Amd	28-DIC	NMOS	0...+70	<550	<137	<250		TTL-TS
Am 27128-3 DC	Amd	28-DIC	NMOS	0...+70	<525	<131	<300		TTL-TS
Am 27128-30 DC	Amd	28-DIC	NMOS	0...+70	<550	<137	<300		TTL-TS

27128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27128-4 DC	Amd	28-DIC	NMOS	0...+70	<525	<131	<450		TTL-TS
Am 27128-45 DC	Amd	28-DIC	NMOS	0...+70	<550	<137	<450		TTL-TS
C 27128	Int	28-DIC	NMOS	0...+70	750	225	<250		TTL-TS
C 27128-2	Int	28-DIC	NMOS	0...+70	750	225	<200		TTL-TS
HN 4827128 G-25	Hit	28-DIC	NMOS				<250		TTL-TS
HN 4827128 G-30	Hit	28-DIC	NMOS				<300		TTL-TS
HN 4827128 G-45	Hit	28-DIC	NMOS				<450		TTL-TS
M5L27128 K	Mit	28-DIC	NMOS	-10...+80	<787	<236	<250		TTL-TS
M5L27128 K-2	Mit	28-DIC	NMOS	-10...+80	<787	<236	<200		TTL-TS
M5L27128 K-3	Mit	28-DIC	NMOS	-10...+80	<787	<236	<300		TTL-TS
TMM 27128 D-20	Tos	28-DIC	NMOS	0...+70	600	175	<200		TTL-TS
TMM 27128 D-25	Tos	28-DIC	NMOS	0...+70	600	175	<250		TTL-TS
TMS 27128-20 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<200		TTL-TS
TMS 27128-25 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<250		TTL-TS
TMS 27128-30 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<300		TTL-TS
TMS 27128-35 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<350		TTL-TS
µPD 27128 D	Nip	28-DIP	NMOS	-10...+80	<525	<137	<250		TTL-TS
µPD 27128 D-2	Nip	28-DIP	NMOS	-10...+80	<525	<137	<200		TTL-TS
µPD 27128 D-3	Nip	28-DIP	NMOS	-10...+80	<525	<137	<300		TTL-TS
µPD 27128 D-4	Nip	28-DIP	NMOS	-10...+80	<525	<137	<450		TTL-TS

27128 — 16384x8-Bit EPROM



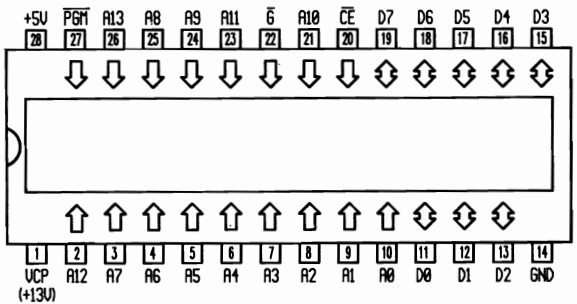
* = AR held at ViH

$\overline{CE}/\overline{PGM}$	$\overline{G}$	V_{pp}	V_{cc}	D_{out}	Mode
L	L	+5V	+5V	data out	read
L	X	+5V	+5V	Hi-Z	standby
pulsed H⊓L	H	+13V	+6V	data in	program
H	L	+13V	+6V	data out	program verify
H	H	+13V	+6V	Hi-Z	program inhibit

27128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27CP128 Q200	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<200		TTL-TS
NMC 27CP128 Q250	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<250		TTL-TS
NMC 27CP128 Q300	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<300		TTL-TS

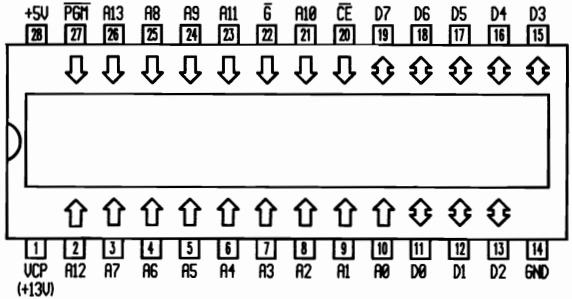
27128

16384x8-Bit PROM



27128 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 27P128-20 NL	Tix	28-DIP	NMOS	0...+70	<100		<200		TTL-TS
TMX 27P128-25 NL	Tix	28-DIP	NMOS	0...+70	<100		<250		TTL-TS
TMX 27P128-35 NL	Tix	28-DIP	NMOS	0...+70	<100		<350		TTL-TS
TMX 27PC128-20 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<200		TTL-TS
TMX 27PC128-25 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<250		TTL-TS
TMX 27PC128-2 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<200		TTL-TS
TMX 27PC128-30 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<300		TTL-TS
TMX 27PC128-3 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<300		TTL-TS
TMX 27PC128-45 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<450		TTL-TS
TMX 27PC128-4 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<450		TTL-TS
TMX 27PC128 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<250		TTL-TS

27128 — 16384x8-Bit EPROM



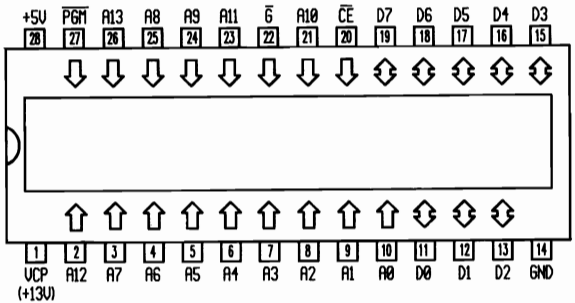
CE	G	A9	PGM	V_{pp}	V_{cc}	D_n	Mode
L	L	X	H	+5V	+5V	data out	read
L	H	X	H	+5V	+5V	Hi-Z	output disable
H	X	X	X	+5V	+5V	Hi-Z	standby
L	H	X	L	+12V	+5V	data in	fast programming
L	L	X	H	+12V	+5V	data out	verify
H	X	X	X	+12V	+5V	Hi-Z	program inhibit
L	L	H	H	+5V	+5V	codes	electronic signature

27128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 27128 AG-17	Hit	28-DIC	NMOS	0...+70	<550	<192,5	<170		TTL-TS
HN 27128 AG-20	Hit	28-DIC	NMOS	0...+70	<550	<192,5	<200		TTL-TS
HN 27128 AG-25	Hit	28-DIC	NMOS	0...+70	<550	<192,5	<250		TTL-TS
HN 27128 AG-30	Hit	28-DIC	NMOS	0...+70	<550	<192,5	<300		TTL-TS
M 27128 A-25F1	Sgs	28-DIC	NMOS	0...+70	<467	<220	<250		TTL-TS
M 27128 A-2F1	Sgs	28-DIC	NMOS	0...+70	<446	<210	<200		TTL-TS
M 27128 A-30F1	Sgs	28-DIC	NMOS	0...+70	<467	<220	<300		TTL-TS
M 27128 A-3F1	Sgs	28-DIC	NMOS	0...+70	<446	<210	<300		TTL-TS

27128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 27128 A-45F1	Sgs	28-DIC	NMOS	0...+70	<467	<220	<450		TTL-TS
M 27128 A-4F1	Sgs	28-DIC	NMOS	0...+70	<446	<210	<450		TTL-TS
M 27128 A-4F6	Sgs	28-DIC	NMOS	-40...+85	<446	<210	<450		TTL-TS
M 27128 AF1	Sgs	28-DIC	NMOS	0...+70	<446	<210	<250		TTL-TS
M 27128 AF6	Sgs	28-DIC	NMOS	-40...+85	<446	<210	<250		TTL-TS
SMJ 27C128-20 J	Tix	28-DIC	CMOS	-55...+125	<137,5	<2,75	<200		TTL-TS
SMJ 27C128-25 J	Tix	28-DIC	CMOS	-55...+125	<137,5	<2,75	<250		TTL-TS
SMJ 27C128-30 J	Tix	28-DIC	CMOS	-55...+125	<137,5	<2,75	<300		TTL-TS
TMS 27C128-100 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<100		TTL-TS
TMS 27C128-100 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<100		TTL-TS
TMS 27C128-120 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<120		TTL-TS
TMS 27C128-120 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<120		TTL-TS
TMS 27C128-12 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<120		TTL-TS
TMS 27C128-12 JL	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<120		TTL-TS
TMS 27C128-15 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27C128-15 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<150		TTL-TS
TMS 27C128-1 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27C128-1 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<150		TTL-TS
TMS 27C128-20 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27C128-20 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<200		TTL-TS
TMS 27C128-25 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27C128-25 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<250		TTL-TS
TMS 27C128-2 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27C128-2 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<200		TTL-TS
TMS 27C128-30 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<300		TTL-TS
TMS 27C128-3 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<300		TTL-TS
TMS 27C128-45 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<450		TTL-TS
TMS 27C128-4 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<450		TTL-TS
TMS 27C128 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27C128 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<250		TTL-TS

27128

16384x8-Bit EPROM

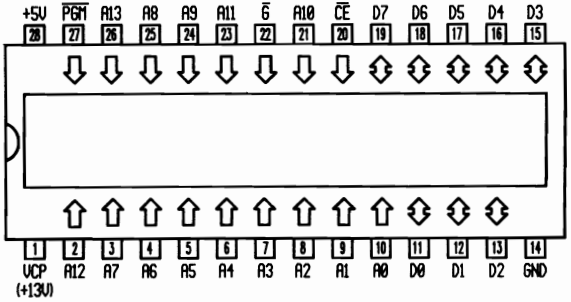


$\overline{CE}$	$\overline{G}$	V_{PP}	V_{CC}	D_n	Mode
L	L	+5V	+5V	data out	read
H	X	+5V	+5V	Hi-Z	standby
H⊓L	H	+12,5V	+6V	data in	program
H	L	+12,5V	+6V	data out	program verify
H	H	+12,5V	+6V	Hi-Z	program inhibit

27128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27C128 BQ45	Nsc	28-DIC	CMOS	0...+70	<360		<45		TTL-TS
NMC 27C128 BQ55	Nsc	28-DIC	CMOS	0...+70	<360		<55		TTL-TS
NMC 27C128 BQ70	Nsc	28-DIC	CMOS	0...+70	<360		<70		TTL-TS
TMM 27128 AD-15	Tos	28-DIP	NMOS	0...+70	<550	<165	<150		TTL-TS
TMM 27128 AD-150	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<150		TTL-TS
TMM 27128 AD-20	Tos	28-DIP	NMOS	0...+70	<550	<165	<200		TTL-TS
TMM 27128 AD-200	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<200		TTL-TS
TMM 27128 ADI-15	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<150		TTL-TS
TMM 27128 ADI-20	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<200		TTL-TS
TMX 27128 A-20 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<200		TTL-TS
TMX 27128 A-20 NL	Tix	28-DIP	NMOS	0...+70	<525	<210	<200		TTL-TS
TMX 27128 A-25 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<250		TTL-TS
TMX 27128 A-25 NL	Tix	28-DIP	NMOS	0...+70	<525	<210	<250		TTL-TS
TMX 27128 A-35 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<350		TTL-TS
TMX 27128 A-35 NL	Tix	28-DIP	NMOS	0...+70	<525	<210	<350		TTL-TS

27128

16384x8-Bit PROM



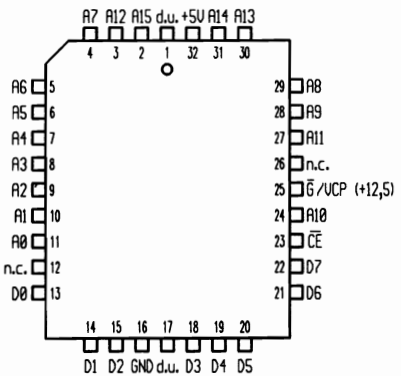
$\overline{CE}$	$\overline{G}$	A9	$\overline{PGM}$	V_{pp}	V_{cc}	D_n	Mode
L	L	X	H	+5V	+5V	data out	read
L	H	X	H	+5V	+5V	Hi-Z	output disable
H	X	X	X	+5V	+5V	Hi-Z	standby
L	H	X	L	+12V	+5V	data in	fast programming
L	L	X	H	+12V	+5V	data out	verify
H	X	X	X	+12V	+5V	Hi-Z	program inhibit
L	L	H	H	+5V	+5V	codes	electronic signature

27128 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC128-15 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27PC128-15 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27PC128-1 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27PC128-1 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27PC128-20 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC128-20 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC128-25 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC128-25 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<250		TTL-TS

27128 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC128-2 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27PC128-2 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC128 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC128 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS

27128

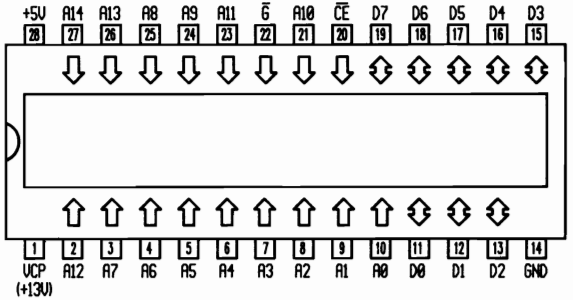
16384x8-Bit PROM



$\overline{CE}$	$\overline{G}$	A9	$\overline{PGM}$	V_{pp}	V_{cc}	D_n	Mode
L	L	X	H	+5V	+5V	data out	read
L	H	X	H	+5V	+5V	Hi-Z	output disable
H	X	X	X	+5V	+5V	Hi-Z	standby
L	H	X	L	+12V	+5V	data in	fast programming
L	L	X	H	+12V	+5V	data out	verify
H	X	X	X	+12V	+5V	Hi-Z	program inhibit
L	L	H	H	+5V	+5V	codes	electronic signature

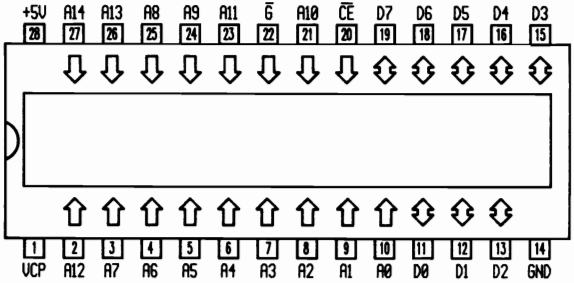
27128 Type	Man	Case	Techn.	T_{ij}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC128-15 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27PC128-15 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27PC128-1 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27PC128-1 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27PC128-20 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC128-20 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC128-25 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC128-25 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27PC128-2 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27PC128-2 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC128 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC128 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS

27256 — 32768x8-Bit PROM



27256 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
TMX 27P256-20 NL	Tix	28-DIP	NMOS	0...+70	<100		<200		TTL-TS
TMX 27P256-25 NL	Tix	28-DIP	NMOS	0...+70	<100		<250		TTL-TS
TMX 27P256-35 NL	Tix	28-DIP	NMOS	0...+70	<100		<350		TTL-TS
TMX 27PC256-20 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<200		TTL-TS
TMX 27PC256-25 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<250		TTL-TS
TMX 27PC256-2 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<200		TTL-TS
TMX 27PC256-30 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<300		TTL-TS
TMX 27PC256-3 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<300		TTL-TS
TMX 27PC256-45 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<450		TTL-TS
TMX 27PC256-4 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<450		TTL-TS
TMX 27PC256 NL	Tix	28-DIP	CMOS	0...+70	<210	1,4	<250		TTL-TS

27256 — 32768x8-BIT EPROM

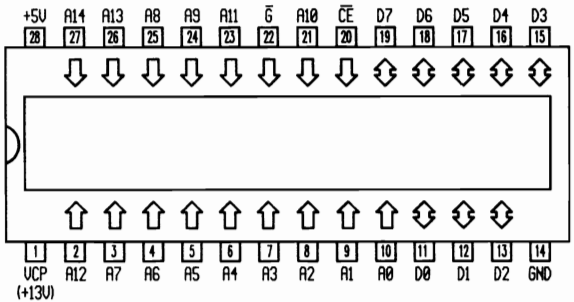


CE	G	VCP	Dn	Mode
L	L	+5V	data out	read
L⎍H*	H	+25V	data in	program
L	L	+25V	data out	program verify
H	X	+5V	Hi-Z	standby

* = one 50ms pulse (active high)

27256 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
C 27256	Int	28-DIC	NMOS	0...+70	500	200	<250		TTL-TS

27256 — 32768x8-Bit EPROM



CE/ALE	Ḡ	V_{pp}	V_{cc}	D_n	Mode
L	L	+ 5V	+ 5V	data out	read
H	X	+ 5V	+ 5V	Hi-Z	standby
H⌐L	H	+ 12,5V	+ 6V	data in	program
H	L	+ 12,5V	+ 6V	data out	program verify
H	H	+ 12,5V	+ 6V	Hi-Z	program inhibit

V_{pp} + 13V bei NMC 27256

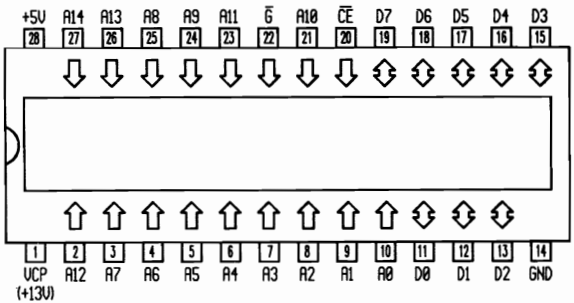
27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 27C256 FP-20	Hit	28-FLAT	CMOS	0...+70	<165	<5,5	<200		TTL-TS
HN 27C256 FP-25	Hit	28-FLAT	CMOS	0...+70	<165	<5,5	<250		TTL-TS
HN 27C256 FP-30	Hit	28-FLAT	CMOS	0...+70	<165	<5,5	<300		TTL-TS
HN 27C256 G-17	Hit	28-DIC	CMOS	0...+70	<165	<5,5	<170		TTL-TS
HN 27C256 G-20	Hit	28-DIC	CMOS	0...+70	<165	<5,5	<200		TTL-TS
HN 27C256 G-25	Hit	28-DIC	CMOS	0...+70	<165	<5,5	<250		TTL-TS
HN 27C256 G-30	Hit	28-DIC	CMOS	0...+70	<165	<5,5	<300		TTL-TS
HN 27256 G-25	Hit	28-DIC	NMOS	0...+70	<550	<220	<250		TTL-TS

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 27256 G-30	Hit	28-DIC	NMOS	0...+70	<550	<220	<300		TTL-TS
M 27256-1 F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<170		TTL-TS
M 27256-20 F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<200		TTL-TS
M 27256-25F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<250		TTL-TS
M 27256-2F1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<200		TTL-TS
M 27256-30F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<300		TTL-TS
M 27256-3F1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<300		TTL-TS
M 27256-45F1	Sgs	28-DIC	NMOS	0...+70	<550	<220	<450		TTL-TS
M 27256-4F1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<450		TTL-TS
M 27256-4F6	Sgs	28-DIC	NMOS	-40...+85	<525	<210	<450		TTL-TS
M 27256 F1	Sgs	28-DIC	NMOS	0...+70	<525	<210	<250		TTL-TS
M 27256 F6	Sgs	28-DIC	NMOS	-40...+85	<525	<210	<250		TTL-TS
NMC 27C256 BQ90	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<90		TTL-TS
NMC 27C256 BQ120	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<120		TTL-TS
NMC 27C256 BQ150	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<150		TTL-TS
NMC 27C256 BQ200	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<200		TTL-TS
NMC 27C256 BQE120	Nsc	28-DIC	CMOS	-40...+85	<220	<0,55	<120		TTL-TS
NMC 27C256 BQM150	Nsc	28-DIC	CMOS	-55...+125	<220	<0,55	<150		TTL-TS
SMJ 27C256-20 J	Tix	28-DIC	CMOS	-55...+125	<137,5	<2,75	<200		TTL-TS
SMJ 27C256-25 J	Tix	28-DIC	CMOS	-55...+125	<137,5	<2,75	<250		TTL-TS
SMJ 27C256-30 J	Tix	28-DIC	CMOS	-55...+125	<137,5	<2,75	<300		TTL-TS
TC 57256 AD-15	Tos	28-DIP	CMOS	0...+70	<157,5	<5,25	<150		TTL-TS
TC 57256 AD-20	Tos	28-DIP	CMOS	0...+70	<157,5	<5,25	<200		TTL-TS
TMM 27256 AD-15	Tos	28-DIP	NMOS	0...+70	<550	<165	<150		TTL-TS
TMM 27256 AD-150	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<150		TTL-TS
TMM 27256 AD-20	Tos	28-DIP	NMOS	0...+70	<550	<165	<200		TTL-TS
TMM 27256 AD-200	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<200		TTL-TS
TMM 27256 ADI-15	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<150		TTL-TS
TMM 27256 ADI-20	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<200		TTL-TS
TMS 27256-20 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<200		TTL-TS
TMS 27256-25 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<250		TTL-TS
TMS 27256-35 JL	Tix	28-DIC	NMOS	0...+70	<525	<210	<350		TTL-TS
TMS 27C256-120 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<120		TTL-TS
TMS 27C256-120 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<120		TTL-TS
TMS 27C256-12 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<120		TTL-TS
TMS 27C256-12 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<120		TTL-TS
TMS 27C256-150 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27C256-150 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27C256-15 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27C256-15 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27C256-17 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<170		TTL-TS
TMS 27C256-17 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<170		TTL-TS
TMS 27C256-1 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<170		TTL-TS
TMS 27C256-1 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<170		TTL-TS
TMS 27C256-20 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27C256-20 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<200		TTL-TS
TMS 27C256-25 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27C256-25 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<250		TTL-TS
TMS 27C256-2 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27C256-2 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<200		TTL-TS
TMS 27C256-30 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<300		TTL-TS
TMS 27C256-3 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<300		TTL-TS
TMS 27C256-45 JL	Tix	28-DIC	CMOS	0...+70	<220	<2,75	<450		TTL-TS
TMS 27C256-4 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<450		TTL-TS
TMS 27C256 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27C256 JL	Tix	28-DIC	CMOS	0...+70	<210	<2,62	<250		TTL-TS
TS 27C256-15 CQ	Tho	28-DIC	CMOS	0...+70	<440	<5,5	<150		TTL-TS
TS 27C256-15 VQ	Tho	28-DIC	CMOS	-40...+85	<440	<5,5	<150		TTL-TS
TS 27C256-15 XCQ	Sgs	28-DIC	CMOS	0...+70	<157,5	<5,25	<150		TTL-TS
TS 27C256-17 CQ	Sgs	28-DIC	CMOS	0...+70	<165	<5,5	<170		TTL-TS
TS 27C256-17 XCQ	Sgs	28-DIC	CMOS	0...+70	<157,5	<5,25	<170		TTL-TS
TS 27C256-20 CQ	Tho	28-DIC	CMOS	0...+70	<440	<5,5	<200		TTL-TS
TS 27C256-20 VQ	Tho	28-DIC	CMOS	-40...+85	<440	<5,5	<200		TTL-TS
TS 27C256-20 XCQ	Sgs	28-DIC	CMOS	0...+70	<157,5	<5,25	<200		TTL-TS
TS 27C256-25 CQ	Tho	28-DIC	CMOS	0...+70	<440	<5,5	<250		TTL-TS
TS 27C256-25 VQ	Tho	28-DIC	CMOS	-40...+85	<440	<5,5	<250		TTL-TS
TS 27C256-25 XCQ	Sgs	28-DIC	CMOS	0...+70	<157,5	<5,25	<250		TTL-TS
TS 27C256-30 CQ	Tho	28-DIC	CMOS	0...+70	<440	<5,5	<300		TTL-TS
TS 27C256-30 VQ	Tho	28-DIC	CMOS	-40...+85	<440	<5,5	<300		TTL-TS
TS 27C256-30 XCQ	Sgs	28-DIC	CMOS	0...+70	<157,5	<5,25	<300		TTL-TS
27C256-12 FA	Phi	28-DIC	CMOS	0...+70	<110	<0,55	<120		TTL-TS
27C256-15 FA	Phi	28-DIC	CMOS	0...+70	<110	<0,55	<150		TTL-TS
27C256-17	Val	28-DIC	CMOS	0...+70	<165	<11	<170		TTL-TS
27C256-17 FA	Phi	28-DIC	CMOS	0...+70	<110	<0,55	<170		TTL-TS

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
27C256-20	Val	28-DIC	CMOS	0...+70	<165	<11	<200		TTL-TS
27C256-20 FA	Phi	28-DIC	CMOS	0...+70	<110	<0,55	<200		TTL-TS
27C256-25	Val	28-DIC	CMOS	0...+70	<165	<11	<250		TTL-TS
27C256-30	Val	28-DIC	CMOS	0...+70	<165	<11	<300		TTL-TS
27C256I15 FA	Phi	28-DIC	CMOS	-40...+85	<550	<5,5	<150		TTL-TS
27C256I15 N	Phi	28-DIP	CMOS	-40...+85	<550	<5,5	<150		TTL-TS
27C256I20 FA	Phi	28-DIC	CMOS	-40...+85	<550	<5,5	<200		TTL-TS
27C256I20 N	Phi	28-DIP	CMOS	-40...+85	<550	<5,5	<200		TTL-TS

27256 — 32768x8-Bit EPROM



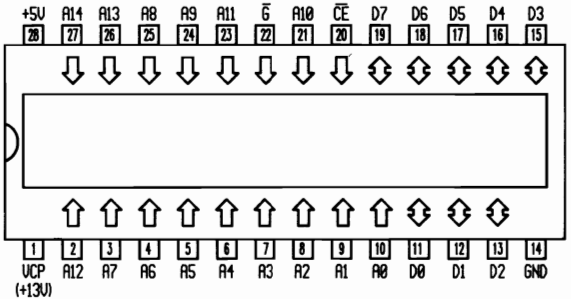
CE/ALE	G	V_{pp}	V_{cc}	D_n	Mode
L	L	+5V	+5V	data out	read
H	X	+5V	+5V	Hi-Z	standby
H⌐L	H	+12,5V	+6V	data in	program
H	L	+12,5V	+6V	data out	program verify
H	H	+12,5V	+6V	Hi-Z	program inhibit

V_{pp} + 13V bei NMC 27256

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 57256 AD-12	Tos	28-DIP	CMOS	0...+70	<157,5	<5,25	<120		TTL-TS
TC 57256 AD-120	Tos	28-DIP	CMOS	0...+70	<165	<5,5	<120		TTL-TS
TC 57256 AD-150	Tos	28-DIP	CMOS	0...+70	<165	<5,5	<150		TTL-TS
TMM 27256 BD-15	Tos	28-DIP	NMOS	0...+70	<550	<165	<150		TTL-TS
TMM 27256 BD-150	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<150		TTL-TS
TMM 27256 BD-20	Tos	28-DIP	NMOS	0...+70	<550	<165	<200		TTL-TS
TMM 27256 BD-200	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<200		TTL-TS
TMM 27256 BDI-15	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<150		TTL-TS
TMM 27256 BDI-20	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<200		TTL-TS

27256

32768x8-Bit PROM



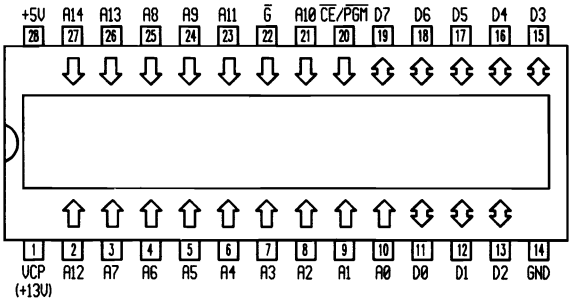
C̄Ē/ALE	Ḡ	V_{pp}	V_{cc}	D_n	Mode
L	L	+5V	+5V	data out	read
H	X	+5V	+5V	Hi-Z	standby
H⌐L	H	+12,5V	+6V	data in	program
H	L	+12,5V	+6V	data out	program verify
H	H	+12,5V	+6V	Hi-Z	program inhibit

V_{pp} + 13V bei NMC 27256

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC256-150 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27PC256-150 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27PC256-15 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<150		TTL-TS
TMS 27PC256-15 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27PC256-17 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<170		TTL-TS
TMS 27PC256-17 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<170		TTL-TS
TMS 27PC256-1 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<170		TTL-TS
TMS 27PC256-1 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<170		TTL-TS

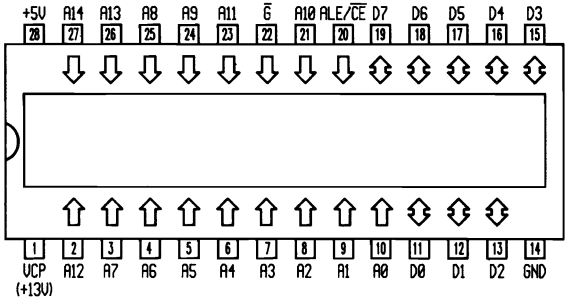
27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC256-20 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC256-20 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC256-25 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC256-25 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27PC256-2 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27PC256-2 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC256 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC256 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS

27256 — 32768x8-Bit EPROM



$\overline{CE}/\overline{PGM}$	$\overline{G}$	V_{pp}	V_{cc}	D_{out}	Mode
L	L	+5V	+5V	data out	read
L	X	+5V	+5V	Hi-Z	standby
pulsed H⌐L L	H	+13V	+6V	data in	program
H	L	+13V	+6V	data out	program verify
H	H	+13V	+6V	Hi-Z	program inhibit

27256 — 32768x8-Bit EPROM



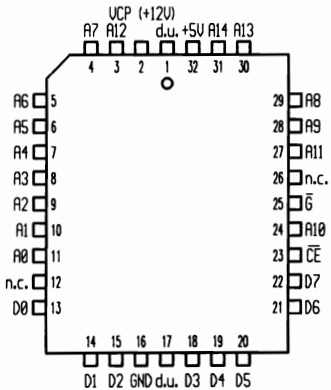
$\overline{CE}/ALE$	$\overline{G}$	V_{pp}	V_{cc}	D_n	Mode
L	L	+5V	+5V	data out	read
H	X	+5V	+5V	Hi-Z	standby
H⌐L L	H	+12,5V	+6V	data in	program
H	L	+12,5V	+6V	data out	program verify
H	H	+12,5V	+6V	Hi-Z	program inhibit

V_{pp} + 13V bei NMC 27256

27256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27C256 Q17	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<170		TTL-TS
NMC 27C256 Q200	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<200		TTL-TS
NMC 27C256 Q250	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<250		TTL-TS
NMC 27C256 Q300	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<300		TTL-TS
NMC 27C256 QE250	Nsc	28-DIC	CMOS	-40...+85	<55	<0,55	<250		TTL-TS
NMC 27C256 QM250	Nsc	28-DIC	CMOS	-55...+125	<55	<0,55	<250		TTL-TS
NMC 27C256 QM350	Nsc	28-DIC	CMOS	-55...+125	<55	<0,55	<350		TTL-TS

27256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
87C256-20	Val	28-DIC	CMOS	0...+70	<165	<11	<200		TTL-TS
87C256-30	Val	28-DIC	CMOS	0...+70	<165	<11	<300		TTL-TS

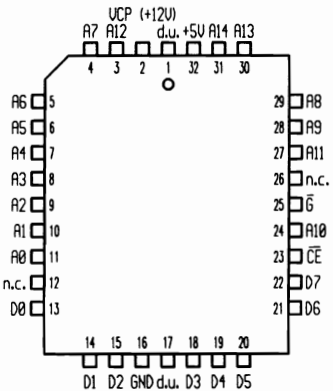
27256 — 32768x8-Bit EPROM



CE	G	V_{PP}	V_{CC}	D_n	Mode
L	L	+5V	+5V	data out	read
H	X	+5V	+5V	Hi-Z	standby
H⊓L	H	+12,5V	+6V	data in	program
H	L	+12,5V	+6V	data out	program verify
H	H	+12,5V	+6V	Hi-Z	program inhibit

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
27C256I15 A	Phi	32-LCC	CMOS	-40...+85	<550	<5,5	<150		TTL-TS
27C256I20 A	Phi	32-LCC	CMOS	-40...+85	<550	<5,5	<200		TTL-TS

27256 — 32768x8-Bit PROM

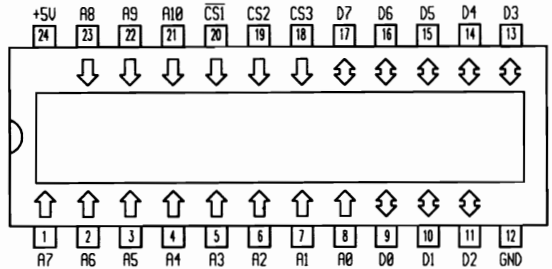


CE	G	V_{PP}	V_{CC}	D_n	Mode
L	L	+5V	+5V	data out	read
H	X	+5V	+5V	Hi-Z	standby
H⊓L	H	+12,5V	+6V	data in	program
H	L	+12,5V	+6V	data out	program verify
H	H	+12,5V	+6V	Hi-Z	program inhibit

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC256-150FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<150		TTL-TS
TMS 27PC256-150FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<150		TTL-TS
TMS 27PC256-15 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<150		TTL-TS

27256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC256-15 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<150		TTL-TS
TMS 27PC256-17 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<170		TTL-TS
TMS 27PC256-17 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<170		TTL-TS
TMS 27PC256-1 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<170		TTL-TS
TMS 27PC256-1 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<170		TTL-TS
TMS 27PC256-20 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC256-20 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC256-25 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC256-25 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27PC256-2 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27PC256-2 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC256 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC256 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS

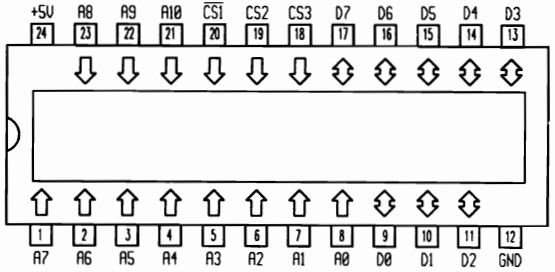
27291 — 2048x8-Bit EPROM



$\overline{CS1}$	CS2	CS3	A9	A0	Dn	Mode
L	H	H	x	x	data out	read
H	x	x	x	x	Hi-Z	output disable
x	L	x	x	x	Hi-Z	output disable
x	x	L	x	x	Hi-Z	output disable
+12V	L	H	x	x	data out	program verify
+12V	H	H	x	x	Hi-Z	program inhibit
+12V	H	L	x	x	data in	fast program
L	L	+12V	x	x	H-Level	blank check H-Level
L	H	+12V	x	x	L-Level	blank check L-Level
L	H	+12V	+12V	L	code 97	signature
L	H	+12V	+12V	H	code 02	signature

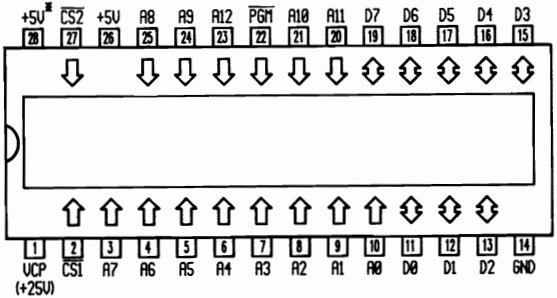
27291 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27C291-35 JL	Tix	24-TDIC	CMOS	0...+70	<412,5		<35		TTL-TS
TMS 27C291-3 JL	Tix	24-TDIC	CMOS	0...+70	<394		<35		TTL-TS
TMS 27C291-45 JL	Tix	24-TDIC	CMOS	0...+70	<330		<45		TTL-TS
TMS 27C291-50 JL	Tix	24-TDIC	CMOS	0...+70	<302,5		<50		TTL-TS
TMS 27C291-5 JL	Tix	24-TDIC	CMOS	0...+70	<289		<50		TTL-TS
TMS 27C291 JL	Tix	24-TDIC	CMOS	0...+70	<315		<45		TTL-TS
TMS 27C292-35 JL	Tix	24-DIC	CMOS	0...+70	<412,5		<35		TTL-TS
TMS 27C292-3 JL	Tix	24-DIC	CMOS	0...+70	<394		<35		TTL-TS
TMS 27C292-45 JL	Tix	24-DIC	CMOS	0...+70	<330		<45		TTL-TS
TMS 27C292-50 JL	Tix	24-DIC	CMOS	0...+70	<302,5		<50		TTL-TS
TMS 27C292-5 JL	Tix	24-DIC	CMOS	0...+70	<289		<50		TTL-TS
TMS 27C292 JL	Tix	24-DIC	CMOS	0...+70	<315		<45		TTL-TS

27291 — 2048x8-Bit PROM



$\overline{CS1}$	CS2	CS3	A9	A0	Dn	Mode
L	H	H	x	x	data out	read
H	x	x	x	x	Hi-Z	output disable
x	L	x	x	x	Hi-Z	output disable
x	x	L	x	x	Hi-Z	output disable
+12V	L	H	x	x	data out	program verify
+12V	H	H	x	x	Hi-Z	program inhibit
+12V	H	L	x	x	data in	fast program
L	L	+12V	x	x	H-Level	blank check H-Level
L	H	+12V	x	x	L-Level	blank check L-Level
L	H	+12V	+12V	L	code 97	signature
L	H	+12V	+12V	H	code 02	signature

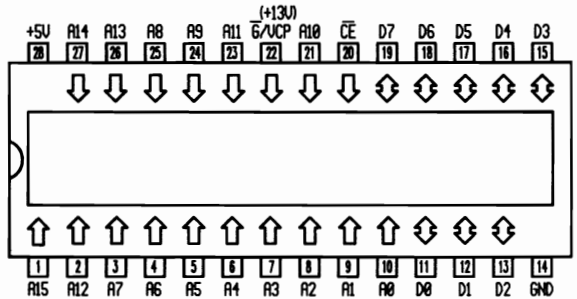
27291 Type	Man	Case	Techn.	T_{Uj}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC291-35 NL	Tix	24-TDIP	CMOS	0...+70	<413		<35		TTL-TS
TMS 27PC291-3 NL	Tix	24-TDIP	CMOS	0...+70	<394		<35		TTL-TS
TMS 27PC291-45 NL	Tix	24-TDIP	CMOS	0...+70	<330		<45		TTL-TS
TMS 27PC291-50 NL	Tix	24-TDIP	CMOS	0...+70	<303		<50		TTL-TS
TMS 27PC291-5 NL	Tix	24-TDIP	CMOS	0...+70	<289		<50		TTL-TS
TMS 27PC291 NL	Tix	24-TDIP	CMOS	0...+70	<315		<45		TTL-TS



$\overline{CS1}$	CS2	CS3	A9	A0	Dn	Mode
L	H	H	x	x	data out	read
H	x	x	x	x	Hi-Z	output disable
x	L	x	x	x	Hi-Z	output disable
x	x	L	x	x	Hi-Z	output disable
+12V	L	H	x	x	data out	program verify
+12V	H	H	x	x	Hi-Z	program inhibit
+12V	H	L	x	x	data in	fast program
L	L	+12V	x	x	H-Level	blank check H-Level
L	H	+12V	x	x	L-Level	blank check L-Level
L	H	+12V	+12V	L	code 97	signature
L	H	+12V	+12V	H	code 02	signature

27291 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC291-35 FNL	Tix	28-PLCC	CMOS	0...+70	<412,5		<35		TTL-TS
TMS 27PC291-3 FNL	Tix	28-PLCC	CMOS	0...+70	<394		<35		TTL-TS
TMS 27PC291-45 FNL	Tix	28-PLCC	CMOS	0...+70	<330		<45		TTL-TS
TMS 27PC291-50 FNL	Tix	28-PLCC	CMOS	0...+70	<302,5		<50		TTL-TS
TMS 27PC291-5 FNL	Tix	28-PLCC	CMOS	0...+70	<289		<50		TTL-TS
TMS 27PC291 FNL	Tix	28-PLCC	CMOS	0...+70	<315		<45		TTL-TS

27512 — 65536x8-Bit EPROM

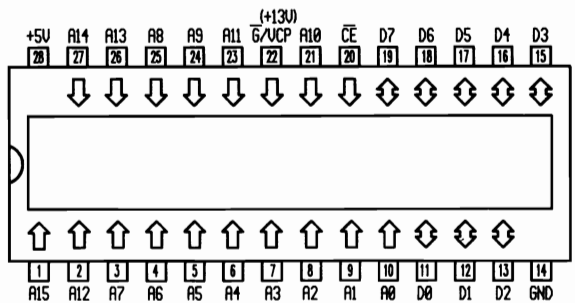


$\overline{CE}$	$\overline{G}/V_{pp}$	V_{cc}	D_n	Mode
L	L	+5V	data out	read
H	X	+5V	Hi-Z	standby
H⌐L L	+13V	+6V	data in	program
L	L	+6V	data out	program verify
H	+13V	+6V	Hi-Z	program inhibit

27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M 27512-25 F1	Sgs	28-DIC	NMOS	0...+70	<687	<220	<250		TTL-TS
M 27512-2 F1	Sgs	28-DIC	NMOS	0...+70	<687,5	<220	<200		TTL-TS
M 27512-30 F1	Sgs	28-DIC	NMOS	0...+70	<687	<220	<300		TTL-TS
M 27512-3 F1	Sgs	28-DIC	NMOS	0...+70	<656	<210	<300		TTL-TS
M 27512 F1	Sgs	28-DIC	NMOS	0...+70	<656	<210	<250		TTL-TS
M 27512 F6	Sgs	28-DIC	NMOS	-40...+85	<687,5	<220	<250		TTL-TS
NMC 27C512 Q20	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<200		TTL-TS
NMC 27C512 Q250	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<250		TTL-TS

27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
NMC 27C512 Q300	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<300		TTL-TS
NMC 27C512 Q350	Nsc	28-DIC	CMOS	0...+70	<55	<0,55	<350		TTL-TS
NMC 27C512 QE250	Nsc	28-DIC	CMOS	-40...+85	<55	<0,55	<250		TTL-TS
NMC 27C512 QM350	Nsc	28-DIC	CMOS	-55...+125	<55	<0,55	<350		TTL-TS
27C512-15 FA	Phi	28-DIC	CMOS	0...+70	<110	<5,5	<150		TTL-TS
27C512-17 FA	Phi	28-DIC	CMOS	0...+70	<110	<5,5	<170		TTL-TS
27C512-20 FA	Phi	28-DIC	CMOS	0...+70	<110	<5,5	<200		TTL-TS

27512 — 65536x8-Bit EPROM

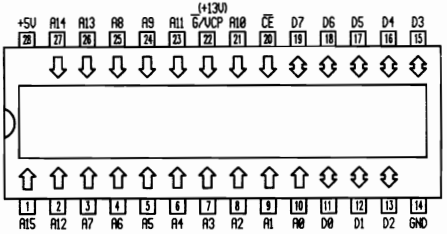


$\overline{CE}$	$\overline{G}/V_{pp}$	V_{cc}	D_n	Mode
L	L	+5V	data out	read
H	X	+5V	Hi-Z	standby
H⌐L	+12,5V	+6V	data in	program
L	L	+6V	data out	program verify
H	+12,5V	+6V	Hi-Z	program inhibit

27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 27C512 G-25	Hit	28-DIC	NMOS	0...+70	<550	<220	<250		TTL-TS
HN 27C512 G-30	Hit	28-DIC	NMOS	0...+70	<550	<220	<300		TTL-TS
NMC 27C512 AQ120	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<120		TTL-TS
NMC 27C512 AQ150	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<150		TTL-TS
NMC 27C512 AQ200	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<200		TTL-TS
NMC 27C512 AQ90	Nsc	28-DIC	CMOS	0...+70	<220	<0,55	<90		TTL-TS
NMC 27C512 AQE120	Nsc	28-DIC	CMOS	-40...+85	<220	<0,55	<120		TTL-TS
NMC 27C512 AQM150	Nsc	28-DIC	CMOS	-55...+125	<220	<0,55	<150		TTL-TS

27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SMJ 27C512-20 J	Tix	28-DIC	CMOS	-55...+125	<275	<2,75	<200		TTL-TS
SMJ 27C512-25 J	Tix	28-DIC	CMOS	-55...+125	<275	<2,75	<250		TTL-TS
SMJ 27C512-30 J	Tix	28-DIC	CMOS	-55...+125	<275	<2,75	<300		TTL-TS
TMM 27512 D-20	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<200		TTL-TS
TMM 27512 D-200	Tos	28-DIP	NMOS	0...+70	<715	<220	<200		TTL-TS
TMM 27512 D-25	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<250		TTL-TS
TMM 27512 D-250	Tos	28-DIP	NMOS	0...+70	<715	<220	<250		TTL-TS
TMM 27512 DI-20	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<200		TTL-TS
TMM 27512 DI-25	Tos	28-DIP	NMOS	-40...+85	<660	<192,5	<250		TTL-TS
TMS 27C512-17 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<170		TTL-TS
TMS 27C512-17 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<170		TTL-TS
TMS 27C512-1 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<170		TTL-TS
TMS 27C512-1 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<170		TTL-TS
TMS 27C512-20 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27C512-20 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27C512-25 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27C512-25 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27C512-2 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27C512-2 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27C512-30 JE	Tix	28-DIC	CMOS	-40...+85	<165	<2,75	<300		TTL-TS
TMS 27C512-30 JL	Tix	28-DIC	CMOS	0...+70	<165	<2,75	<300		TTL-TS
TMS 27C512-3 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<300		TTL-TS
TMS 27C512-3 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<300		TTL-TS
TMS 27C512 JE	Tix	28-DIC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27C512 JL	Tix	28-DIC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS
TMX 27C512-20 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<200		TTL-TS
TMX 27C512-25 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<250		TTL-TS
TMX 27C512-2 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<200		TTL-TS
TMX 27C512-30 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<300		TTL-TS
TMX 27C512-3 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<300		TTL-TS
TMX 27C512-45 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<450		TTL-TS
TMX 27C512-4 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<450		TTL-TS
TMX 27C512 JL	Tix	28-DIC	CMOS	0...+70	<263	1,4	<250		TTL-TS

27512 — 65536x8-Bit EPROM

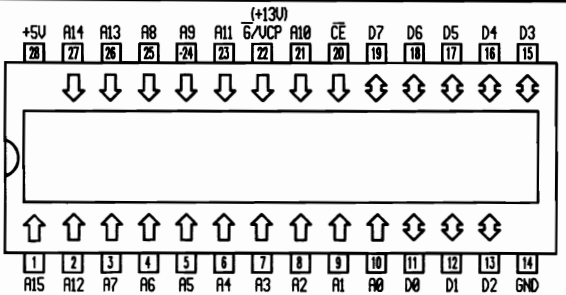


$\overline{CE}$	$\overline{G}/V_{PP}$	V_{CC}	D_n	Power	Mode
L	L	+5V	data out	active	read
X	H	+5V	Hi-Z	active	output deselect
H	X	+5V	Hi-Z	standby	standby
L	+12,5V*	+6V**	data in	active	program
H	+12,5V*	+6V**	Hi-Z	active	program inhibit
L	L	+6V*	data out	active	program verify

* Schnellprogrammierung Modus I; Schnellprogrammierung Modus II mit +12,75V.
** Schnellprogrammierung Modus I; Schnellprogrammierung Modus II mit +6,25V.
* High speed programming mode I; High speed programming mode II with +12,75V.
** High speed programming mode I; High speed programming mode II with +6,25V.

27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMM 27512 AD-17	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<170		TTL-TS
TMM 27512 AD-20	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<200		TTL-TS
TMM 27512 AD-200	Tos	28-DIP	NMOS	0...+70	<715	<220	<200		TTL-TS
TMM 27512 AD-25	Tos	28-DIP	NMOS	0...+70	<660	<192,5	<250		TTL-TS
TMM 27512 AD-250	Tos	28-DIP	NMOS	0...+70	<715	<220	<250		TTL-TS
TMM 27512 ADI-17	Tos	28-DIP	NMOS	-40...+85	<682,5	<210	<170		TTL-TS
TMM 27512 ADI-20	Tos	28-DIP	NMOS	-40...+85	<682,5	<210	<200		TTL-TS
TMM 27512 ADI-25	Tos	28-DIP	NMOS	-40...+85	<682,5	<210	<250		TTL-TS

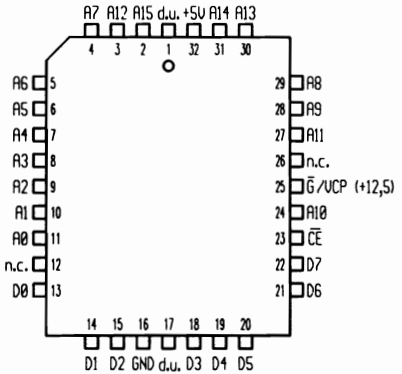
27512 — 65536x8-Bit EPROM



$\overline{CE}$	$\overline{G}/V_{pp}$	V_{cc}	D_n	Mode
L	L	+5V	data out	read
H	X	+5V	Hi-Z	standby
H⎍L	+12,5V	+6V	data in	program
L	L	+6V	data out	program verify
H	+12,5V	+6V	Hi-Z	program inhibit

27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC512-20 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC512-20 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC512-25 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC512-25 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27PC512-2 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS
TMS 27PC512-2 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC512-30 NE	Tix	28-DIP	CMOS	-40...+85	<165	<2,75	<300		TTL-TS
TMS 27PC512-30 NL	Tix	28-DIP	CMOS	0...+70	<165	<2,75	<300		TTL-TS
TMS 27PC512-3 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<300		TTL-TS
TMS 27PC512-3 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<300		TTL-TS
TMS 27PC512 NE	Tix	28-DIP	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC512 NL	Tix	28-DIP	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS

27512 — 65536x8-Bit PROM

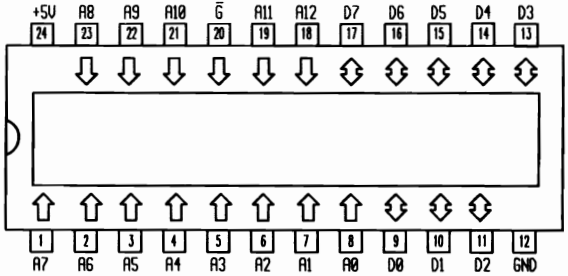


$\overline{CE}$	$\overline{G}/V_{pp}$	V_{cc}	D_n	Mode
L	L	+5V	data out	read
H	X	+5V	Hi-Z	standby
H⎍L	+12,5V	+6V	data in	program
L	L	+6V	data out	program verify
H	+12,5V	+6V	Hi-Z	program inhibit

27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC512-20 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<200		TTL-TS
TMS 27PC512-20 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<200		TTL-TS
TMS 27PC512-25 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<250		TTL-TS
TMS 27PC512-25 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<250		TTL-TS
TMS 27PC512-2 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<200		TTL-TS

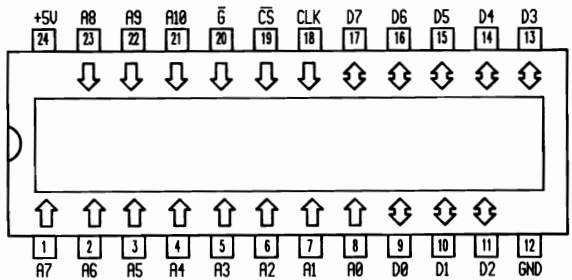
27512 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 27PC512-2 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<200		TTL-TS
TMS 27PC512-30 FME	Tix	32-PLCC	CMOS	-40...+85	<165	<2,75	<300		TTL-TS
TMS 27PC512-30 FML	Tix	32-PLCC	CMOS	0...+70	<165	<2,75	<300		TTL-TS
TMS 27PC512-3 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<300		TTL-TS
TMS 27PC512-3 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<300		TTL-TS
TMS 27PC512 FME	Tix	32-PLCC	CMOS	-40...+85	<157,5	<2,75	<250		TTL-TS
TMS 27PC512 FML	Tix	32-PLCC	CMOS	0...+70	<157,5	<2,75	<250		TTL-TS

27641 — 8192x8-Bit EPROM

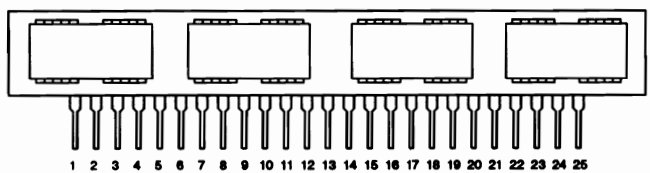


27641 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
27HC641-35 FA	Phi	24-DIC	CMOS	0...+70	<605		<35		TTL-TS
27HC641-45	Val	24-DIC	CMOS	0...+70	<550		<45		TTL-TS
27HC641-45 FA	Phi	24-DIC	CMOS	0...+70	<605		<45		TTL-TS
27HC641-55	Val	24-DIC	CMOS	0...+70	<550		<55		TTL-TS
27HC641-55 FA	Phi	24-DIC	CMOS	0...+70	<605		<55		TTL-TS

28166 — 2048x8-Bit Register PROM



41000 — 1048576x4-Bit dyn. RAM-Modul (page mode)

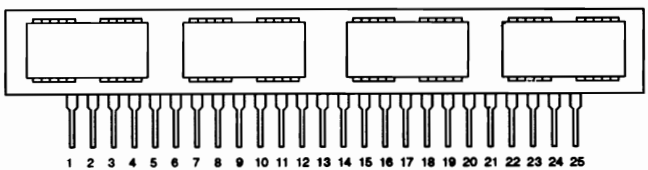


1 = GND	8 = $\overline{CAS}$	15 = A1	22 = $\overline{RAS}$
2 = T	9 = A7	16 = A3	23 = Din3
3 = A9	10 = A5	17 = A6	24 = Dout3
4 = A8	11 = A4	18 = Dout2	25 = GND
5 = +5V	12 = Din1	19 = Din2	
6 = Din0	13 = Dout1	20 = A2	
7 = Dout0	14 = $\overline{W}$	21 = A0	

28166 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TBP 28R166 J	Tix	24-DIC	TTL	0...+70	<735		20		TTL-TS
TBP 28R166 MJ	Tix	24-DIC	TTL	-55...+125	<770		20		TTL-TS
TBP 28R166 N	Tix	24-DIP	TTL	0...+70	<735		20		TTL-TS

41000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 41000 L-10	Tos	25-SIP	CMOS	0...+70	<1320	<22	<100	<8	TTL-TS
THM 41000 L-12	Tos	25-SIP	CMOS	0...+70	<1100	<22	<120	<8	TTL-TS

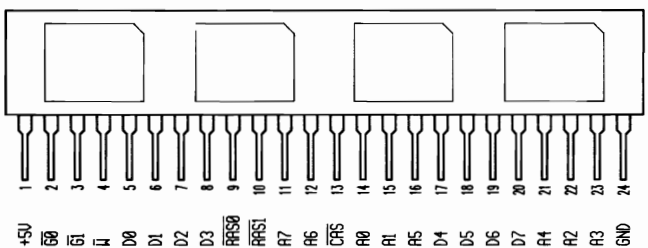
41001 — 1048576x4-Bit dyn. RAM-Modul (nibble m.)



1 = GND	8 = $\overline{CAS}$	15 = A1	22 = $\overline{RAS}$
2 = T	9 = A7	16 = A3	23 = Din3
3 = A9	10 = A5	17 = A6	24 = Dout3
4 = A8	11 = A4	18 = Dout2	25 = GND
5 = +5V	12 = Din1	19 = Din2	
6 = Din0	13 = Dout1	20 = A2	
7 = Dout0	14 = $\overline{W}$	21 = A0	

41001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 41001 L-10	Tos	25-SIP	CMOS	0...+70	<1320	<22	<100	<8	TTL-TS
THM 41001 L-12	Tos	25-SIP	CMOS	0...+70	<1100	<22	<120	<8	TTL-TS

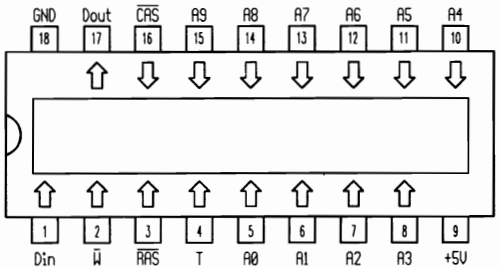
41002 — 1048576x4-Bit dyn. RAM-Modul (static c.)



41002 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
THM 41002 L-10	Tos	25-SIP	CMOS	0...+70	<1320	<22	<100	<8	TTL-TS
THM 41002 L-12	Tos	25-SIP	CMOS	0...+70	<1100	<22	<120	<8	TTL-TS

41024

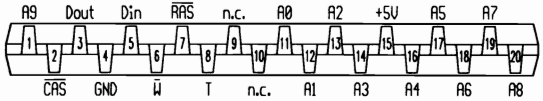
1048576x1-Bit dynam. RAM (page mode)



41024 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 511000-10	Sie	18-DIP	CMOS	0...+70	<330	<5,5	<55	<8	TTL-TS
HYB 511000-12	Sie	18-DIP	CMOS	0...+70	<275	<5,5	<70	<8	TTL-TS
HYB 511000-85	Sie	18-DIP	CMOS	0...+70	<385	<5,5	<50	<8	TTL-TS
HYB 511000 B-60	Sie	18-DIP	CMOS	0...+70	<495	<11	<60	<8	TTL-TS
HYB 511000 B-70	Sie	18-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
HYB 511000 B-80	Sie	18-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
HYB 511000 BL-60	Sie	18-DIP	CMOS	0...+70	<495	<5,5	<60	<64	TTL-TS
HYB 511000 BL-70	Sie	18-DIP	CMOS	0...+70	<440	<5,5	<70	<64	TTL-TS

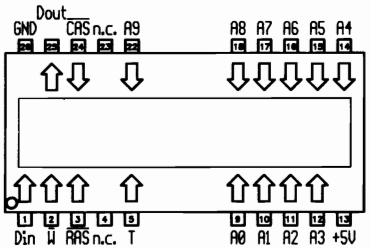
41024 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41C1000 P-10	Sam	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
MCM 511000 P-10	Mot	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
MCM 511000 P-12	Mot	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511000 P-85	Mot	18-DIP	CMOS	0...+70	<385	<11	<85	<8	TTL-TS
SMJ 4C1024-12 JDS	Tix	18-TDIC	CMOS	-55...+125			<120	<8	TTL-TS
SMJ 4C1024-15 JDS	Tix	18-TDIC	CMOS	-55...+125			<150	<8	TTL-TS
TMS 4C1024-10 NL	Tix	18-DIP	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 4C1024-12 NL	Tix	18-DIP	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 4C1024-15 NL	Tix	18-DIP	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 4C1024-10 NL	Tix	18-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1024-12 NL	Tix	18-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1024-15 NL	Tix	18-TDIP	CMOS	0...+70			<150	<8	TTL-TS

41024 — 1048576x1-Bit dynamic RAM



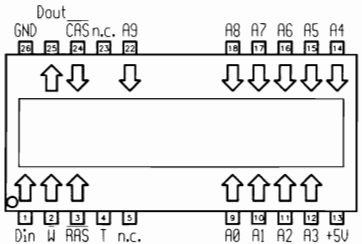
41024 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 511000 BZ-60	Sie	20-ZIP	CMOS	0...+70	<495	<11	<60	<8	TTL-TS
HYB 511000 BZ-70	Sie	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
HYB 511000 BZ-80	Sie	20-ZIP	CMOS	0...+70	<395	<11	<80	<8	TTL-TS
HYB 511000 BZL-60	Sie	20-ZIP	CMOS	0...+70	<495	<5,5	<60	<64	TTL-TS
HYB 511000 BZL-70	Sie	20-ZIP	CMOS	0...+70	<440	<5,5	<70	<64	TTL-TS
KM 41C1000 Z-10	Sam	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1000 Z-12	Sam	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS

41024 — 1048576x1-Bit dynam. RAM (page mode)



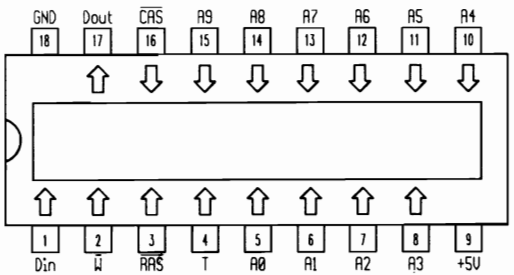
41024 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SMJ 4C1024-12 HJS	Tix	26-FLAT	CMOS	-55...+125			<120	<8	TTL-TS
SMJ 4C1024-15 HJS	Tix	26-FLAT	CMOS	-55...+125			<150	<8	TTL-TS
TMS 4C1024-10 DJL	Tix	26-FLAT	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 4C1024-12 DJL	Tix	26-FLAT	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 4C1024-15 DJL	Tix	26-FLAT	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 4C1024-10 DJL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1024-12 DJL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1024-15 DJL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

41024 — 1048576x1-Bit dynamic RAM



41024 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 511000 BJ-60	Sie	26-FLAT	CMOS	0...+70	<495	<11	<60	<8	TTL-TS
HYB 511000 BJ-70	Sie	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
HYB 511000 BJ-80	Sie	26-FLAT	CMOS	0...+70	<395	<11	<80	<8	TTL-TS
HYB 511000 BJL-60	Sie	26-FLAT	CMOS	0...+70	<495	<5,5	<60	<64	TTL-TS
HYB 511000 BJL-70	Sie	26-FLAT	CMOS	0...+70	<440	<5,5	<70	<64	TTL-TS
HYB 511000J-10	Sie	26-FLAT	CMOS	0...+70	<330	<5,5	<55	<8	TTL-TS
HYB 511000J-12	Sie	26-FLAT	CMOS	0...+70	<275	<5,5	<70	<8	TTL-TS
HYB 511000J-85	Sie	26-FLAT	CMOS	0...+70	<385	<5,5	<55	<8	TTL-TS
KM 41C1000 J-10	Sam	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1000 J-12	Sam	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511000 J-10	Mot	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
MCM 511000 J-12	Mot	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511000 J-85	Mot	26-FLAT	CMOS	0...+70	<385	<11	<85	<8	TTL-TS

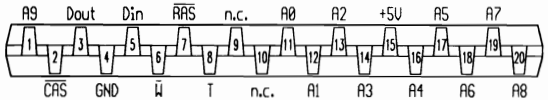
41025 — 1048576x1-Bit dynam. RAM (nibble mode)



41025 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41C1001 P-10	Sam	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1001 P-12	Sam	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511001 P-10	Mot	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
MCM 511001 P-12	Mot	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511001 P-85	Mot	18-DIP	CMOS	0...+70	<385	<11	<85	<8	TTL-TS
TMS 4C1025-10 NL	Tix	18-DIP	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 4C1025-12 NL	Tix	18-DIP	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 4C1025-15 NL	Tix	18-DIP	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS

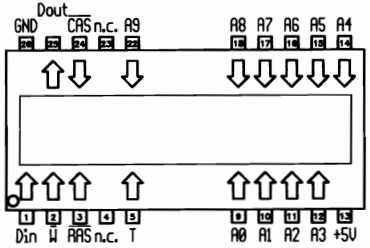
41025 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 4C1025-10 NL	Tix	18-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1025-12 NL	Tix	18-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1025-15 NL	Tix	18-TDIP	CMOS	0...+70			<150	<8	TTL-TS

41025 — 1048576x1-Bit dynam. RAM (nibble mode)



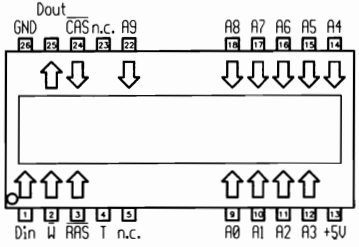
41025 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41C1001 Z-10	Sam	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1001 Z-12	Sam	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS

41025 — 1048576x1-Bit dynam. RAM (nibble mode)



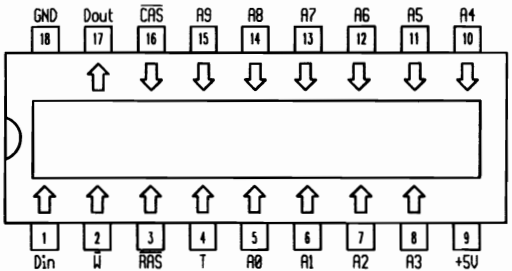
41025 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4C1025-10 DJL	Tix	26-FLAT	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 4C1025-12 DJL	Tix	26-FLAT	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 4C1025-15 DJL	Tix	26-FLAT	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 4C1025-10 DJL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1025-12 DJL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1025-15 DJL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

41025 — 1048576x1-Bit dynam. RAM (nibble mode)



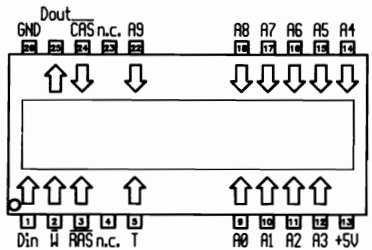
41025 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41C1001 J-10	Sam	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1001 J-12	Sam	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511001 J-10	Mot	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
MCM 511001 J-12	Mot	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511001 J-85	Mot	26-FLAT	CMOS	0...+70	<385	<11	<85	<8	TTL-TS

41026 — 1048576x1-Bit dynamic RAM



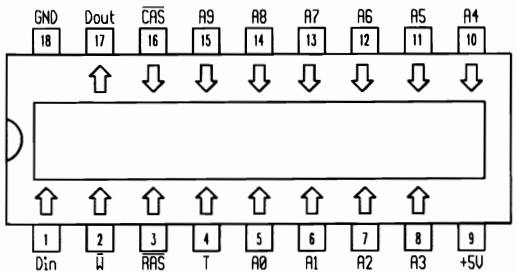
41026 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 4C1026-10 NL	Tix	18-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1026-12 NL	Tix	18-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1026-15 NL	Tix	18-TDIP	CMOS	0...+70			<150	<8	TTL-TS

41026 — 1048576x1-Bit dynamic RAM



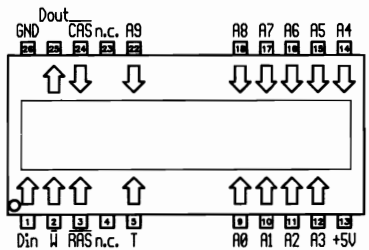
41026 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 4C1026-10 DJL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1026-12 DJL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1026-15 DJL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

41027 — 1048576x1-Bit dynam. RAM (static column)



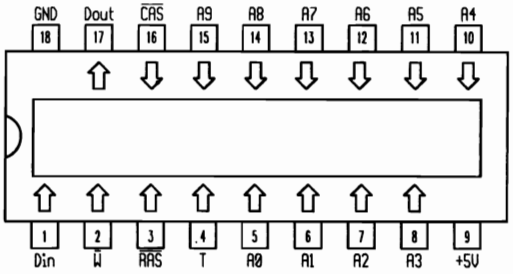
41027 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4C1027-10 NL	Tix	18-DIP	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 4C1027-12 NL	Tix	18-DIP	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 4C1027-15 NL	Tix	18-DIP	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 4C1027-10 NL	Tix	18-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1027-12 NL	Tix	18-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1027-15 NL	Tix	18-TDIP	CMOS	0...+70			<150	<8	TTL-TS

41027 — 1048576x1-Bit dynam. RAM (static column)



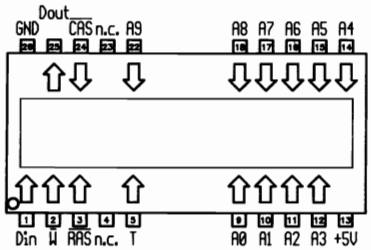
41027 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4C1027-10 DJL	Tix	26-FLAT	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 4C1027-12 DJL	Tix	26-FLAT	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 4C1027-15 DJL	Tix	26-FLAT	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 4C1027-10 DJL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1027-12 DJL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1027-15 DJL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

41029 — 1048576x1-Bit dynamic RAM



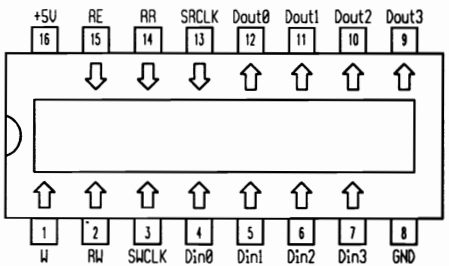
41029 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 4C1029-10 NL	Tix	18-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1029-12 NL	Tix	18-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1029-15 NL	Tix	18-TDIP	CMOS	0...+70			<150	<8	TTL-TS

41029 — 1048576x1-Bit dynamic RAM



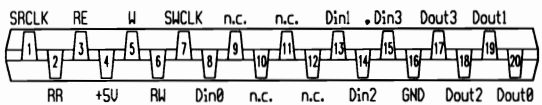
41029 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 4C1029-10 DJL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 4C1029-12 DJL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 4C1029-15 DJL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

41050 — 262144x4-Bit FIFO (pseudo static)



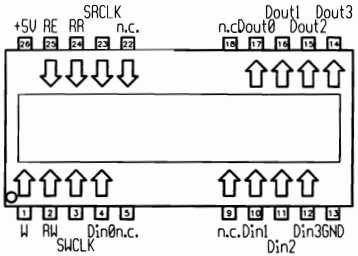
41050 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4C1050-3 NL	Tix	16-DIP	CMOS	0...+70	<275	<38,5	<30		TTL
TMS 4C1050-4 NL	Tix	16-DIP	CMOS	0...+70	<247,5	<38,5	<40		TTL
TMS 4C1050-6 NL	Tix	16-DIP	CMOS	0...+70	<192,5	<38,5	<60		TTL

41050 — 262144x4-Bit FIFO (pseudo static)

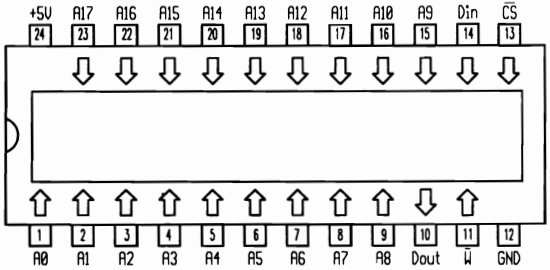


41050 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4C1050-3 SDL	Tix	20-ZIP	CMOS	0...+70	<275	<38,5	<30		TTL
TMS 4C1050-4 SDL	Tix	20-ZIP	CMOS	0...+70	<247,5	<38,5	<40		TTL
TMS 4C1050-6 SDL	Tix	20-ZIP	CMOS	0...+70	<192,5	<38,5	<60		TTL

41050 — 262144x4-Bit FIFO (pseudo static)



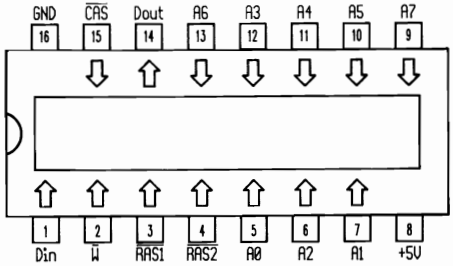
41100 — 910 wordsx8-Bit FIFO



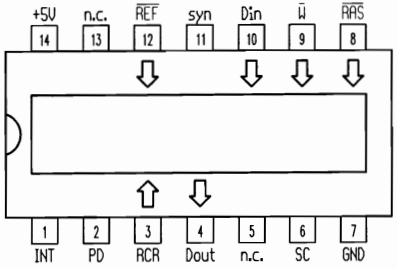
41050 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 4C1050-3 DJL	Tix	26-FLAT	CMOS	0...+70	<275	<38,5	<30		TTL
TMS 4C1050-4 DJL	Tix	26-FLAT	CMOS	0...+70	<247,5	<38,5	<40		TTL
TMS 4C1050-6 DJL	Tix	26-FLAT	CMOS	0...+70	<192,5	<38,5	<60		TTL

41100 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 41101 C-1	Nec	24-DIP	NMOS	-20...+70	<495		<69		TTL-TS
µPD 41101 C-2	Nec	24-DIP	NMOS	-20...+70	<495		<34		TTL-TS
µPD 41101 C-3	Nec	24-DIP	NMOS	-20...+70	<495		<34		TTL-TS
µPD 41102 C-1	Nec	24-DIP	NMOS	-20...+70	<495		<56		TTL-TS
µPD 41102 C-2	Nec	24-DIP	NMOS	-20...+70	<495		<28		TTL-TS
µPD 41102 C-3	Nec	24-DIP	NMOS	-20...+70	<495		<28		TTL-TS
µPD 42505 C-50	Nec	24-DIP	CMOS	0...+70	<660		<50		TTL-TS
µPD 42505 C-75	Nec	24-DIP	CMOS	0...+70	<660		<75		TTL-TS

41128 — 2 x 65536x1-Bit dynamic RAM



41200 — 320 row x 700 column serial vRAM

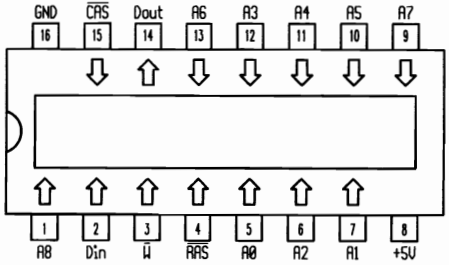


41128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 41128 B	Tix	16-DIP x 2	NMOS	0...+70	<357	<55	<150	<4	TTL-TS

41200 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 41221 C-70	Nec	14-DIP	CMOS	-10...+70	<247.5	82.5	<70	2	TTL-TS
µPD 41221 C-90	Nec	14-DIP	CMOS	-10...+70	<247.5	82.5	<90	2	TTL-TS

41256

262144 x 1-Bit dynam RAM (page mode)



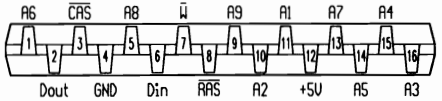
41256 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
HM 50256 P-12	Hit	16-DIP	NMOS	0...+70	<456,5	<24,75	<120	<4	TTL-TS
HM 50256 P-15	Hit	16-DIP	NMOS	0...+70	<385	<24,75	<150	<4	TTL-TS
HM 50256 P-20	Hit	16-DIP	NMOS	0...+70	<302,5	<24,75	<200	<4	TTL-TS
HM 51256 LP-10	Hit	16-DIP	CMOS	0...+70	<330	<33	<100	<4	TTL-TS
HM 51256 LP-12	Hit	16-DIP	CMOS	0...+70	<275	<33	<120	<4	TTL-TS
HM 51256 LP-15	Hit	16-DIP	CMOS	0...+70	<220	<33	<150	<4	TTL-TS
HM 51256 P-10	Hit	16-DIP	CMOS	0...+70	<330	<33	<100	<4	TTL-TS
HM 51256 P-12	Hit	16-DIP	CMOS	0...+70	<275	<33	<120	<4	TTL-TS

41256 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
HM 51256 P-15	Hit	16-DIP	CMOS	0...+70	<220	<33	<150	<4	TTL-TS
HYB 41256-10	Sie	16-DIP	NMOS	0...+70	<358	<28	<100	<4	TTL-TS
HYB 41256-12	Sie	16-DIP	NMOS	0...+70	<358	<28	<120	<4	TTL-TS
HYB 41256-15	Sie	16-DIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
KM 41256 AP-10	Sam	16-DIP	NMOS	0...+70	<467,5	<24,75	<100	<4	TTL-TS
KM 41256 AP-12	Sam	16-DIP	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41256 AP-15	Sam	16-DIP	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS
M5M 4256 AP-10	Mit	16-DIP	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4256 AP-12	Mit	16-DIP	NMOS	0...+70	<330	<25	<120	<4	TTL-TS
M5M 4256 AP-15	Mit	16-DIP	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4256 AP-85	Mit	16-DIP	NMOS	0...+70	<385	<25	<85	<4	TTL-TS
MCM 6256 BP-10	Mot	16-DIP	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
MCM 6256 BP-12	Mot	16-DIP	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
MCM 6256 BP-15	Mot	16-DIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
MKB 45F56 P-80	Tho	16-DIP	NMOS	-55...+110	<385	<27,5	<100	<4	TTL-TS
MKB 45F56 P-81	Tho	16-DIP	NMOS	-55...+110	<385	<27,5	<120	<4	TTL-TS
MKB 45F56 P-82	Tho	16-DIP	NMOS	-55...+110	<385	<27,5	<150	<4	TTL-TS
MN 41256 A-08	Mat	16-DIP	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41256 A-10	Mat	16-DIP	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41256 A-12	Mat	16-DIP	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
SMJ 4256-12 JD	Tix	16-DIC	NMOS	-55...+110	<440	<27,5	<120	<4	TTL-TS
SMJ 4256-15 JD	Tix	16-DIC	NMOS	-55...+110	<412,5	<27,5	<150	<4	TTL-TS
SMJ 4256-20 JD	Tix	16-DIC	NMOS	-55...+110	<330	<27,5	<200	<4	TTL-TS
TMM 41256 AP-10	Tos	16-DIP	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41256 AP-12	Tos	16-DIP	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
TMM 41256 AP-15	Tos	16-DIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
TMS 4256-10 NE	Tix	16-DIP	NMOS	-40...+85	<385	<24,75	<100	<4	TTL-TS
TMS 4256-10 NL	Tix	16-DIP	NMOS	0...+70	<385	<24,75	<100	<4	TTL-TS
TMS 4256-10 NS	Tix	16-DIP	NMOS	-55...+100	<385	<24,75	<100	<4	TTL-TS
TMS 4256-12 NE	Tix	16-DIP	NMOS	-40...+85	<385	<24,75	<120	<4	TTL-TS
TMS 4256-12 NL	Tix	16-DIP	NMOS	0...+70	<429	<25,75	<120	<4	TTL-TS
TMS 4256-12 NS	Tix	16-DIP	NMOS	-55...+100	<385	<24,75	<120	<4	TTL-TS
TMS 4256-15 NE	Tix	16-DIP	NMOS	-40...+85	<385	<24,75	<150	<4	TTL-TS
TMS 4256-15 NL	Tix	16-DIP	NMOS	0...+70	<374	<25,75	<150	<4	TTL-TS
TMS 4256-15 NS	Tix	16-DIP	NMOS	-55...+100	<385	<24,75	<150	<4	TTL-TS
TMS 4256-20 NL	Tix	16-DIP	NMOS	0...+70	<319	<25,75	<200	<4	TTL-TS
TMS 4256-8 NE	Tix	16-DIP	NMOS	-40...+85	<385	<24,75	<80	<4	TTL-TS

41256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
TMS 4256-8 NL	Tix	16-DIP	NMOS	0...+70	<385	<24,75	<80	<4	TTL-TS
TMS 4256-8 NS	Tix	16-DIP	NMOS	-55...+100	<385	<24,75	<80	<4	TTL-TS
µPD 41256 C-10	Nec	16-DIC	NMOS	0...+70	<457	28	<100	<4	TTL-TS
µPD 41256 C-12	Nec	16-DIC	NMOS	0...+70	<457	28	<120	<4	TTL-TS
µPD 41256 C-15	Nec	16-DIC	NMOS	0...+70	<385	28	<150	<4	TTL-TS
µPD 41256 D-10	Nec	16-DIP	NMOS	0...+70	<457	28	<100	<4	TTL-TS
µPD 41256 D-12	Nec	16-DIP	NMOS	0...+70	<457	28	<120	<4	TTL-TS
µPD 41256 D-15	Nec	16-DIP	NMOS	0...+70	<385	28	<150	<4	TTL-TS

41256

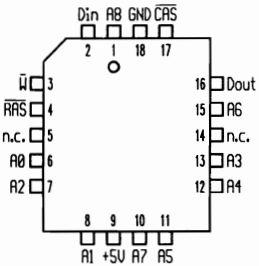
262144x1-Bit dynamic RAM



41256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 50256 ZP-12	Hit	16-ZIP	NMOS	0...+70	<456,5	<24,75	<120	<4	TTL-TS
HM 50256 ZP-15	Hit	16-ZIP	NMOS	0...+70	<385	<24,75	<150	<4	TTL-TS
HM 50256 ZP-20	Hit	16-ZIP	NMOS	0...+70	<302,5	<24,75	<200	<4	TTL-TS
KM 41256 AZ-10	Sam	16-ZIP	NMOS	0...+70	<467,5	<24,75	<100	<4	TTL-TS
KM 41256 AZ-12	Sam	16-ZIP	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41256 AZ-15	Sam	16-ZIP	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS
M5M 4256 AJ-10	Mit	16-ZIP	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4256 AJ-12	Mit	16-ZIP	NMOS	0...+70	<330	<25	<120	<4	TTL-TS

41256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 4256 AJ-15	Mit	16-ZIP	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4256 AJ-85	Mit	16-ZIP	NMOS	0...+70	<385	<25	<85	<4	TTL-TS
MN 41256 AL-08	Mat	16-ZIP	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41256 AL-10	Mat	16-ZIP	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41256 AL-12	Mat	16-ZIP	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
TMM 41256 AZ-10	Tos	16-ZIP	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41256 AZ-12	Tos	16-ZIP	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
TMM 41256 AZ-15	Tos	16-ZIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
TMS 4256-10 SDE	Tix	16-ZIP	NMOS	-40...+85	<385	<24,75	<100	<4	TTL-TS
TMS 4256-10 SDL	Tix	16-ZIP	NMOS	0...+70	<385	<24,75	<100	<4	TTL-TS
TMS 4256-10 SDS	Tix	16-ZIP	NMOS	-55...+100	<385	<24,75	<100	<4	TTL-TS
TMS 4256-12 SDE	Tix	16-ZIP	NMOS	-40...+85	<385	<24,75	<120	<4	TTL-TS
TMS 4256-12 SDL	Tix	16-ZIP	NMOS	0...+70	<385	<24,75	<120	<4	TTL-TS
TMS 4256-12 SDS	Tix	16-ZIP	NMOS	-55...+100	<385	<24,75	<120	<4	TTL-TS
TMS 4256-15 SDE	Tix	16-ZIP	NMOS	-40...+85	<385	<24,75	<150	<4	TTL-TS
TMS 4256-15 SDL	Tix	16-ZIP	NMOS	0...+70	<385	<24,75	<150	<4	TTL-TS
TMS 4256-15 SDS	Tix	16-ZIP	NMOS	-55...+100	<385	<24,75	<150	<4	TTL-TS
TMS 4256-8 SDE	Tix	16-ZIP	NMOS	-40...+85	<385	<24,75	<80	<4	TTL-TS
TMS 4256-8 SDL	Tix	16-ZIP	NMOS	0...+70	<385	<24,75	<80	<4	TTL-TS
TMS 4256-8 SDS	Tix	16-ZIP	NMOS	-55...+100	<385	<24,75	<80	<4	TTL-TS
µPD 41256 V-10	Nec	16-ZIP	NMOS	0...+70	<457	28	<100	<4	TTL-TS
µPD 41256 V-12	Nec	16-ZIP	NMOS	0...+70	<457	28	<120	<4	TTL-TS

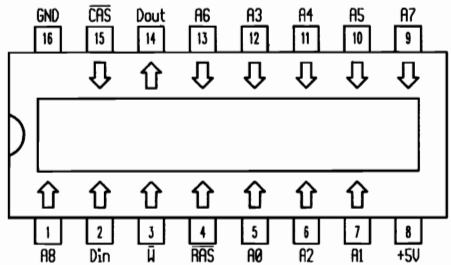
41256 — 262144x1-Bit dynamic RAM



41256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 50256 CP-12	Hit	18-PLCC	NMOS	0...+70	<456,5	<24,75	<120	<4	TTL-TS
HM 50256 CP-15	Hit	18-PLCC	NMOS	0...+70	<385	<24,75	<150	<4	TTL-TS
HM 50256 CP-20	Hit	18-PLCC	NMOS	0...+70	<302,5	<24,75	<200	<4	TTL-TS
HM 51256 CP-10	Hit	18-PLCC	CMOS	0...+70	<330	<33	<100	<4	TTL-TS
HM 51256 CP-12	Hit	18-PLCC	CMOS	0...+70	<275	<33	<120	<4	TTL-TS
HM 51256 CP-15	Hit	18-PLCC	CMOS	0...+70	<220	<33	<150	<4	TTL-TS
HM 51256 LCP-10	Hit	18-PLCC	CMOS	0...+70	<330	<33	<100	<4	TTL-TS
HM 51256 LCP-12	Hit	18-PLCC	CMOS	0...+70	<275	<33	<120	<4	TTL-TS

41256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 51256 LCP-15	Hit	18-PLCC	CMOS	0...+70	<220	<33	<150	<4	TTL-TS
KM 41256 AJ-10	Sam	18-PLCC	NMOS	0...+70	<467,5	<24,75	<100	<4	TTL-TS
KM 41256 AJ-12	Sam	18-PLCC	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41256 AJ-15	Sam	18-PLCC	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS
M5M 4256 AL-10	Mit	18-PLCC	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4256 AL-12	Mit	18-PLCC	NMOS	0...+70	<330	<25	<120	<4	TTL-TS
M5M 4256 AL-15	Mit	18-PLCC	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4256 AL-85	Mit	18-PLCC	NMOS	0...+70	<385	<25	<85	<4	TTL-TS
MKB 45F56 E-80	Tho	18-LCC	NMOS	-55...+110	<385	<27,5	<100	<4	TTL-TS
MKB 45F56 E-81	Tho	18-LCC	NMOS	-55...+110	<385	<27,5	<120	<4	TTL-TS
MKB 45F56 E-82	Tho	18-LCC	NMOS	-55...+110	<385	<27,5	<150	<4	TTL-TS
MN 41256 AJ-08	Mat	18-PLCC	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41256 AJ-10	Mat	18-PLCC	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41256 AJ-12	Mat	18-PLCC	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
SMJ 4256-12 FV	Tix	18-LCC	NMOS	-55...+110	<440	<27,5	<120	<4	TTL-TS
SMJ 4256-15 FV	Tix	18-LCC	NMOS	-55...+110	<412,5	<27,5	<150	<4	TTL-TS
SMJ 4256-20 FV	Tix	18-LCC	NMOS	-55...+110	<330	<27,5	<200	<4	TTL-TS
TMM 41256 AT-10	Tos	18-PLCC	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41256 AT-12	Tos	18-PLCC	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
TMM 41256 AT-15	Tos	18-PLCC	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
TMS 4256-10 FME	Tix	18-PLCC	NMOS	-40...+85	<385	<24,75	<100	<4	TTL-TS
TMS 4256-10 FML	Tix	18-PLCC	NMOS	0...+70	<385	<24,75	<100	<4	TTL-TS
TMS 4256-10 FMS	Tix	18-PLCC	NMOS	-55...+100	<385	<24,75	<100	<4	TTL-TS
TMS 4256-12 FME	Tix	18-PLCC	NMOS	-40...+85	<385	<24,75	<120	<4	TTL-TS
TMS 4256-12 FML	Tix	18-PLCC	NMOS	0...+70	<429	<25,75	<120	<4	TTL-TS
TMS 4256-12 FMS	Tix	18-PLCC	NMOS	-55...+100	<385	<24,75	<120	<4	TTL-TS
TMS 4256-15 FME	Tix	18-PLCC	NMOS	-40...+85	<385	<24,75	<150	<4	TTL-TS
TMS 4256-15 FML	Tix	18-PLCC	NMOS	0...+70	<374	<25,75	<150	<4	TTL-TS
TMS 4256-15 FMS	Tix	18-PLCC	NMOS	-55...+100	<385	<24,75	<150	<4	TTL-TS
TMS 4256-20 FML	Tix	18-PLCC	NMOS	0...+70	<319	<25,75	<200	<4	TTL-TS
TMS 4256-8 FME	Tix	18-PLCC	NMOS	-40...+85	<385	<24,75	<80	<4	TTL-TS
TMS 4256-8 FML	Tix	18-PLCC	NMOS	0...+70	<385	<24,75	<80	<4	TTL-TS
TMS 4256-8 FMS	Tix	18-PLCC	NMOS	-55...+100	<385	<24,75	<80	<4	TTL-TS
µPD 41256 L-10	Nec	18-PLCC	NMOS	0...+70	<457	28	<100	<4	TTL-TS
µPD 41256 L-12	Nec	18-PLCC	NMOS	0...+70	<457	28	<120	<4	TTL-TS
µPD 41256 L-15	Nec	18-PLCC	NMOS	0...+70	<385	28	<150	<4	TTL-TS

41257 — 262144x1-Bit dynam. RAM (nibble mode)

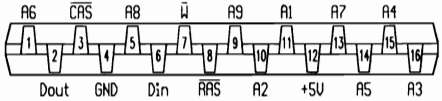


41257 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 50257 P-12	Hit	16-DIP	NMOS	0...+70	<402,5	<24,75	<120	<4	TTL-TS
HM 50257 P-15	Hit	16-DIP	NMOS	0...+70	<385	<24,75	<150	<4	TTL-TS
HM 50257 P-20	Hit	16-DIP	NMOS	0...+70	<302,5	<24,75	<200	<4	TTL-TS
KM 41257 AP-10	Sam	16-DIP	NMOS	0...+70	<467,5	<24,75	<100	<4	TTL-TS
KM 41257 AP-12	Sam	16-DIP	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41257 AP-15	Sam	16-DIP	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS
M5M 4257 AP-10	Mit	16-DIP	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4257 AP-12	Mit	16-DIP	NMOS	0...+70	<330	<25	<120	<4	TTL-TS

41257

262144x1-Bit dynam. RAM (nibble mode)

Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	$mW/bit	taa ns	tref ms	Ausgang Output Sortie Uscita Salida
M5M 4257 AP-15	Mit	16-DIP	NMOS	0...+70	<305	<25		<150	<4	TTL-TS
M5M 4257 AP-85	Mit	16-DIP	NMOS	0...+70	<385	<25		<85	<4	TTL-TS
MCM 6257 BP-10	Mot	16-DIP	NMOS	0...+70	<440	<28		<100	<4	TTL-TS
MCM 6257 BP-12	Mot	16-DIP	NMOS	0...+70	<396	<28		<120	<4	TTL-TS
MCM 6257 BP-15	Mot	16-DIP	NMOS	0...+70	<358	<28		<150	<4	TTL-TS
MN 41257 A-08	Mat	16-DIP	NMOS	0...+70	<440	<16,5		<80	<4	TTL-TS
MN 41257 A-10	Mat	16-DIP	NMOS	0...+70	<385	<16,5		<100	<4	TTL-TS
MN 41257 A-12	Mat	16-DIP	NMOS	0...+70	<358	<16,5		<120	<4	TTL-TS
NMC 41257-10 N	Nsc	16-DIP	NMOS	0...+70	<413	<22		<100	<4	TTL-TS
NMC 41257-12 N	Nsc	16-DIP	NMOS	0...+70	<413	<22		<120	<4	TTL-TS
NMC 41257-15 N	Nsc	16-DIP	NMOS	0...+70	<413	<22		<150	<4	TTL-TS
TMM 41257 AP-10	Tos	16-DIP	NMOS	0...+70	<440	<28		<100	<4	TTL-TS
TMM 41257 AP-12	Tos	16-DIP	NMOS	0...+70	<396	<28		<120	<4	TTL-TS
TMM 41257 AP-15	Tos	16-DIP	NMOS	0...+70	<358	<28		<150	<4	TTL-TS
TMS 4257-10 NE	Tix	16-DIP	NMOS	-40...+85	<385	<24,75		<100	<4	TTL-TS
TMS 4257-10 NL	Tix	16-DIP	NMOS	0...+70	<385	<24,75		<100	<4	TTL-TS
TMS 4257-10 NS	Tix	16-DIP	NMOS	-55...+100	<385	<24,75		<100	<4	TTL-TS
TMS 4257-12 NE	Tix	16-DIP	NMOS	-40...+85	<385	<24,75		<120	<4	TTL-TS
TMS 4257-12 NL	Tix	16-DIP	NMOS	0...+70	<429	<25,75		<120	<4	TTL-TS
TMS 4257-12 NS	Tix	16-DIP	NMOS	-55...+100	<385	<24,75		<120	<4	TTL-TS
TMS 4257-15 NE	Tix	16-DIP	NMOS	-40...+85	<385	≤24,75		<150	<4	TTL-TS
TMS 4257-15 NL	Tix	16-DIP	NMOS	0...+70	<374	<25,75		<150	<4	TTL-TS
TMS 4257-15 NS	Tix	16-DIP	NMOS	-55...+100	<385	<24,75		<150	<4	TTL-TS
TMS 4257-20 NL	Tix	16-DIP	NMOS	0...+70	<319	<25,75		<200	<4	TTL-TS
µPD 41257 C-10	Nec	16-DIP	NMOS	0...+70	<440	28		<100	<4	TTL-TS
µPD 41257 C-12	Nec	16-DIP	NMOS	0...+70	<412	28		<120	<4	TTL-TS
µPD 41257 C-15	Nec	16-DIP	NMOS	0...+70	<385	28		<150	<4	TTL-TS

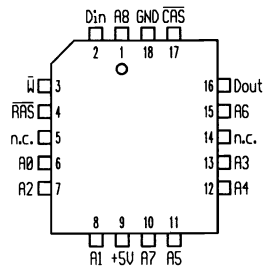


Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	$mW/bit	taa ns	tref ms	Output
HM 50257 ZP-12	Hit	16-ZIP	NMOS	0...+70	<402,5	<24,75		<120	<4	TTL-TS
HM 50257 ZP-15	Hit	16-ZIP	NMOS	0...+70	<385	<24,75		<150	<4	TTL-TS
HM 50257 ZP-20	Hit	16-ZIP	NMOS	0...+70	<302,5	<24,75		<200	<4	TTL-TS
KM 41257 AZ-10	Sam	16-ZIP	NMOS	0...+70	<467,5	<24,75		<100	<4	TTL-TS
KM 41257 AZ-12	Sam	16-ZIP	NMOS	0...+70	<412,5	<24,75		<120	<4	TTL-TS
KM 41257 AZ-15	Sam	16-ZIP	NMOS	0...+70	<357,5	<24,75		<150	<4	TTL-TS
M5M 4257 AL-10	Mit	16-ZIP	NMOS	0...+70	<360	<25		<100	<4	TTL-TS
M5M 4257 AL-12	Mit	16-ZIP	NMOS	0...+70	<330	<25		<120	<4	TTL-TS

41257 Type	Man	Case	Techn.	TU/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 4257 AL-15	Mit	16-ZIP	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4257 AL-85	Mit	16-ZIP	NMOS	0...+70	<385	<25	<85	<4	TTL-TS
MN 41257 AL-08	Mat	16-ZIP	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41257 AL-10	Mat	16-ZIP	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41257 AL-12	Mat	16-ZIP	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
TMM 41257 AZ-10	Tos	16-ZIP	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41257 AZ-12	Tos	16-ZIP	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
TMM 41257 AZ-15	Tos	16-ZIP	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
TMS 4257-10 SDE	Tix	16-ZIP	NMOS	-40...+85	<385	<24,75	<100	<4	TTL-TS
TMS 4257-10 SDL	Tix	16-ZIP	NMOS	0...+70	<385	<24,75	<100	<4	TTL-TS
TMS 4257-10 SDS	Tix	16-ZIP	NMOS	-55...+100	<385	<24,75	<100	<4	TTL-TS
TMS 4257-12 SDE	Tix	16-ZIP	NMOS	-40...+85	<385	<24,75	<120	<4	TTL-TS
TMS 4257-12 SDL	Tix	16-ZIP	NMOS	0...+70	<385	<24,75	<120	<4	TTL-TS
TMS 4257-12 SDS	Tix	16-ZIP	NMOS	-55...+100	<385	<24,75	<120	<4	TTL-TS
TMS 4257-15 SDE	Tix	16-ZIP	NMOS	-40...+85	<385	<24,75	<150	<4	TTL-TS
TMS 4257-15 SDL	Tix	16-ZIP	NMOS	0...+70	<385	<24,75	<150	<4	TTL-TS
TMS 4257-15 SDS	Tix	16-ZIP	NMOS	-55...+100	<385	<24,75	<150	<4	TTL-TS

41257

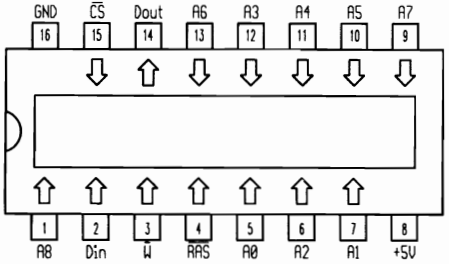
262144x1-Bit dynam. RAM (nibble mode)



41257 Type	Man	Case	Techn.	TU/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 50257 CP-12	Hit	18-PLCC	NMOS	0...+70	<402,5	<24,75	<120	<4	TTL-TS
HM 50257 CP-15	Hit	18-PLCC	NMOS	0...+70	<385	<24,75	<150	<4	TTL-TS
HM 50257 CP-20	Hit	18-PLCC	NMOS	0...+70	<302,5	<24,75	<200	<4	TTL-TS
KM 41257 AJ-10	Sam	18-PLCC	NMOS	0...+70	<467,5	<24,75	<100	<4	TTL-TS
KM 41257 AJ-12	Sam	18-PLCC	NMOS	0...+70	<412,5	<24,75	<120	<4	TTL-TS
KM 41257 AJ-15	Sam	18-PLCC	NMOS	0...+70	<357,5	<24,75	<150	<4	TTL-TS
M5M 4257 AJ-10	Mit	18-PLCC	NMOS	0...+70	<360	<25	<100	<4	TTL-TS
M5M 4257 AJ-12	Mit	18-PLCC	NMOS	0...+70	<330	<25	<120	<4	TTL-TS

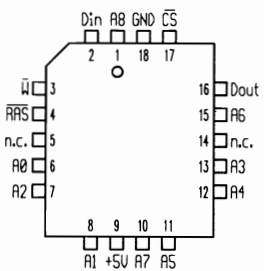
41257 Type	Man	Case	Techn.	T_{Uj}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 4257 AJ-15	Mit	18-PLCC	NMOS	0...+70	<305	<25	<150	<4	TTL-TS
M5M 4257 AJ-85	Mit	18-PLCC	NMOS	0...+70	<385	<25	<85	<4	TTL-TS
MN 41257 AJ-08	Mat	18-PLCC	NMOS	0...+70	<440	<16,5	<80	<4	TTL-TS
MN 41257 AJ-10	Mat	18-PLCC	NMOS	0...+70	<385	<16,5	<100	<4	TTL-TS
MN 41257 AJ-12	Mat	18-PLCC	NMOS	0...+70	<358	<16,5	<120	<4	TTL-TS
TMM 41257 AT-10	Tos	18-PLCC	NMOS	0...+70	<440	<28	<100	<4	TTL-TS
TMM 41257 AT-12	Tos	18-PLCC	NMOS	0...+70	<396	<28	<120	<4	TTL-TS
TMM 41257 AT-15	Tos	18-PLCC	NMOS	0...+70	<358	<28	<150	<4	TTL-TS
TMS 4257-10 FME	Tix	18-PLCC	NMOS	-40...+85	<385	<24,75	<100	<4	TTL-TS
TMS 4257-10 FML	Tix	18-PLCC	NMOS	0...+70	<385	<24,75	<100	<4	TTL-TS
TMS 4257-10 FMS	Tix	18-PLCC	NMOS	-55...+100	<385	<24,75	<100	<4	TTL-TS
TMS 4257-12 FME	Tix	18-PLCC	NMOS	-40...+85	<385	<24,75	<120	<4	TTL-TS
TMS 4257-12 FML	Tix	18-PLCC	NMOS	0...+70	<429	<25,75	<120	<4	TTL-TS
TMS 4257-12 FMS	Tix	18-PLCC	NMOS	-55...+100	<385	<24,75	<120	<4	TTL-TS
TMS 4257-15 FME	Tix	18-PLCC	NMOS	-40...+85	<385	<24,75	<150	<4	TTL-TS
TMS 4257-15 FML	Tix	18-PLCC	NMOS	0...+70	<374	<25,75	<150	<4	TTL-TS
TMS 4257-15 FMS	Tix	18-PLCC	NMOS	-55...+100	<385	<24,75	<150	<4	TTL-TS
TMS 4257-20 FML	Tix	18-PLCC	NMOS	0...+70	<319	<25,75	<200	<4	TTL-TS
µPD 41257 L-10	Nec	18-PLCC	NMOS	0...+70	<440	28	<100	<4	TTL-TS
µPD 41257 L-12	Nec	18-PLCC	NMOS	0...+70	<412	28	<120	<4	TTL-TS
µPD 41257 L-15	Nec	18-PLCC	NMOS	0...+70	<385	28	<150	<4	TTL-TS

41258 — 262144x1-Bit dynamic RAM

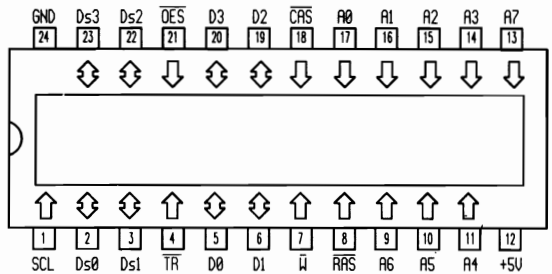


41258 Type	Man	Case	Techn.	T_{Uj}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 51258 P-10	Hit	16-DIP	CMOS	0...+70	<330	<33	<100	<4	TTL-TS
HM 51258 P-12	Hit	16-DIP	CMOS	0...+70	<275	<33	<120	<4	TTL-TS
HM 51258 P-15	Hit	16-DIP	CMOS	0...+70	<220	<33	<150	<4	TTL-TS
HM 51258 P-8	Hit	16-DIP	CMOS	0...+70	<385	<33	<85	<4	TTL-TS

41258 — 262144x1-Bit dynamic RAM



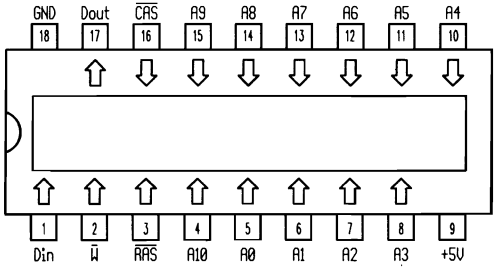
41264 — 262144x1-Bit DUALPORT dynamic vRAM



41258 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 51258 CP-10	Hit	18-PLCC	CMOS	0...+70	<330	<33	<100	<4	TTL-TS
HM 51258 CP-12	Hit	18-PLCC	CMOS	0...+70	<275	<33	<120	<4	TTL-TS
HM 51258 CP-15	Hit	18-PLCC	CMOS	0...+70	<220	<33	<150	<4	TTL-TS
HM 51258 CP-8	Hit	18-PLCC	CMOS	0...+70	<385	<33	<85	<4	TTL-TS

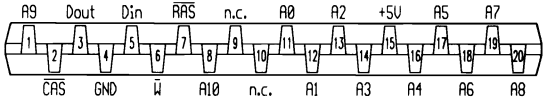
41264 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 41264 C-12	Nec	24-DIP	NMOS	0...+70	<522.5	66	<120	4	TTL-TS
µPD 41264 C-15	Nec	24-DIP	NMOS	0...+70	<467.5	66	<150	4	TTL-TS

44100 — 4194304x1-Bit dynamic RAM (page mode)



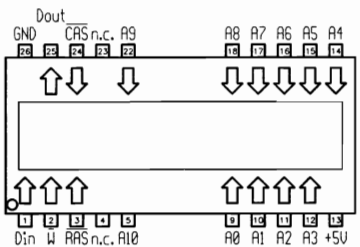
44100 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 41C4000-08	Mat	18-DIP	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C4000-10	Mat	18-DIP	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44100 — 4194304x1-Bit dynam RAM (page mode)



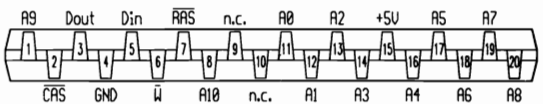
44100 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44100 L-10	Mit	20-ZIP	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44100 L-8	Mit	20-ZIP	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS
MN 41C4000 L-08	Mat	20-ZIP	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C4000 L-10	Mat	20-ZIP	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44100 — 4194304x1-Bit dynam RAM (page mode)



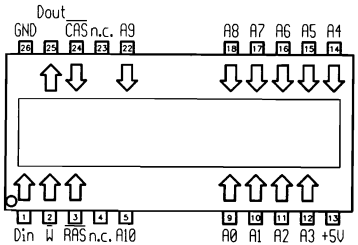
44100 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 514100 J-10	Sie	26-FLAT	CMOS	0...+70	<440	<11	<100	<16	TTL-TS
HYB 514100 J-80	Sie	26-FLAT	CMOS	0...+70	<495	<11	<80	<16	TTL-TS
M5M 44100 J-10	Mit	26-FLAT	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44100 J-8	Mit	26-FLAT	CMOS	0...+70	<552,5	<5,5	<80	<16	TTL-TS
MN 41C4000 SJ-08	Mat	26-FLAT	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C4000 SJ-10	Mat	26-FLAT	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44101 — 4194304x1-Bit dynam RAM (page mode)



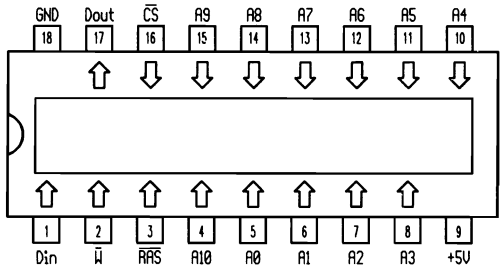
44101 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44101 L-10	Mit	20-ZIP	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44101 L-8	Mit	20-ZIP	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS

44101 — 4194304x1-Bit dynam RAM (nibble mode)



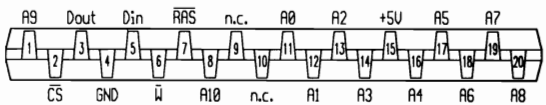
44101 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44101 J-10	Mit	26-FLAT	CMOS	0…+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44101 J-8	Mit	26-FLAT	CMOS	0…+70	<522,5	<5,5	<80	<16	TTL-TS

44102 — 4194304x1-Bit Dynam RAM (static column)



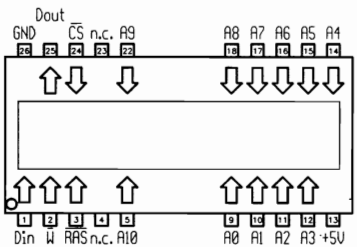
44102 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 41C4002-08	Mat	18-DIP	CMOS	0…+70	<440	<5,5	<80	<16	TTL-TS
MN 41C4002-10	Mat	18-DIP	CMOS	0…+70	<385	<5,5	<100	<16	TTL-TS

44102 — 4194304x1-Bit dynam RAM (static column)



44102 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44102 L-10	Mit	20-ZIP	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44102 L-8	Mit	20-ZIP	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS
MN 41C4002 L-08	Mat	20-ZIP	CMOS	0...+70	<440	<5,5	<80	<16	TTL-TS
MN 41C4002 L-10	Mat	20-ZIP	CMOS	0...+70	<385	<5,5	<100	<16	TTL-TS

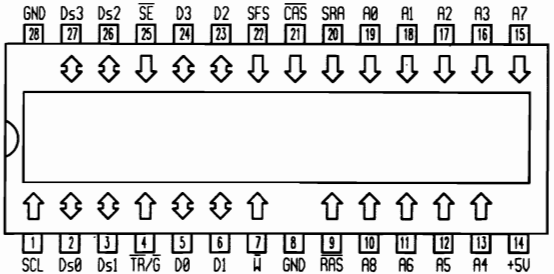
44102 — 4194304x1-Bit dynam RAM (static column)

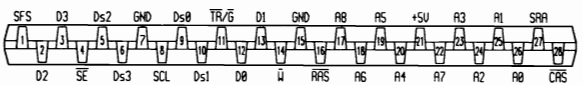


44102 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44102 J-10	Mit	26-FLAT	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44102 J-8	Mit	26-FLAT	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS
MN 41C4002 SJ-08	Mat	26-FLAT	CMOS	0...+70	<440	<5,5	<80	<16	TTL-TS
MN 41C4002 SJ-10	Mat	26-FLAT	CMOS	0...+70	<385	<5,5	<100	<16	TTL-TS

44251 — 262144x4-Bit Multiport Video RAM

44251 — 262144x4-Bit Multiport Video RAM





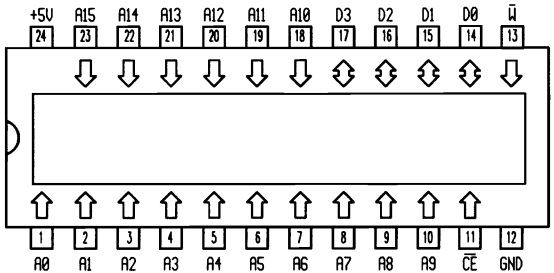
RAS Fall					CAS Fall	Address	Address	Dout	Dout	
CAS	TR/G	W	SFS	SE	SFS	RAS	CAS	RAS	CAS*/W	Mode
L	x	H	x	x	x	x	x	x	x	CAS before RAS refresh
H	L	L	x	L	x	row address	tap point	x	x	Register to memory transfer (Transfer write)
H	L	L	H	x	x	row address	tap point	x	x	alternate transfer write (independent of SE)
H	L	L	L	H	x	row address	tap point	x	x	serial write mode enable (pseudo transfer write)
H	L	H	L	x	x	row address	tap point	x	x	memory to register transfer (transfer read)
H	L	H	H	x	x	row address	tap point	x	x	split register transfer read (must reload tap)
H	H	L	L	x	L	row address	col address	write mask	valid data	load and use write mask write data to dRAM
H	H	L	L	x	H	row address	col A2-A8	write mask	address mask	load and use write mask block write to dRAM
H	H	L	H	x	L	row address	col address	x	valid data	persistent write per bit write data to dRAM
H	H	L	H	x	H	row address	col A2-A8	x	address mask	block write to dRAM (non masked)
H	H	H	H	x	L	refresh address	x	x	write mask	load write mask
H	H	H	H	x	H	refresh address	x	x	color data	load color register

RAS Fall					CAS Fall	Address	Address	Dout	Dout	
CAS	TR/G	W	SFS	SE	SFS	RAS	CAS	RAS	CAS*/W	Mode
L	x	H	x	x	x	x	x	x	x	CAS before RAS refresh
H	L	L	x	L	x	row address	tap point	x	x	Register to memory transfer (Transfer write)
H	L	L	H	x	x	row address	tap point	x	x	alternate transfer write (independent of SE)
H	L	L	L	H	x	row address	tap point	x	x	serial write mode enable (pseudo transfer write)
H	L	H	L	x	x	row address	tap point	x	x	memory to register transfer (transfer read)
H	L	H	H	x	x	row address	tap point	x	x	split register transfer read (must reload tap)
H	H	L	L	x	L	row address	col address	write mask	valid data	load and use write mask write data to dRAM
H	H	L	L	x	H	row address	col A2-A8	write mask	address mask	load and use write mask block write to dRAM
H	H	L	H	x	L	row address	col address	x	valid data	persistent write per bit write data to dRAM
H	H	L	H	x	H	row address	col A2-A8	x	address mask	block write to dRAM (non masked)
H	H	H	H	x	L	refresh address	x	x	write mask	load write mask
H	H	H	H	x	H	refresh address	x	x	color data	load color register

44251 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 44C251-10 DJL	Tix	28-TDIC	CMOS	0...+70	<605	<192,5	<100	<8	TTL-TS
TMS 44C251-12 DJL	Tix	28-TDIC	CMOS	0...+70	<605	<165	<120	<8	TTL-TS
TMS 44C251-15 DJL	Tix	28-TDIC	CMOS	0...+70	<605	<165	<150	<8	TTL-TS

44251 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 44C251-10 SDL	Tix	28-ZIP	CMOS	0...+70	<605	<192,5	<100	<8	TTL-TS
TMS 44C251-12 SDL	Tix	28-ZIP	CMOS	0...+70	<605	<165	<120	<8	TTL-TS
TMS 44C251-15 SDL	Tix	28-ZIP	CMOS	0...+70	<605	<165	<150	<8	TTL-TS

44252 — 65536x4-Bit static RAM

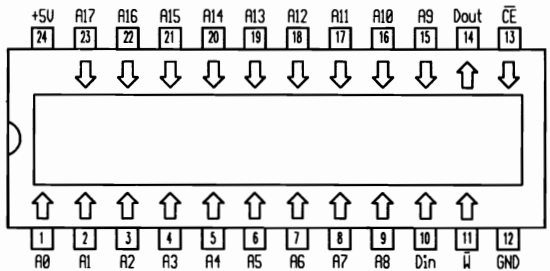


CE	W	D_n	Mode
L	H	data out	read
L	L	data in	write
H	X	Hi-Z	not selected (standby)

44252 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
FCB 61C252-20 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<20		TTL-TS
FCB 61C252-20 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<20		TTL-TS
FCB 61C252-25 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<25		TTL-TS
FCB 61C252-25 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<25		TTL-TS
FCB 61C252-35 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<35		TTL-TS
FCB 61C252-35 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<35		TTL-TS
FCB 61C252-45 P	Phi	24-TDIP	CMOS	0...+70	<660	<55	<45		TTL-TS
FCB 61C252-45 T	Phi	24-FLAT	CMOS	0...+70	<660	<55	<45		TTL-TS

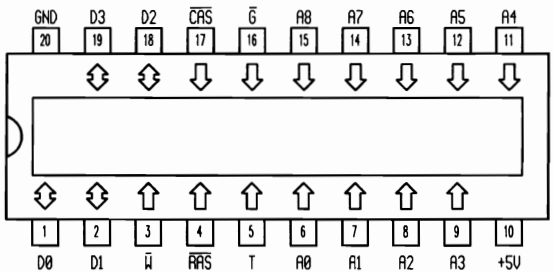
44252 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 44252-015	Mat	24-DIP	CMOS	0...+70	<660	<0,55	<15		TTL-TS
MN 44252-020	Mat	24-DIP	CMOS	0...+70	<660	<0,55	<20		TTL-TS
MN 44252-025	Mat	24-DIP	CMOS	0...+70	<660	<0,55	<25		TTL-TS
MN 44252 S-015	Mat	24-FLAT	CMOS	0...+70	<660	<0,55	<15		TTL-TS
MN 44252 S-020	Mat	24-FLAT	CMOS	0...+70	<660	<0,55	<20		TTL-TS
MN 44252 S-025	Mat	24-FLAT	CMOS	0...+70	<660	<0,55	<25		TTL-TS

44253 — 262144x1-Bit static RAM



CE	W	D_n	Mode
L	H	data out	read
L	L	data in	write
H	X	Hi-Z	not selected (standby)

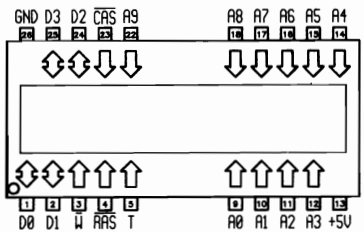
44256 — 26144x4-Bit dynam RAM (page mode)



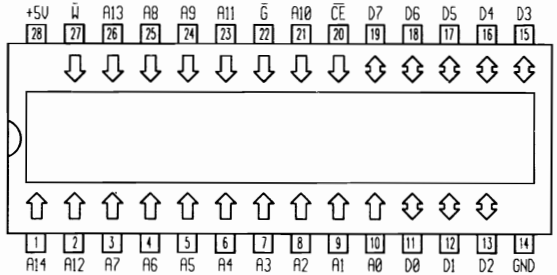
44253 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 44253-015	Mat	24-DIP	CMOS	0...+70	<660	<0,55	<15		TTL-TS
MN 44253-020	Mat	24-DIP	CMOS	0...+70	<660	<0,55	<20		TTL-TS
MN 44253-025	Mat	24-DIP	CMOS	0...+70	<660	<0,55	<25		TTL-TS
MN 44253 S-015	Mat	24-FLAT	CMOS	0...+70	<660	<0,55	<15		TTL-TS
MN 44253 S-020	Mat	24-FLAT	CMOS	0...+70	<660	<0,55	<20		TTL-TS
MN 44253 S-025	Mat	24-FLAT	CMOS	0...+70	<660	<0,55	<25		TTL-TS

44256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SMJ 44C256-12 JDS	Tix	20-TDIC	CMOS	-55...+125			<120	<8	TTL-TS
SMJ 44C256-15 JDS	Tix	20-TDIC	CMOS	-55...+125			<150	<8	TTL-TS
TMS 44C256-10 NL	Tix	20-TDIP	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 44C256-12 NL	Tix	20-TDIP	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 44C256-15 NL	Tix	20-TDIP	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 44C256-10 NL	Tix	20-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 44C256-12 NL	Tix	20-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 44C256-15 NL	Tix	20-TDIP	CMOS	0...+70			<150	<8	TTL-TS

44256 — 32768x8-Bit static RAM



44256 — 32768x8-Bit static RAM



CE	G	W	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

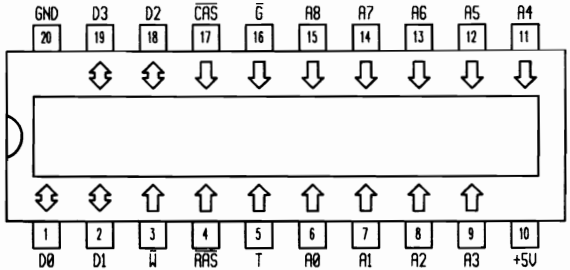
44256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SMJ 44C256-12 HJS	Tix	26-FLAT	CMOS	-55...+125			<120	<8	TTL-TS
SMJ 44C256-15 HJS	Tix	26-FLAT	CMOS	-55...+125			<150	<8	TTL-TS
TMS 44C256-10 DJL	Tix	26-FLAT	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 44C256-12 DJL	Tix	26-FLAT	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 44C256-15 DJL	Tix	26-FLAT	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 44C256-10 JDL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 44C256-12 JDL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 44C256-15 JDL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

44256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
FCB 61C257-100 P	Phi	28-DIP	CMOS	0...+70	<440	<27,5µ	<100		TTL-TS
FCB 61C257-100 T	Phi	28-FLAT	CMOS	0...+70	<440	<27,5µ	<100		TTL-TS
FCB 61C257-55 P	Phi	28-DIP	CMOS	0...+70	<440	<27,5µ	<55		TTL-TS
FCB 61C257-55 T	Phi	28-FLAT	CMOS	0...+70	<440	<27,5µ	<55		TTL-TS
FCB 61C257-70 P	Phi	28-DIP	CMOS	0...+70	<440	<27,5µ	<70		TTL-TS
FCB 61C257-70 T	Phi	28-FLAT	CMOS	0...+70	<440	<27,5µ	<70		TTL-TS
MN 44251-015	Mat	28-DIP	CMOS	0...+70	<660	<0,55	<15		TTL-TS
MN 44251-020	Mat	28-DIP	CMOS	0...+70	<660	<0,55	<20		TTL-TS

44256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 44251-025	Mat	28-DIP	CMOS	0...+70	<660	<0,55	<25		TTL-TS
MN 44251 S-015	Mat	28-FLAT	CMOS	0...+70	<660	<0,55	<15		TTL-TS
MN 44251 S-020	Mat	28-FLAT	CMOS	0...+70	<660	<0,55	<20		TTL-TS
MN 44251 S-025	Mat	28-FLAT	CMOS	0...+70	<660	<0,55	<25		TTL-TS
MN 44256-010 L	Mat	28-DIP	CMOS	0...+70	<247,5	<16,5	<100		TTL-TS
MN 44256-010 LL	Mat	28-DIP	CMOS	0...+70	<247,5	<16,5	<100		TTL-TS
MN 44256 S-010 L	Mat	28-FLAT	CMOS	0...+70	<247,5	<16,5	<100		TTL-TS
MN 44256 S-010 LL	Mat	28-FLAT	CMOS	0...+70	<247,5	<16,5	<100		TTL-TS

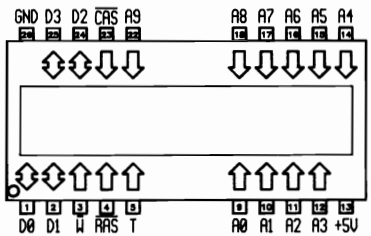
44257

262144x4-Bit dynam RAM (static column)

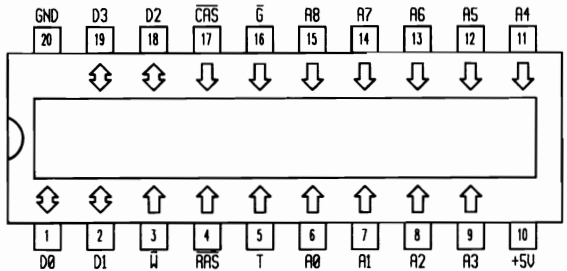


44257 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 44C257-10 NL	Tix	20-TDIP	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 44C257-12 NL	Tix	20-TDIP	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 44C257-15 NL	Tix	20-TDIP	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 44C257-10 NL	Tix	20-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 44C257-12 NL	Tix	20-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 44C257-15 NL	Tix	20-TDIP	CMOS	0...+70			<150	<8	TTL-TS

44257 — 262144x4-Bit dynam RAM (static column)



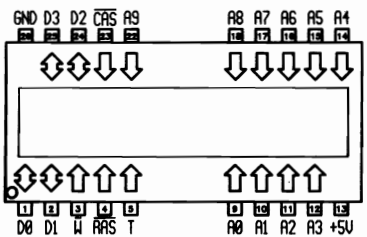
44259 — 262144x4-Bit dynamic RAM



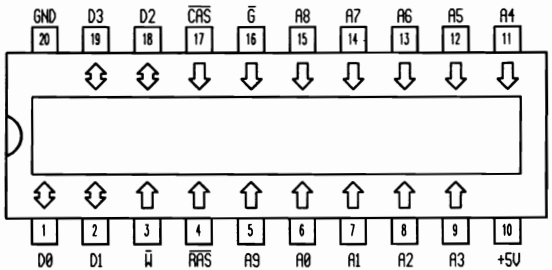
44257 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMS 44C257-10 DJL	Tix	26-FLAT	CMOS	0...+70	<385	<16,5	<100	<8	TTL-TS
TMS 44C257-12 DJL	Tix	26-FLAT	CMOS	0...+70	<330	<16,5	<120	<8	TTL-TS
TMS 44C257-15 DJL	Tix	26-FLAT	CMOS	0...+70	<302,5	<16,5	<150	<8	TTL-TS
TMX 44C257-10 JDL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 44C257-12 JDL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 44C257-15 JDL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

44259 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 44C259-10 NL	Tix	20-TDIP	CMOS	0...+70			<100	<8	TTL-TS
TMX 44C259-12 NL	Tix	20-TDIP	CMOS	0...+70			<120	<8	TTL-TS
TMX 44C259-15 NL	Tix	20-TDIP	CMOS	0...+70			<150	<8	TTL-TS

44259 — 262144x4-Bit dynamic RAM



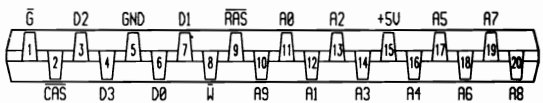
44400 — 1048576x4-Bit dynam RAM (page mode)



44259 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 44C259-10 JDL	Tix	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
TMX 44C259-12 JDL	Tix	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
TMX 44C259-15 JDL	Tix	26-FLAT	CMOS	0...+70			<150	<8	TTL-TS

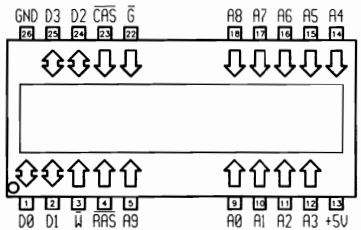
44400 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 41C41000-08	Mat	20-DIP	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C41000-10	Mat	20-DIP	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44400 — 1048576x4-Bit dynam RAM (page mode)



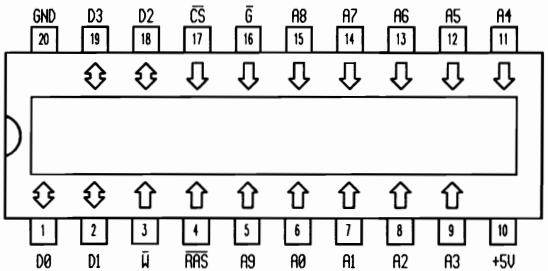
44400 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44400 L-10	Mit	20-ZIP	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44400 L-8	Mit	20-ZIP	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS
MN 41C41000 L-08	Mat	20-ZIP	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C41000 L-10	Mat	20-ZIP	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44400 — 1048576x4-Bit dynam. RAM (page mode)



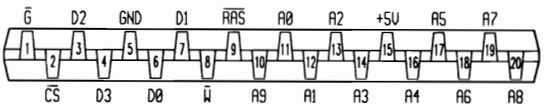
44400 Typ · Type · Tipo	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 514400 J-10	Sie	26-FLAT	CMOS	0...+70	<467,5	<11	<100	<16	TTL-TS
HYB 514400 J-80	Sie	26-FLAT	CMOS	0...+70	<522,5	<11	<80	<16	TTL-TS
M5M 44400 J-10	Mit	26-FLAT	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44400 J-8	Mit	26-FLAT	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS
MN 41C41000 SJ-08	Mat	26-FLAT	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C41000 SJ-10	Mat	26-FLAT	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44402 — 1048576x4-Bit dynam. RAM (static column)



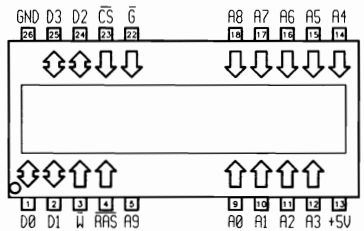
44402 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 41C41002-08	Mat	20-DIP	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C41002-10	Mat	20-DIP	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44402 — 1048576x4-Bit dynam. RAM (static column)

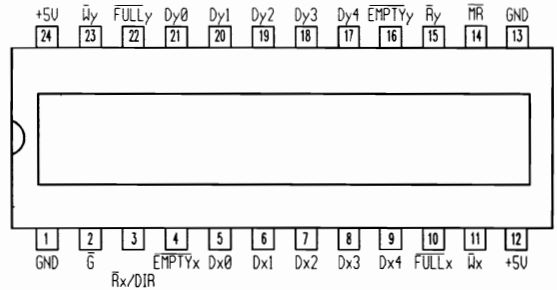


44402 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44402 L-10	Mit	20-ZIP	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44402 L-8	Mit	20-ZIP	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS
MN 41C41002 L-08	Mat	20-ZIP	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C41002 L-10	Mat	20-ZIP	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

44402 — 1048576x4-Bit dynam. RAM (static column)



45264 — (64x5)x2-Bit bidirectional Biport FIFO

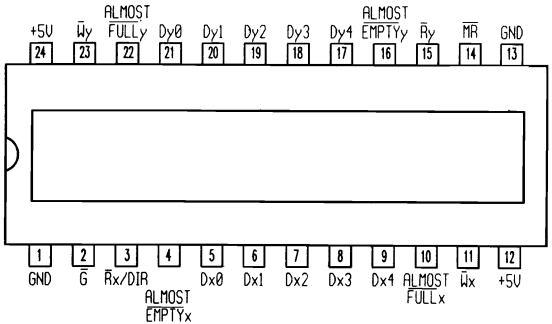


W	CS	G	RS	D_n	Match	Mode
X	X	X	L	—	High	reset clear
X	H	X	H	Hi-Z	High	deselect
H	L	H	H	data in	Low	Miss-nomatch
H	L	H	H	data in	High	match
H	L	L	H	data out	High	read
L	L	X	H	data in	High	write

44402 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44402 J-10	Mit	26-FLAT	CMOS	0...+70	<467,5	<5,5	<100	<16	TTL-TS
M5M 44402 J-8	Mit	26-FLAT	CMOS	0...+70	<522,5	<5,5	<80	<16	TTL-TS
MN 41C41002 SJ-08	Mat	26-FLAT	CMOS	0...+70	<467,5	<5,5	<80	<16	TTL-TS
MN 41C41002 SJ-10	Mat	26-FLAT	CMOS	0...+70	<412,5	<5,5	<100	<16	TTL-TS

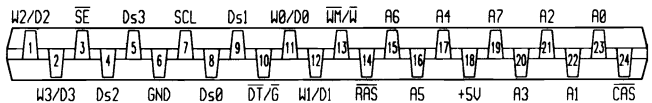
45264 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45264 N-55	Sgs	24-DIP	CMOS	0...+70	<330		<55		
MK 45264 N-70	Sgs	24-DIP	CMOS	0...+70	<330		<70		

45265 — (64x5)x2-Bit bidirectional Biport FIFO



$\overline{W}$	$\overline{CS}$	$\overline{G}$	$\overline{RS}$	D_n	Match	Mode
X	X	X	L	—	High	reset clear
X	H	X	H	Hi-Z	High	deselect
H	L	H	H	data in	Low	Miss-nomatch
H	L	H	H	data in	High	match
H	L	L	H	data out	High	read
L	L	X	H	data in	High	write

47464 — 65536x4-Bit Multi-Port dynamic RAM



45265 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 45265 N-55	Sgs	24-DIP	CMOS	0...+70	<330		<55		
MK 45265 N-70	Sgs	24-DIP	CMOS	0...+70	<330		<70		

47464 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 47464 L-12	Mat	24-ZIP	NMOS	0...+70	<523	<110	<120	<4	TTL

$\overline{DT/G}$	$\overline{W}$	$\overline{SE}$	RAM-Port	SAM-Port
H	H	X	normal read/write	—
H	L	X	write mask	—
L	H	X	read transfer (RAM→SRAM)	output mode set
L	L	L	write transfer (SRAM→RAM)	input mode
L	L	H	read refresh	input mode

Ordinary read/write

$\overline{RAS}$	$\overline{CAS}$	$\overline{WM/W}$	$\overline{DT/G}$	A_x	D_n	Mode
H	H	X	X	X	—	standby
L	L	H	H→L	address	data out	read
L	L	L	H→X	address	data in	early write
L	L	H→L	H→X	address	data in	delayed write
L	L	H→L	H→L→H	address	data out→data in	read modify write
L	H	X	H→X	row address	Hi-Z	RAS only refresh
H→L	L	X	H→X	X	Hi-Z	CAS before RAS refresh

Write mask

$\overline{DT/G}$	$\overline{WM/W}$	$W_0...W_3$	Mode
H	H	X	early write to $D_0...D_3$ possible
H	L	H	write possible
H	L	L	write impossible (mask state)

Serial access operation: asynchronous RAM-port

$\overline{DT/G}$	$\overline{WM/W}$	SCL	$\overline{SE}$	D_n	Mode
H	X	clock	L	input/output*	sequential access enable
H	X	clock	H	input/output*	sequential access disable

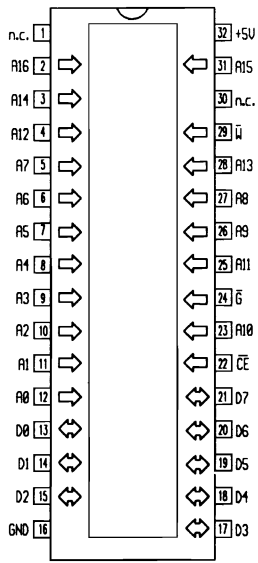
* Nach dem pseudo write transfer ist der input mode aktiv, nach dem read transfer ist der output mode aktiv.
* After the pseudo write transfer, the input mode is used, after the read transfer mode the output mode is used.

Write mask operation

$\overline{DT/G}$	$\overline{WM/W}$	W_0/D_0	W_1/D_1	W_2/D_3	W_4/D_4	Mode
H	H	X	X	X	X	write enable
H	L	L	H	L	H	write enable (D_1, D_4) write disable (D_0, D_3)

48127

131072x8-Bit static RAM

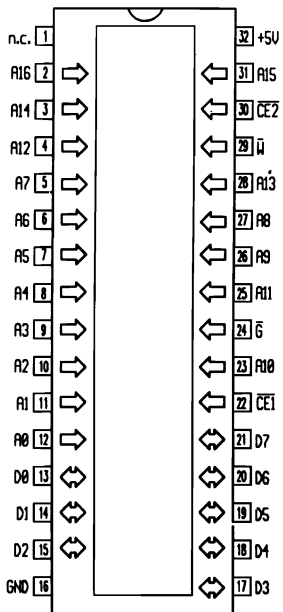


$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

48127 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 48127 N-55	Sgs	32-DIP	CMOS	0...+70			<55		TTL-TS
MK 48127 N-70	Sgs	32-DIP	CMOS	0...+70			<70		TTL-TS
MK 48127 N-85	Sgs	32-DIP	CMOS	0...+70			<85		TTL-TS
MK 48127 X-55	Sgs	32-FLAT	CMOS	0...+70			<55		TTL-TS
MK 48127 X-70	Sgs	32-FLAT	CMOS	0...+70			<70		TTL-TS
MK 48127 X-85	Sgs	32-FLAT	CMOS	0...+70			<85		TTL-TS

48128

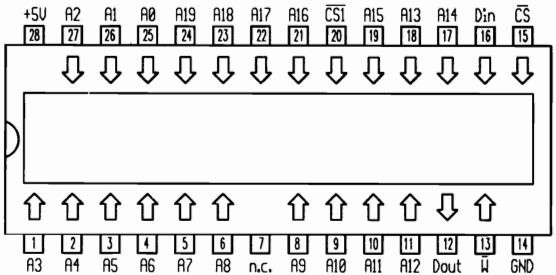
131072x8-Bit static RAM



W	CE1	CE2	G	D_n	Power	Mode
X	H	X	X	Hi-Z	standby	deselect
X	X	L	X	Hi-Z	standby	deselect
H	L	H	H	Hi-Z	active	read
H	L	H	L	data out	active	read
L	L	H	X	data in	active	write

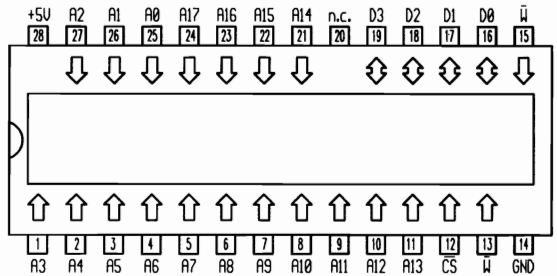
48128 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
FCB 61C1025-35 LLP	Phi	32-DIP	CMOS	0...+70	<440	<11µ	<35		TTL-TS
FCB 61C1025-35 LLT	Phi	32-FLAT	CMOS	0...+70	<440	<11µ	<35		TTL-TS
FCB 61C1025-35 LP	Phi	32-DIP	CMOS	0...+70	<440	<0,55	<35		TTL-TS
FCB 61C1025-35 LT	Phi	32-FLAT	CMOS	0...+70	<440	<0,55	<35		TTL-TS
FCB 61C1025-45 LLP	Phi	32-DIP	CMOS	0...+70	<440	<11µ	<45		TTL-TS
FCB 61C1025-45 LLT	Phi	32-FLAT	CMOS	0...+70	<440	<11µ	<45		TTL-TS
FCB 61C1025-45 LP	Phi	32-DIP	CMOS	0...+70	<440	<0,55	<45		TTL-TS
FCB 61C1025-45 LT	Phi	32-FLAT	CMOS	0...+70	<440	<0,55	<45		TTL-TS
FCB 61C1025-55 LLP	Phi	32-DIP	CMOS	0...+70	<440	<11µ	<55		TTL-TS
FCB 61C1025-55 LLT	Phi	32-FLAT	CMOS	0...+70	<440	<11µ	<55		TTL-TS
FCB 61C1025-55 LP	Phi	32-DIP	CMOS	0...+70	<440	<0,55	<55		TTL-TS
FCB 61C1025-55 LT	Phi	32-FLAT	CMOS	0...+70	<440	<0,55	<55		TTL-TS
MK 48128 N-55	Sgs	32-DIP	CMOS	0...+70			<55		TTL-TS
MK 48128 N-70	Sgs	32-DIP	CMOS	0...+70			<70		TTL-TS
MK 48128 N-85	Sgs	32-DIP	CMOS	0...+70			<85		TTL-TS
MK 48128 X-55	Sgs	32-FLAT	CMOS	0...+70			<55		TTL-TS
MK 48128 X-70	Sgs	32-FLAT	CMOS	0...+70			<70		TTL-TS
MK 48128 X-85	Sgs	32-FLAT	CMOS	0...+70			<85		TTL-TS
TC 551001 FL-100	Tos	32-FLAT	CMOS	0...+70	<27,5	<0,55	<100		TTL-TS
TC 551001 FL-70	Tos	32-FLAT	CMOS	0...+70	<27,5	<0,55	<70		TTL-TS
TC 551001 FL-85	Tos	32-FLAT	CMOS	0...+70	<27,5	<0,55	<85		TTL-TS
TC 551001 PL-100	Tos	32-DIP	CMOS	0...+70	<27,5	<0,55	<100		TTL-TS
TC 551001 PL-70	Tos	32-DIP	CMOS	0...+70	<27,5	<0,55	<70		TTL-TS
TC 551001 PL-85	Tos	32-DIP	CMOS	0...+70	<27,5	<0,55	<85		TTL-TS

51001 — 1048576x1-Bit static RAM



CS	W	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

51004 — 262144x4-Bit static RAM



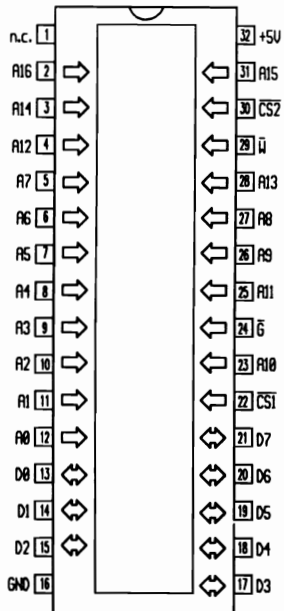
W	CS	G	D_n	Mode
X	H	X	Hi-Z	standby
H	L	H	Hi-Z	output disabled
H	L	L	data out	read
L	L	X	data in	write

51001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
M5M 51001 J-35	Mit	28-FLAT	CMOS	0...+70	<660	<55	<35		TTL-TS
M5M 51001 J-45	Mit	28-FLAT	CMOS	0...+70	<660	<55	<45		TTL-TS
M5M 51001 P-35	Mit	28-DIP	CMOS	0...+70	<660	<55	<35		TTL-TS
M5M 51001 P-45	Mit	28-DIP	CMOS	0...+70	<660	<55	<45		TTL-TS

51004 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 51004 J-35	Mit	28-FLAT	CMOS	0...+70	<660	<55	<35		TTL-TS
M5M 51004 J-45	Mit	28-FLAT	CMOS	0...+70	<660	<55	<45		TTL-TS
M5M 51004 P-35	Mit	28-DIP	CMOS	0...+70	<660	<55	<35		TTL-TS
M5M 51004 P-45	Mit	28-DIP	CMOS	0...+70	<660	<55	<45		TTL-TS

51008

131072x8-Bit static RAM

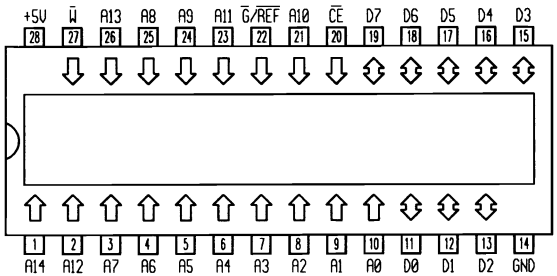


W	CS1	CS2	G	D_n	Mode
X	H	X	X	Hi-Z	not selected (power down)
X	X	L	X	Hi-Z	not selected (power down)
H	L	H	H	Hi-Z	output disabled
H	L	H	L	data out	read
L	L	H	X	data in	write

51008 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 51008 FP-10	Mit	32-FLAT	CMOS	0...+70	<550	<11	<100		TTL-TS
M5M 51008 FP-10L	Mit	32-FLAT	CMOS	0...+70	<550	<0,55	<100		TTL-TS
M5M 51008 FP-12	Mit	32-FLAT	CMOS	0...+70	<550	<11	<120		TTL-TS
M5M 51008 FP-12L	Mit	32-FLAT	CMOS	0...+70	<550	<0,55	<120		TTL-TS
M5M 51008 FP-70	Mit	32-FLAT	CMOS	0...+70	<550	<11	<70		TTL-TS
M5M 51008 FP-70L	Mit	32-FLAT	CMOS	0...+70	<550	<0,55	<70		TTL-TS
M5M 51008 FP-85	Mit	32-FLAT	CMOS	0...+70	<550	<11	<85		TTL-TS
M5M 51008 FP-85L	Mit	32-FLAT	CMOS	0...+70	<550	<0,55	<85		TTL-TS
M5M 51008 P-10	Mit	32-DIP	CMOS	0...+70	<550	<11	<100		TTL-TS
M5M 51008 P-10L	Mit	32-DIP	CMOS	0...+70	<550	<0,55	<100		TTL-TS
M5M 51008 P-12	Mit	32-DIP	CMOS	0...+70	<550	<11	<120		TTL-TS
M5M 51008 P-12L	Mit	32-DIP	CMOS	0...+70	<550	<0,55	<120		TTL-TS
M5M 51008 P-70	Mit	32-DIP	CMOS	0...+70	<550	<11	<70		TTL-TS
M5M 51008 P-70L	Mit	32-DIP	CMOS	0...+70	<550	<0,55	<70		TTL-TS
M5M 51008 P-85	Mit	32-DIP	CMOS	0...+70	<550	<11	<85		TTL-TS
M5M 51008 P-85L	Mit	32-DIP	CMOS	0...+70	<550	<0,55	<85		TTL-TS

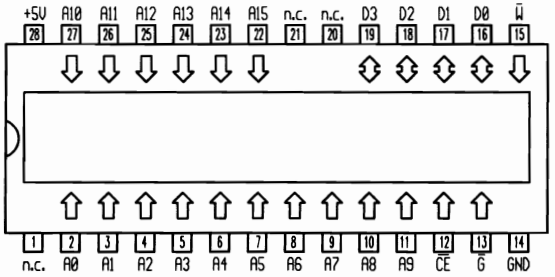
51832

32768x8-Bit pseudo-static RAM



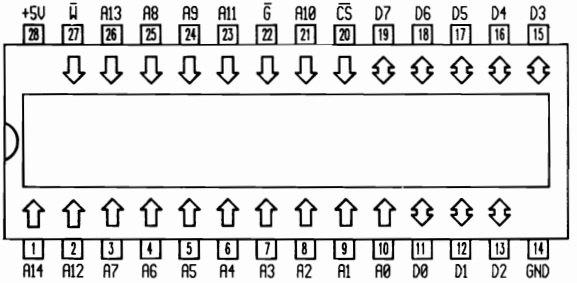
51832 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 51832 F-10	Tos	28-FLAT	CMOS	0...+70	<248	<5,5	<100	<4	TTL-TS
TC 51832 F-12	Tos	28-FLAT	CMOS	0...+70	<220	<5,5	<120	<4	TTL-TS
TC 51832 F-85	Tos	28-FLAT	CMOS	0...+70	<303	<5,5	<85	<4	TTL-TS
TC 51832 FL-10	Tos	28-FLAT	CMOS	0...+70	<248	<1,1	<100	<4	TTL-TS
TC 51832 FL-12	Tos	28-FLAT	CMOS	0...+70	<220	<1,1	<120	<4	TTL-TS
TC 51832 FL-85	Tos	28-FLAT	CMOS	0...+70	<303	<1,1	<85	<4	TTL-TS
TC 51832 P-10	Tos	28-DIP	CMOS	0...+70	<248	<5,5	<100	<4	TTL-TS
TC 51832 P-12	Tos	28-DIP	CMOS	0...+70	<220	<5,5	<120	<4	TTL-TS
TC 51832 P-85	Tos	28-DIP	CMOS	0...+70	<303	<5,5	<85	<4	TTL-TS
TC 51832 PL-10	Tos	28-DIP	CMOS	0...+70	<248	<1,1	<100	<4	TTL-TS
TC 51832 PL-12	Tos	28-DIP	CMOS	0...+70	<220	<1,1	<120	<4	TTL-TS
TC 51832 PL-85	Tos	28-DIP	CMOS	0...+70	<303	<1,1	<85	<4	TTL-TS
TC 51832 SP-10	Tos	28-TDIP	CMOS	0...+70	<248	<5,5	<100	<4	TTL-TS
TC 51832 SP-12	Tos	28-TDIP	CMOS	0...+70	<220	<5,5	<120	<4	TTL-TS
TC 51832 SP-85	Tos	28-TDIP	CMOS	0...+70	<303	<5,5	<85	<4	TTL-TS
TC 51832 SPL-10	Tos	28-TDIP	CMOS	0...+70	<248	<1,1	<100	<4	TTL-TS
TC 51832 SPL-12	Tos	28-TDIP	CMOS	0...+70	<220	<1,1	<120	<4	TTL-TS
TC 51832 SPL-85	Tos	28-TDIP	CMOS	0...+70	<303	<1,1	<85	<4	TTL-TS

61253 — 65536x4-Bit static RAM



CE	W	D_n	Mode
L	H	data out	read
L	L	data in	write
H	X	Hi-Z	not selected (standby)

61256 — 32768x8-Bit static RAM



W	CS	G	D_n	Mode
X	H	X	Hi-Z	standby
H	L	H	Hi-Z	output disabled
H	L	L	data out	read
L	L	X	data in	write

61253 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
FCB 61C253-20 P	Phi	28-TDIP	CMOS	0...+70	<660	<55	<20		TTL-TS
FCB 61C253-20 T	Phi	28-FLAT	CMOS	0...+70	<660	<55	<20		TTL-TS
FCB 61C253-25 P	Phi	28-TDIP	CMOS	0...+70	<660	<55	<25		TTL-TS
FCB 61C253-25 T	Phi	28-FLAT	CMOS	0...+70	<660	<55	<25		TTL-TS
FCB 61C253-35 P	Phi	28-TDIP	CMOS	0...+70	<660	<55	<35		TTL-TS
FCB 61C253-35 T	Phi	28-FLAT	CMOS	0...+70	<660	<55	<35		TTL-TS
FCB 61C253-45 P	Phi	28-TDIP	CMOS	0...+70	<660	<55	<45		TTL-TS
FCB 61C253-45 T	Phi	28-FLAT	CMOS	0...+70	<660	<55	<45		TTL-TS

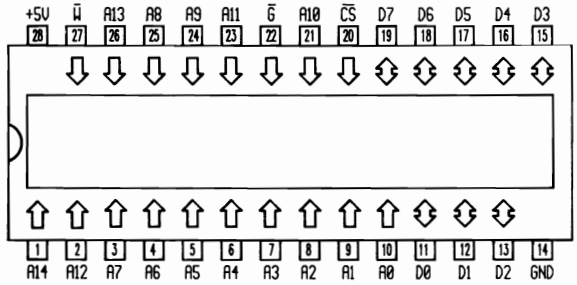
61256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 62256 FP-10	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<100		TTL-TS
HM 62256 FP-12	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<120		TTL-TS
HM 62256 FP-15	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<150		TTL-TS
HM 62256 FP-8	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<85		TTL-TS
HM 62256 LFP-10	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<100		TTL-TS
HM 62256 LFP-12	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<120		TTL-TS
HM 62256 LFP-15	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<150		TTL-TS
HM 62256 LFP-8	Hit	28-FLAT	CMOS	0...+70	<385	<82,5	<85		TTL-TS

61256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 62256 LP-10	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<100		TTL-TS
HM 62256 LP-12	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<120		TTL-TS
HM 62256 LP-15	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<150		TTL-TS
HM 62256 LP-8	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<85		TTL-TS
HM 62256 P-10	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<100		TTL-TS
HM 62256 P-12	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<120		TTL-TS
HM 62256 P-15	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<150		TTL-TS
HM 62256 P-8	Hit	28-DIP	CMOS	0...+70	<385	<82,5	<85		TTL-TS
KM 62256 LP-10	Sam	28-DIP	CMOS	0...+70	<248	<550µ	<100		TTL-TS
KM 62256 LP-12	Sam	28-DIP	CMOS	0...+70	<248	<550µ	<120		TTL-TS
KM 62256 LP-15	Sam	28-DIP	CMOS	0...+70	<248	<550µ	<150		TTL-TS
KM 62256 P-10	Sam	28-DIP	CMOS	0...+70	<248	<5,5	<100		TTL-TS
KM 62256 P-12	Sam	28-DIP	CMOS	0...+70	<248	<5,5	<120		TTL-TS
KM 62256 P-15	Sam	28-DIP	CMOS	0...+70	<248	<5,5	<150		TTL-TS
M5M 5256 BFP-10	Mit	28-FLAT	CMOS	0...+70	<385	<11	<100		TTL-TS
M5M 5256 BFP-10L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5256 BFP-10LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5256 BFP-12	Mit	28-FLAT	CMOS	0...+70	<385	<11	<120		TTL-TS
M5M 5256 BFP-12L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5256 BFP-12LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5256 BFP-15	Mit	28-FLAT	CMOS	0...+70	<385	<11	<150		TTL-TS
M5M 5256 BFP-15L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<150		TTL-TS
M5M 5256 BFP-15LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<150		TTL-TS
M5M 5256 BFP-70	Mit	28-FLAT	CMOS	0...+70	<385	<11	<70		TTL-TS
M5M 5256 BFP-70L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<70		TTL-TS
M5M 5256 BFP-70LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<70		TTL-TS
M5M 5256 BFP-85	Mit	28-FLAT	CMOS	0...+70	<385	<11	<85		TTL-TS
M5M 5256 BFP-85L	Mit	28-FLAT	CMOS	0...+70	<385	<0,55	<85		TTL-TS
M5M 5256 BFP-85LL	Mit	28-FLAT	CMOS	0...+70	<385	<0,11	<85		TTL-TS
M5M 5256 BKP-10	Mit	28-TDIP	CMOS	0...+70	<385	<11	<100		TTL-TS
M5M 5256 BKP-10L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5256 BKP-10LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5256 BKP-12	Mit	28-TDIP	CMOS	0...+70	<385	<11	<120		TTL-TS
M5M 5256 BKP-12L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5256 BKP-12LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5256 BKP-15	Mit	28-TDIP	CMOS	0...+70	<385	<11	<150		TTL-TS
M5M 5256 BKP-15L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<150		TTL-TS

61256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 5256 BKP-15LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<150		TTL-TS
M5M 5256 BKP-70	Mit	28-TDIP	CMOS	0...+70	<385	<11	<70		TTL-TS
M5M 5256 BKP-70L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<70		TTL-TS
M5M 5256 BKP-70LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<70		TTL-TS
M5M 5256 BKP-85	Mit	28-TDIP	CMOS	0...+70	<385	<11	<85		TTL-TS
M5M 5256 BKP-85L	Mit	28-TDIP	CMOS	0...+70	<385	<0,55	<85		TTL-TS
M5M 5256 BKP-85LL	Mit	28-TDIP	CMOS	0...+70	<385	<0,11	<85		TTL-TS
M5M 5256 BP-10	Mit	28-DIP	CMOS	0...+70	<385	<11	<100		TTL-TS
M5M 5256 BP-10L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<100		TTL-TS
M5M 5256 BP-10LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<100		TTL-TS
M5M 5256 BP-12	Mit	28-DIP	CMOS	0...+70	<385	<11	<120		TTL-TS
M5M 5256 BP-12L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<120		TTL-TS
M5M 5256 BP-12LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<120		TTL-TS
M5M 5256 BP-15	Mit	28-DIP	CMOS	0...+70	<385	<11	<150		TTL-TS
M5M 5256 BP-15L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<150		TTL-TS
M5M 5256 BP-15LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<150		TTL-TS
M5M 5256 BP-70	Mit	28-DIP	CMOS	0...+70	<385	<11	<70		TTL-TS
M5M 5256 BP-70L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<70		TTL-TS
M5M 5256 BP-70LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<70		TTL-TS
M5M 5256 BP-85	Mit	28-DIP	CMOS	0...+70	<385	<11	<85		TTL-TS
M5M 5256 BP-85L	Mit	28-DIP	CMOS	0...+70	<385	<0,55	<85		TTL-TS
M5M 5256 BP-85LL	Mit	28-DIP	CMOS	0...+70	<385	<0,11	<85		TTL-TS
MCM 6206 J-45	Mot	28-FLAT	CMOS	0...+70	<660		<45		TTL-TS
MCM 6206 J-55	Mot	28-FLAT	CMOS	0...+70	<605		<55		TTL-TS
MCM 6206 J-70	Mot	28-FLAT	CMOS	0...+70	<550		<70		TTL-TS
MCM 6206 P-45	Mot	28-DIP	CMOS	0...+70	<660		<45		TTL-TS
MCM 6206 P-55	Mot	28-DIP	CMOS	0...+70	<605		<55		TTL-TS
MCM 6206 P-70	Mot	28-DIP	CMOS	0...+70	<550		<70		TTL-TS
MCM 60L256 P-10	Mot	28-DIP	CMOS	0...+70	<385	<0,55	<100		TTL-TS
MCM 60L256 P-12	Mot	28-DIP	CMOS	0...+70	<385	<0,55	<120		TTL-TS
MCM 60L256 P-85	Mot	28-DIP	CMOS	0...+70	<385	<0,55	<85		TTL-TS
MCM 60256 P-10	Mot	28-DIP	CMOS	0...+70	<385	<16,5	<100		TTL-TS
MCM 60256 P-12	Mot	28-DIP	CMOS	0...+70	<385	<16,5	<120		TTL-TS
MCM 60256 P-85	Mot	28-DIP	CMOS	0...+70	<385	<16,5	<85		TTL-TS
MK 4832L N-120	Sgs	28-DIP	CMOS	0...+70	<385	<16,5	<120		TTL-TS
MK 4832L N-70	Sgs	28-DIP	CMOS	0...+70	<385	<16,5	<70		TTL-TS
MK 4832 N-120	Sgs	28-DIP	CMOS	0...+70	<385	<16,5	<120		TTL-TS

61256 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MK 4832 N-70	Sgs	28-DIP	CMOS	0...+70	<385	<16,5	<70		TTL-TS
NMC 61256 N-100	Nsc	28-DIP	CMOS	0...+70	<275	<22	<100		TTL-TS
NMC 61256 N-100 L	Nsc	28-DIP	CMOS	0...+70	<275	<11	<100		TTL-TS
NMC 61256 N-120	Nsc	28-DIP	CMOS	0...+70	<275	<22	<120		TTL-TS
NMC 61256 N-120 L	Nsc	28-DIP	CMOS	0...+70	<275	<11	<120		TTL-TS
NMC 61256 N-70	Nsc	28-DIP	CMOS	0...+70	<275	<22	<70		TTL-TS
NMC 61256 N-70 L	Nsc	28-DIP	CMOS	0...+70	<275	<11	<70		TTL-TS
TC 55257 AFL-10	Tos	28-FLAT	CMOS	0...+70	<27,5	<0,55	<100		TTL-TS
TC 55257 AFL-10L	Tos	28-FLAT	CMOS	0...+70	<27,5	<11µ	<100		TTL-TS
TC 55257 AFL-12	Tos	28-FLAT	CMOS	0...+70	<27,5	<0,55	<120		TTL-TS
TC 55257 AFL-12L	Tos	28-FLAT	CMOS	0...+70	<27,5	<11µ	<120		TTL-TS
TC 55257 AFL-85	Tos	28-FLAT	CMOS	0...+70	<27,5	<0,55	<85		TTL-TS
TC 55257 AFL-85L	Tos	28-FLAT	CMOS	0...+70	<27,5	<11µ	<85		TTL-TS
TC 55257 APL-10	Tos	28-DIP	CMOS	0...+70	<27,5	<0,55	<100		TTL-TS
TC 55257 APL-10L	Tos	28-DIP	CMOS	0...+70	<27,5	<11µ	<100		TTL-TS
TC 55257 APL-12	Tos	28-DIP	CMOS	0...+70	<27,5	<0,55	<120		TTL-TS
TC 55257 APL-12L	Tos	28-DIP	CMOS	0...+70	<27,5	<11µ	<120		TTL-TS
TC 55257 APL-85	Tos	28-DIP	CMOS	0...+70	<27,5	<0,55	<85		TTL-TS
TC 55257 APL-85L	Tos	28-DIP	CMOS	0...+70	<27,5	<11µ	<85		TTL-TS

61256 — 32768x8-Bit pseudo-static RAM

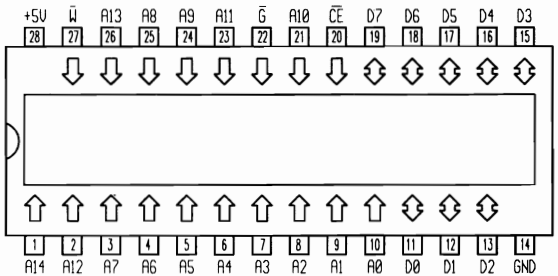


$\overline{CE}$	$\overline{G}/V_{pp}$	V_{cc}	D_{out}	Mode
L	L	+5V	data out	read
H	X	+5V	Hi-Z	standby
L	+13V	+6V	data in	program
L	L	+6V	data out	program verify
H	+13V	+6V	Hi-Z	program inhibit

61256 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 42832 C-12	Nec	28-DIP	CMOS	0...+70	<275	2.75	<120	<4	TTL-TS
µPD 42832 C-15	Nec	28-DIP	CMOS	0...+70	<220	2.75	<150	<4	TTL-TS
µPD 42832 G-12	Nec	28-FLAT	CMOS	0...+70	<275	2.75	<100	<4	TTL-TS
µPD 42832 G-15	Nec	28-FLAT	CMOS	0...+70	<220	2.75	<150	<4	TTL-TS

61256

32768x8-Bit pseudo-static RAM



1) Der Ausgang muß vorher den Low-Z-Level halten.
2) Der Ausgang muß vorher ausgeschaltet sein.
3) CE Pulsweite ≥300µ sec.
4) Einmal ausgeschaltet, bleibt der Ausgang Hi-Z.

1) Output must keep Low-Z State in previous precharge cycle.
2) Output must turn off in previous precharge cycle.
3) CE pulse width ≥300µ sec.
4) Once output turn off, out remain in Hi-Z state.

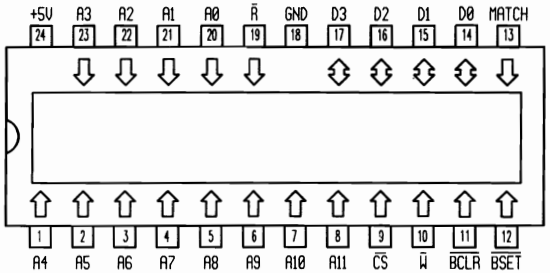
1) La sortie doit maintenir auparavant le niveau Z bas (low).
2) La sortie doit être d'abord déconnectée.
3) Largeur d'impulsion CE ≥300µs.
4) Une fois déconnectée, la sortie est maintenue au niveau Hi-Z.

1) L'uscita deve tenere precedentemente il livello low-z.
2) L'uscita deve essere disinserita precedentemente.
3) Ampiezza di cadenza CE ≥300µ se.
4) Una volta disinserita, l'uscita resta HI-Z.

1) La salida debe mantener el estado de baja impedancia en el ciclo de carga previo.
2) La salida debe estar desconectada previamente.
3) pulsos CE de duración ≥300µs.
4) Cuando se desconecta, la salida permanece en estado de alta impedancia.

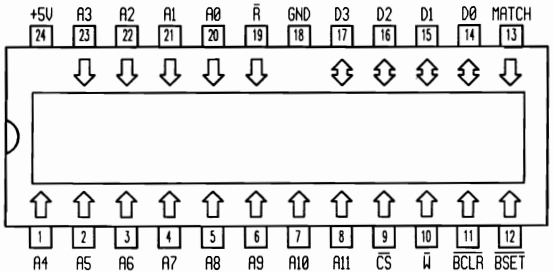
61256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 65256 AP-12	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 AP-15	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 AP-20	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS
HM 65256 ASP-12	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 ASP-15	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 ASP-20	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS
HM 65256 BFP-12	Hit	28-FLAT	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 BFP-15	Hit	28-FLAT	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 BFP-20	Hit	28-FLAT	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS
HM 65256 BLFP-12	Hit	28-FLAT	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 BLFP-15	Hit	28-FLAT	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 BLFP-20	Hit	28-FLAT	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS
HM 65256 BLP-12	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 BLP-15	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 BLP-20	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS
HM 65256 BLSP-12	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 BLSP-15	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 BLSP-20	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS
HM 65256 BP-12	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 BP-15	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 BP-20	Hit	28-DIP	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS
HM 65256 BSP-12	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<120	<4	TTL-TS
HM 65256 BSP-15	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<150	<4	TTL-TS
HM 65256 BSP-20	Hit	28-TDIP	CMOS	0...+70	<357,5	<11	<200	<4	TTL-TS

62350 — 4096x4-Bit Cache Address Tag Comparator



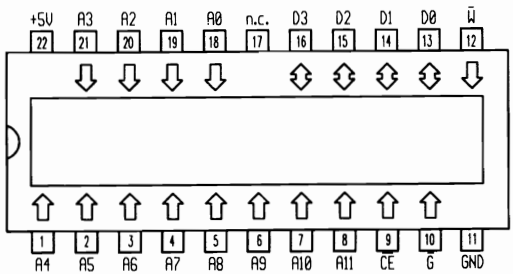
62350 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 62350 J-22	Mot	24-FLAT	CMOS	0...+70			<22		
MCM 62350 J-25	Mot	24-FLAT	CMOS	0...+70			<25		
MCM 62350 J-30	Mot	24-FLAT	CMOS	0...+70			<30		
MCM 62350 P-22	Mot	24-TDIP	CMOS	0...+70			<22		
MCM 62350 P-25	Mot	24-TDIP	CMOS	0...+70			<25		
MCM 62350 P-30	Mot	24-TDIP	CMOS	0...+70			<30		

62351 — 4096x4-Bit Cache Address Tag Comparator



62351 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 62351 J-22	Mot	24-FLAT	CMOS	0...+70			<22		
MCM 62351 J-25	Mot	24-FLAT	CMOS	0...+70			<25		
MCM 62351 J-30	Mot	24-FLAT	CMOS	0...+70			<30		
MCM 62351 P-22	Mot	24-TDIP	CMOS	0...+70			<22		
MCM 62351 P-25	Mot	24-TDIP	CMOS	0...+70			<25		
MCM 62351 P-30	Mot	24-TDIP	CMOS	0...+70			<30		

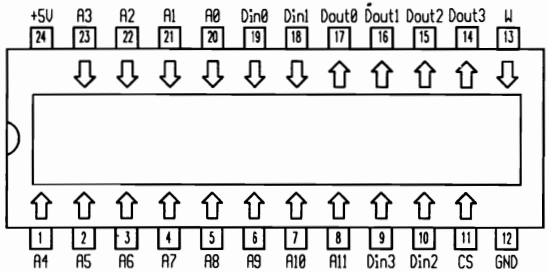
65770 — 4096x4-Bit static RAM



$\overline{CE}$	$\overline{G}$	$\overline{W}$	D_n	Mode
H	X	X	Hi-Z	deselect
L	X	L	data in	write
L	L	H	data out	read
L	H	H	Hi-Z	read

65770 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65770 E-5	Mhs	22-DIC	CMOS	0...+70	<495	<110	<15		TTL-TS
HM1 65770 F-5	Mhs	22-DIC	CMOS	0...+70	<495	<110	<20		TTL-TS
HM1 65770 H-5	Mhs	22-DIC	CMOS	0...+70	<495	<110	<25		TTL-TS
HM1 65770 K-2	Mhs	22-DIC	CMOS	-55...+125	<660	<110	<35		TTL-TS
HM1 65770 K-5	Mhs	22-DIC	CMOS	0...+70	<495	<110	<35		TTL-TS
HM1 65770 M-2	Mhs	22-DIC	CMOS	-55...+125	<660	<110	<40		TTL-TS
HM1 65770 M-5	Mhs	22-DIC	CMOS	0...+70	<495	<110	<40		TTL-TS
HM3 65770 E-5	Mhs	22-DIP	CMOS	0...+70	<495	<110	<15		TTL-TS
HM3 65770 F-5	Mhs	22-DIP	CMOS	0...+70	<495	<110	<20		TTL-TS
HM3 65770 H-5	Mhs	22-DIP	CMOS	0...+70	<495	<110	<25		TTL-TS
HM3 65770 K-2	Mhs	22-DIP	CMOS	-55...+125	<660	<110	<35		TTL-TS
HM3 65770 K-5	Mhs	22-DIP	CMOS	0...+70	<495	<110	<35		TTL-TS
HM3 65770 M-2	Mhs	22-DIP	CMOS	-55...+125	<660	<110	<40		TTL-TS
HM3 65770 M-5	Mhs	22-DIP	CMOS	0...+70	<495	<110	<40		TTL-TS

65772 — 4096x4-Bit static RAM

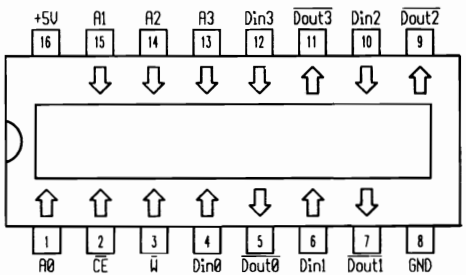


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

65772 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM1 65772 E-5	Mhs	24-DIC	CMOS	0...+70	<385	<27,5	<15		TTL-TS
HM1 65772 F-5	Mhs	24-DIC	CMOS	0...+70	<385	<27,5	<20		TTL-TS
HM1 65772 H-5	Mhs	24-DIC	CMOS	0...+70	<385	<27,5	<25		TTL-TS
HM1 65772 K-2	Mhs	24-DIC	CMOS	-55...+125	<495	<55	<35		TTL-TS
HM1 65772 K-5	Mhs	24-DIC	CMOS	0...+70	<385	<27,5	<35		TTL-TS
HM1 65772 M-2	Mhs	24-DIC	CMOS	-55...+125	<495	<55	<45		TTL-TS
HM1 65772 M-5	Mhs	24-DIC	CMOS	0...+70	<385	<27,5	<45		TTL-TS
HM3 65772 E-5	Mhs	24-DIP	CMOS	0...+70	<385	<27,5	<15		TTL-TS
HM3 65772 F-5	Mhs	24-DIP	CMOS	0...+70	<385	<27,5	<20		TTL-TS
HM3 65772 H-5	Mhs	24-DIP	CMOS	0...+70	<385	<27,5	<25		TTL-TS
HM3 65772 K-2	Mhs	24-DIP	CMOS	-55...+125	<495	<55	<35		TTL-TS
HM3 65772 K-5	Mhs	24-DIP	CMOS	0...+70	<385	<27,5	<35		TTL-TS
HM3 65772 M-2	Mhs	24-DIP	CMOS	-55...+125	<495	<55	<45		TTL-TS
HM3 65772 M-5	Mhs	24-DIP	CMOS	0...+70	<385	<27,5	<45		TTL-TS

74189

16x4-Bit RAM (bipolar)



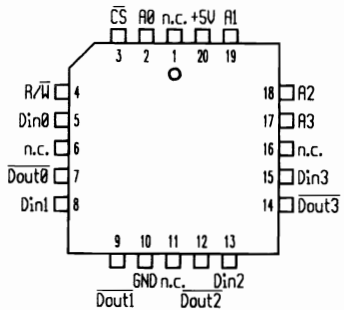
$\overline{CE}_{1...3}$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	H	disabled

74189 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S02 C	Amd	16-DIP	TTL	0...+75	<551		<35		TTL-OC
Am 27S03 C	Amd	16-DIP	TTL	0...+75	<656		<35		TTL-TS
Am 7489	Amd	16-DIP	TTL	0...+75	<525		<50		TTL-OC
Am 7489-1	Amd	16-DIP	TTL	0...+75	<525		<35		TTL-OC
Am 74S189	Amd	16-DIP	TTL	0...+75	<577		<50		TTL-TS
Am 74S289	Amd	16-DIP	TTL	0...+75	<577		<50		TTL-OC
DM 7489	Nsc	16-DIP	TTL	0...+70	<630		<60		TTL-OC
DM 8599	Nsc	16-DIP	TTL	0...+70	<630		<50		TTL-TS

74189 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 54S189	Nsc	16-DIP	TTL	-55...+125	<605		<50		TTL-TS
DM 54S189 A	Nsc	16-DIP	TTL	-55...+125	<550		<30		TTL-TS
DM 74LS189	Nsc	16-DIP	TTL	0...+70	<152		<80		TTL-TS
DM 74S189	Nsc	16-DIP	TTL	0...+70	<577		<35		TTL-TS
DM 74S189 A	Nsc	16-DIP	TTL	0...+70	<550		<25		TTL-TS
DM 74S189 A	Nsc	16-DIP	TTL	0...+70	<550		<25		TTL-TS
DM 74LS289	Nsc	16-DIP	TTL	0...+70	<152		<80		TTL-OC
DM 74S289	Nsc	16-DIP	TTL	0...+70	<551		<35		TTL-OC
IM 5501 C	Isi	16-DIP	TTL	0...+75	<525		<60		TTL-OC
L 6560	Mmi	16-DIP	TTL	0...+75	<252		<100		TTL-OC
L 6561	Mmi	16-DIP	TTL	0...+75	<252		<100		TTL-TS
MB 461	Fui	16-DIP	TTL	0...+75	<682		<60		TTL-TS
MM 74C89 D	Nsc	16-DIC	CMOS	-40...+85	<4,5		<800		TTL-OC
MM 74C89 N	Nsc	16-DIP	CMOS	-40...+85	<4,5		<800		TTL-OC
MM 74C989 J	Nsc	16-DIC	CMOS	-40...+85	<0,825	<16,5µ	<710		TTL-TS
MM 74C989 N	Nsc	16-DIP	CMOS	-40...+85	<0,825	<16,5µ	<710		TTL-TS
N 3101A D	Val	16-FLAT	TTL	0...+75	<551		<35		TTL-OC
N 3101A N	Val	16-DIP	TTL	0...+75	<551		<35		TTL-OC
N 7489	Sig	16-DIP	TTL	0...+75	<577		<50		TTL-OC
N 82S25 D	Val	16-FLAT	TTL	0...+75	<551		<50		TTL-OC
N 82S25 N	Val	16-DIP	TTL	0...+75	<551		<50		TTL-OC
N 74F189A D	Val	16-FLAT	TTL	0...+75	<367		<15		TTL-TS
N 74F189A N	Val	16-DIP	TTL	0...+75	<367		<15		TTL-TS
N 74F189 D	Val	16-FLAT	TTL	0...+75	<525		<20		TTL-TS
N 74F189 N	Val	16-DIP	TTL	0...+75	<525		<20		TTL-TS
N 74S189 D	Val	16-FLAT	TTL	0...+75	<577		<35		TTL-TS
N 74S189 N	Val	16-DIP	TTL	0...+75	<577		<35		TTL-TS
SN 7489 J	Tix	16-DIC	TTL	0...+70	<551		<60		TTL-OC
SN 7489 N	Tix	16-DIP	TTL	0...+70	<551		<60		TTL-OC
SN 54HC189 J	Tix	16-DIC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HCT189 J	Tix	16-DIC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54LS189 AJ	Tix	16-DIC	TTL	-55...+125	<330		<90		TTL-TS
SN 54S189 AJ	Tix	16-DIC	TTL	-55...+125	<605		<50		TTL-TS
SN 54LS289 AJ	Tix	16-DIC	TTL	-55...+125	<330		<90		TTL-OC
SN 54S289 AJ	Tix	16-DIC	TTL	-55...+125	<577		<50		TTL-OC
SN 74HC189 D	Tix	16-FLAT	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HC189 J	Tix	16-DIC	CMOS	-40...+85	<0,44		<55		TTL-TS

74189 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74HC189 N	Tix	16-DIP	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HCT189 D	Tix	16-FLAT	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HCT189 J	Tix	16-DIC	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HCT189 N	Tix	16-DIP	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74LS189 AJ	Tix	16-DIC	TTL	0...+70	<315		<80		TTL-TS
SN 74LS189 AN	Tix	16-DIP	TTL	0...+70	<315		<80		TTL-TS
SN 74189 N	Tix	16-DIP	TTL	0...+70	<577		<35		TTL-TS
SN 74S189 AJ	Tix	16-DIC	TTL	0...+70	<577		<35		TTL-TS
SN 74S189 AN	Tix	16-DIP	TTL	0...+70	<577		<35		TTL-TS
SN 74LS289 AJ	Tix	16-DIC	TTL	0...+70	<315		<80		TTL-OC
SN 74LS289 AN	Tix	16-DIP	TTL	0...+70	<315		<80		TTL-OC
SN 74289 N	Tix	16-DIP	TTL	0...+70	<551		<35		TTL-OC
SN 74S289 AJ	Tix	16-DIC	TTL	0...+70	<551		<35		TTL-OC
SN 74S289 AN	Tix	16-DIP	TTL	0...+70	<551		<35		TTL-OC
3101	Nsc	16-DIP	TTL	0...+75	<551		<60		TTL-OC
3101 A	Nsc	16-DIP	TTL	0...+75	<551		<35		TTL-OC
6560	Mmi	16-DIP	TTL	0...+75	<551		<50		TTL-OC
6561	Mmi	16-DIP	TTL	0...+75	<656		<50		TTL-TS
74LS89 D	Fch	16-DIC	TTL	0...+70	<210		37		TTL-OC
74LS89 P	Fch	16-DIP	TTL	0...+70	<210		37		TTL-OC
8225	Sig	16-DIP	TTL	0...+75	<577		<50		TTL-OC
34725	Fch	16-DIP	CMOS	-40...+85			<200		TTL-TS
93403 C	Tix	16-DIP	TTL	0...+75	<630		<60		TTL-OC
µPB 2289 D	Nec	16-DIP	TTL	0...+75	<604		<35		TTL-OC
µPB 2089 D	Nec	16-DIP	TTL	0...+75	<604		<60		TTL-OC
µPB 2289 D	Nip	16-DIC	TTL	0...+75	<604		<35		TTL-OC

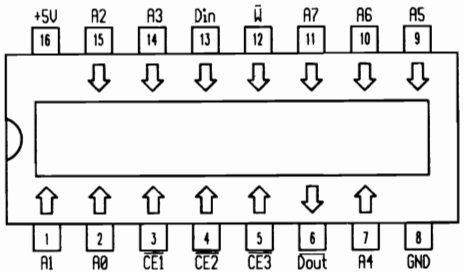
74189 — 16x4-Bit static RAM



$\overline{CE}_{1...3}$	$\overline{W}$	D_{In}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	H	disabled

74189 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54HC189 FH	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HC189 FK	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HCT189 FH	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HCT189 FK	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS

74200 — 256x1-Bit RAM (bipolar)

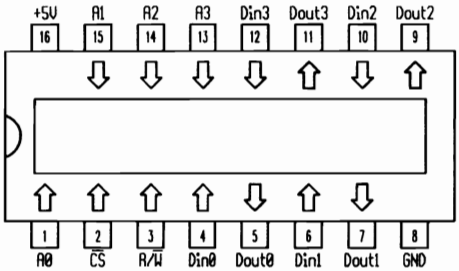


$\overline{CE}_{1...3}$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	Hi-Z	disabled

74200 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27LS00 A	Amd	16-DIP	TTL	0...+75	<604		<35		TTL-TS
Am 27LS00 C	Amd	16-DIP	TTL	0...+75	<367		<45		TTL-TS
DM 74S200	Nsc	16-DIP	TTL	0...+70	<683		<50		TTL-TS
IM 5523	Isi	16-DIP	TTL	0...+70	<656		<80		TTL-TS
IM 5523 A	Isi	16-DIP	TTL	0...+70	<656		<60		TTL-TS
L 6531	Mmi	16-DIP	TTL	0...+75	<446		<95		TTL-TS
N 74S200 F	Val	16-DIC	TTL	0...+75	<683		<50		TTL-TS
N 74S200 N	Sig	16-DIP	TTL	0...+75	<638		<50		TTL-TS

74200 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 74S201 F	Sig	16-DIC	TTL	0...+75	<683		<50		TTL-TS
N 74S201 N	Sig	16-DIP	TTL	0...+75	<683		<50		TTL-TS
S 54S200 F	Sig	16-DIC	TTL	-55...+125	<715		<70		TTL-TS
S 54S200 N	Sig	16-DIP	TTL	-55...+125	<715		<70		TTL-TS
S 54S201 F	Sig	16-DIC	TTL	-55...+125	<715		<70		TTL-TS
S 54S201 N	Sig	16-DIP	TTL	-55...+125	<715		<70		TTL-TS
SN 74S201 J	Tix	16-DIC	TTL	0...+70	<735		<65		TTL-TS
SN 74S201 N	Tix	16-DIP	TTL	0...+70	<735		<65		TTL-TS
SN 74S301 J	Tix	16-DIC	TTL	0...+70	<735		<65		TTL-OC
SN 74S301 N	Tix	16-DIP	TTL	0...+70	<735		<65		TTL-OC
3106-8	Int	16-DIP	TTL	0...+70	<683		<80		TTL-TS
3106 A	Int	16-DIP	TTL	0...+70	<683		<60		TTL-TS
3106 C	Int	16-DIC	TTL	0...+70	<683		<80		TTL-TS
3106 P	Int	16-DIP	TTL	0...+70	<683		<80		TTL-TS
6531	Mmi	16-DIP	TTL	0...+75	<683		<55		TTL-TS
µPB 2200 D	Nip	16-DIP	TTL	0...+75	<604		<50		TTL-TS
µPB 2202 D	Nip	16-DIC	TTL	0...+75	<394		<65		TTL-TS

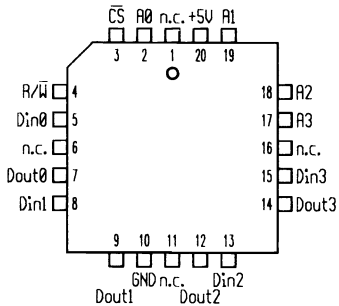
74219 — 16x4-Bit RAM (bipolar)



$\overline{CE}_{1...3}$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	H	disabled

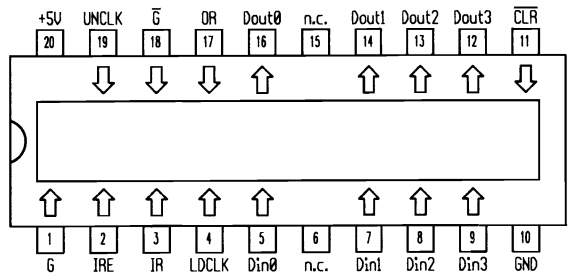
74219 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 75S06 J	Nsc	16-DIC	TTL	-55...+125	<550		<50		TTL-OC
DM 75S07 AJ	Nsc	16-DIC	TTL	-55...+125	<550		<30		TTL-TS
DM 75S07 J	Nsc	16-DIC	TTL	-55...+125	<550		<50		TTL-TS
DM 85S06 J	Nsc	16-DIC	TTL	0...+70	<525		<35		TTL-OC
DM 85S06 N	Nsc	16-DIP	TTL	0...+70	<525		<35		TTL-OC
DM 85S07 AJ	Nsc	16-DIC	TTL	0...+70	<525		<25		TTL-TS
DM 85S07 AN	Nsc	16-DIP	TTL	0...+70	<525		<25		TTL-TS
DM 85S07 J	Nsc	16-DIC	TTL	0...+70	<525		<35		TTL-TS
DM 85S07 N	Nsc	16-DIP	TTL	0...+70	<525		<35		TTL-TS
N 74F219 D	Phi	16-FLAT	TTL	0...+70	<385		<10,5		TTL-TS
N 74F219 N	Phi	16-DIP	TTL	0...+70	<385		<10,5		TTL-TS
SN 54HC219 J	Tix	16-DIC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HCT219 J	Tix	16-DIC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54LS219 AJ	Tix	16-DIC	TTL	-55...+125	<330		<90		TTL-TS
SN 54LS319 AJ	Tix	16-DIC	TTL	-55...+125	<330		<90		TTL-OC
SN 74HC219 D	Tix	16-FLAT	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HC219 J	Tix	16-DIC	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HC219 N	Tix	16-DIP	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HCT219 D	Tix	16-FLAT	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HCT219 J	Tix	16-DIC	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74HCT219 N	Tix	16-DIP	CMOS	-40...+85	<0,44		<55		TTL-TS
SN 74LS219 AJ	Tix	16-DIC	TTL	0...+70	<315		<80		TTL-TS
SN 74LS219 AN	Tix	16-DIP	TTL	0...+70	<315		<80		TTL-TS
SN 74LS319 AJ	Tix	16-DIC	TTL	0...+70	<315		<80		TTL-OC
SN 74LS319 AN	Tix	16-DIP	TTL	0...+70	<315		<80		TTL-OC

74219 — 16x4-Bit static RAM



$\overline{CE}_{1...3}$	$\overline{W}$	D_{In}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	H	disabled

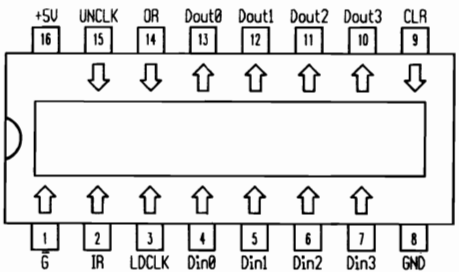
74222 — 16 words x 4-Bit asynchronous FIFO



74219 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54HC219 FH	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HC219 FK	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HCT219 FH	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS
SN 54HCT219 FK	Tix	20-PLCC	CMOS	-55...+125	<0,88		<55		TTL-TS

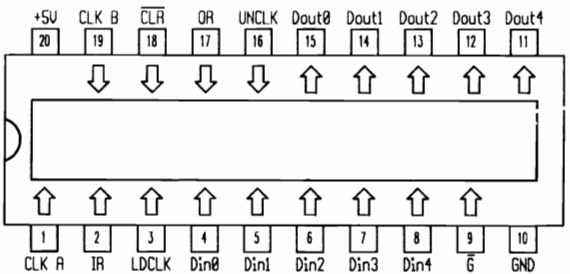
74222 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54LS222 J	Tix	20-DIC	TTL	-55...+125	<489				TTL-TS
SN 54LS227 J	Tix	20-DIC	TTL	-55...+125	<489				TTL-OC
SN 74LS222 J	Tix	20-DIC	TTL	0...+70	<467				TTL-TS
SN 74LS222 N	Tix	20-DIP	TTL	0...+70	<467				TTL-TS
SN 74LS227 J	Tix	20-DIC	TTL	0...+70	<467				TTL-OC
SN 74LS227 N	Tix	20-DIP	TTL	0...+70	<467				TTL-OC

74224 — 16 words x 4-Bit FIFO



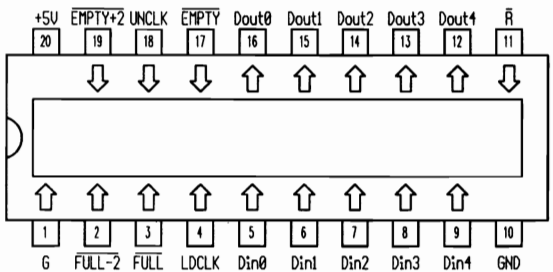
74224 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54LS224 J	Tix	16-DIC	TTL	-55...+125	<489				TTL-TS
SN 54LS228 J	Tix	16-DIC	TTL	-55...+125	<489				TTL-OC
SN 74LS224 J	Tix	16-DIC	TTL	0...+70	<467				TTL-TS
SN 74LS224 N	Tix	16-DIP	TTL	0...+70	<467				TTL-TS
SN 74LS228 J	Tix	16-DIC	TTL	0...+70	<467				TTL-OC
SN 74LS228 N	Tix	16-DIP	TTL	0...+70	<467				TTL-OC

74225 — 16 words x 5-Bit asynchronous FIFO



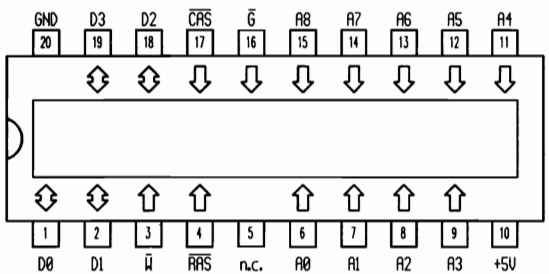
74225 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74S225 J	Tix	20-DIC	TTL	0...+70	<630				TTL-TS
SN 74S225 N	Tix	20-DIP	TTL	0...+70	<630				TTL-TS

74229 — 16 words x 5-Bit asynchronous FIFO



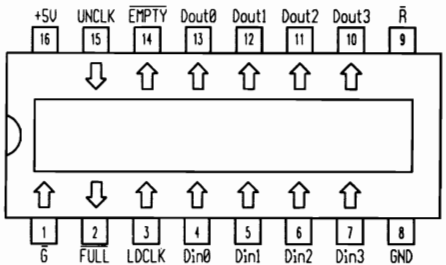
74229 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS229 AJ	Tix	20-DIC	TTL	-55...+125	<825		<35		TTL-TS
SN 74ALS229 ADW	Tix	20-FLAT	TTL	0...+70	<770		<29		TTL-TS
SN 74ALS229 AN	Tix	20-DIP	TTL	0...+70	<770		<29		TTL-TS

74229 — 16 words x 5-Bit asynchronous FIFO



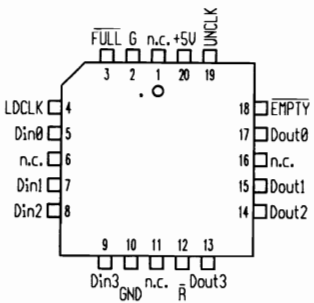
74229 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS229 AFK	Tix	20-PLCC	TTL	-55...+125	<825		<35		TTL-TS
SN 74ALS229 AFN	Tix	20-PLCC	TTL	0...+70	<770		<29		TTL-TS

74232 — 16 words x 4-Bit asynchronous FIFO



74232 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS232 AJ	Tix	16-DIC	TTL	-55...+125	<688		<50		TTL-TS
SN 74ALS232 AD	Tix	16-FLAT	TTL	0...+70	<688		<46		TTL-TS
SN 74ALS232 AN	Tix	16-DIP	TTL	0...+70	<688		<46		TTL-TS

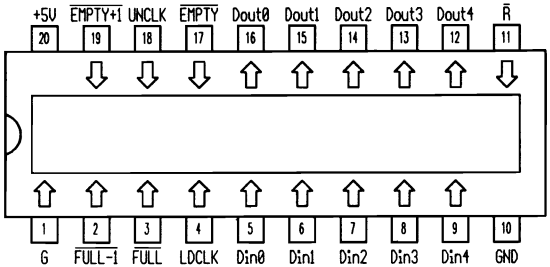
74232 — 16 words x 4-Bit asynchronous FIFO

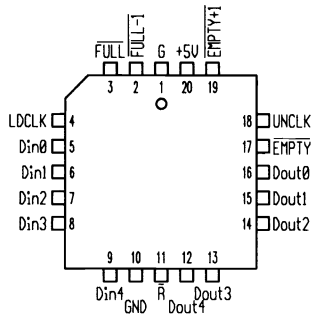


74232 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS232 AFK	Tix	20-PLCC	TTL	-55...+125	<688		<50		TTL-TS
SN 74ALS232 AFN	Tix	20-PLCC	TTL	0...+70	<688		<46		TTL-TS

74233	16 words x 5-Bit asynchronous FIFO

74233	16 words x 5-Bit asynchronous FIFO

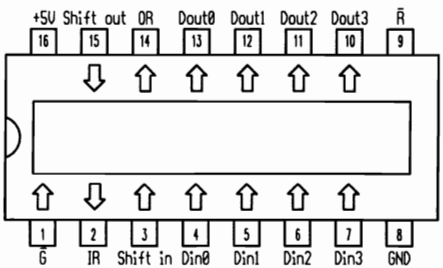




74233 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS233 AJ	Tix	20-DIC	TTL	-55...+125	<787		<52		TTL-TS
SN 74ALS233 ADW	Tix	20-FLAT	TTL	0...+70	<732		<48		TTL-TS
SN 74ALS233 AN	Tix	20-DIP	TTL	0...+70	<732		<48		TTL-TS

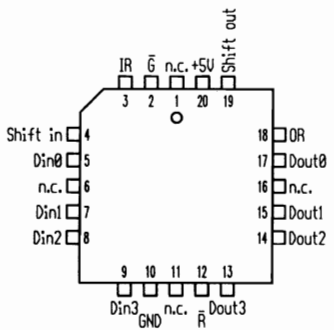
74233 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS233 AFK	Tix	20-PLCC	TTL	-55...+125	<787		<52		TTL-TS
SN 74ALS233 AFN	Tix	20-PLCC	TTL	0...+70	<732		<48		TTL-TS

74234 — 64 words x 4-Bit asynchronous FIFO



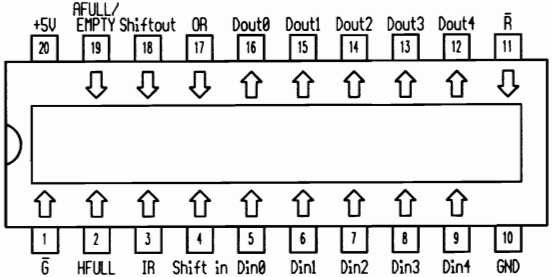
74234 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS234 J	Tix	16-DIC	TTL	-55...+125	<869		<1200		TTL-TS
SN 74ALS234 D	Tix	16-FLAT	TTL	0...+70	<814		<1000		TTL-TS
SN 74ALS234 N	Tix	16-DIP	TTL	0...+70	<814		<1000		TTL-TS

74234 — 64 words x 4-Bit asynchronous FIFO



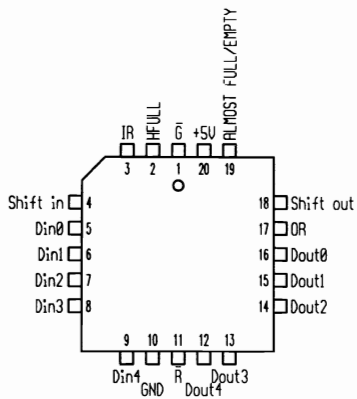
74234 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS234 FK	Tix	20-PLCC	TTL	-55...+125	<869		<1200		TTL-TS
SN 74ALS234 FN	Tix	20-PLCC	TTL	0...+70	<814		<1000		TTL-TS

74235 — 64 words x 5-Bit asynchronous FIFO



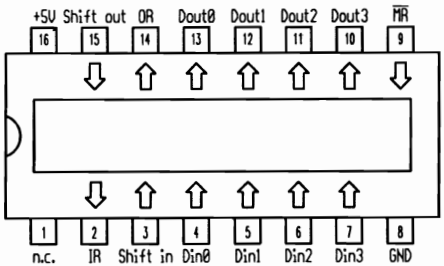
74235 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS235 J	Tix	20-DIC	TTL	-55...+125	<990		<1200		TTL-TS
SN 74ALS235 DW	Tix	20-FLAT	TTL	0...+70	<935		<1000		TTL-TS
SN 74ALS235 N	Tix	20-DIP	TTL	0...+70	<935		<1000		TTL-TS

74235 — 64 words x 5-Bit asynchronous FIFO



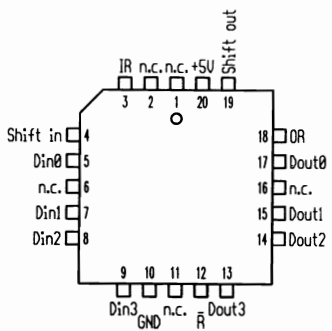
74235 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS235 FK	Tix	20-PLCC	TTL	-55...+125	<990		<1200		TTL-TS
SN 74ALS235 FN	Tix	20-PLCC	TTL	0...+70	<935		<1000		TTL-TS

74236 — 64 words x 4-Bit asynchronous FIFO



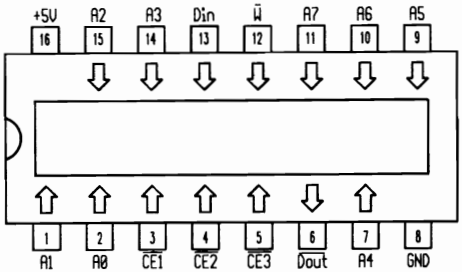
74236 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS236 J	Tix	16-DIC	TTL	-55...+125	<853		<1200		TTL-TS
SN 74ALS236 D	Tix	16-FLAT	TTL	0...+70	<798		<1000		TTL-TS
SN 74ALS236 N	Tix	16-DIP	TTL	0...+70	<798		<1000		TTL-TS

74236 — 64 words x 4-Bit asynchronous FIFO



74236 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 54ALS236 FK	Tix	20-PLCC	TTL	-55...+125	<853		<1200		TTL-TS
SN 74ALS236 FN	Tix	20-PLCC	TTL	0...+70	<798		<1000		TTL-TS

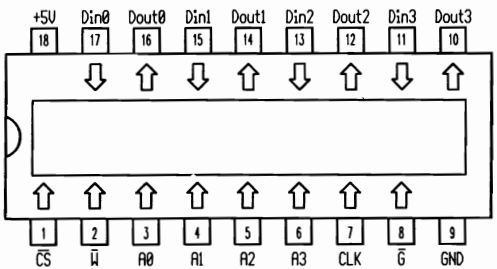
74301 — 256x1-Bit RAM (bipolar)



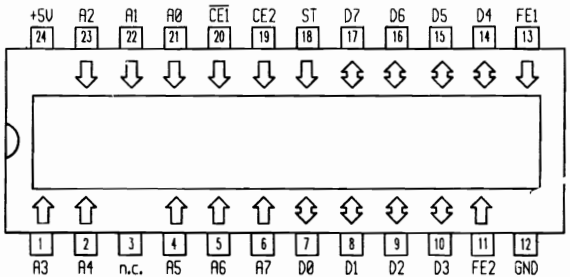
$\overline{CE}_{1...3}$	$\overline{W}$	D_{in}	D_{out}	Mode
L	H	X	stored $\overline{data}$	read
L	L	L	H	write »0«
L	L	H	L	write »1«
H	X	X	H	disabled

74301 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27LS01	Amd	16-DIP	TTL	0...+75	<367		<45		TTL-OC
Am 27LS01 A	Amd	16-DIP	TTL	0...+75	<604		<35		TTL-OC
Am 27LS01 C	Amd	16-DIP	TTL	0...+75	<367		<45		TTL-OC
DM 74S206	Nsc	16-DIP	TTL	0...+70	<683		<60		TTL-OC
IM 5503	Isi	16-DIP	TTL	0...+70	<656		<80		TTL-OC
IM 5503 A	Isi	16-DIP	TTL	0...+70	<656		<60		TTL-OC
IM 5533	Isi	16-DIP	TTL	0...+70	<656		<80		TTL-OC
IM 5533 A	Isi	16-DIP	TTL	0...+70	<656		<60		TTL-OC
L 6530	Mmi	16-DIP	TTL	0...+75	<446		<95		TTL-OC
N 74LS301 D	Val	16-FLAT	TTL	0...+75	<367		<40		TTL-OC
N 74LS301 N	Val	16-DIP	TTL	0...+75	<367		<40		TTL-OC
N 74S301 D	Val	16-FLAT	TTL	0...+75	<682		<50		TTL-OC
N 74S301 F	Sig	16-DIC	TTL	0...+75	<638		<50		TTL-OC
N 74S301 N	Val	16-DIP	TTL	0...+75	<682		<50		TTL-OC
S 54S301 F	Sig	16-DIC	TTL	-55...+125	<715		<70		TTL-OC
S 54S301 N	Sig	16-DIP	TTL	-55...+125	<715		<70		TTL-OC
SN 74S301 N	Tix	16-DIP	TTL	0...+70	<735		<65		TTL-OC
3107-8	Int	16-DIP	TTL	0...+70	<683		<80		TTL-OC
3107 A	Int	16-DIP	TTL	0...+70	<683		<60		TTL-OC
3107 C	Int	16-DIC	TTL	0...+70	<683		<80		TTL-OC
3107 P	Int	16-DIP	TTL	0...+70	<683		<80		TTL-OC
6530	Mmi	16-DIP	TTL	0...+75	<683		<55		TTL-OC
93411A DC	Fch	16-DIC	TTL	0...+75	475		<45		TTL-OC
93411A DC	Fch	16-DIC	TTL	0...+75	475		<45		TTL-OC
93411 DC	Fch	16-DIC	TTL	0...+75	475		<55		TTL-OC
93411 DM	Fch	16-DIP	TTL	-55...+125	475		<65		TTL-OC
93411A FC	Fch	16-FLAT	TTL	0...+75	475		<45		TTL-OC
93411 FC	Fch	16-FLAT	TTL	0...+75	475		<55		TTL-OC
93411 FM	Fch	16-FLAT	TTL	-55...+125	475		<65		TTL-OC
93411A PC	Fch	16-DIP	TTL	0...+75	475		<45		TTL-OC
93411 PC	Fch	16-DIP	TTL	0...+75	475		<55		TTL-OC
µPB 2206 D	Nip	16-DIC	TTL	0...+75	<604		<50		TTL-OC

74410 — 16x4-Bit RAM (bipolar)



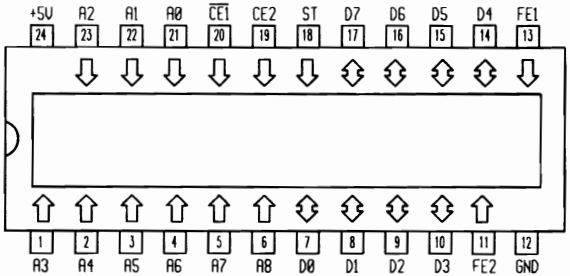
82114 — 256x8-Bit PROM



74410 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $	t_{aa} ns	t_{ref} ms	Output
N 74F410 N	Phi	18-DIP	TTL	0...+70	<385	<19,5		TTL-TS

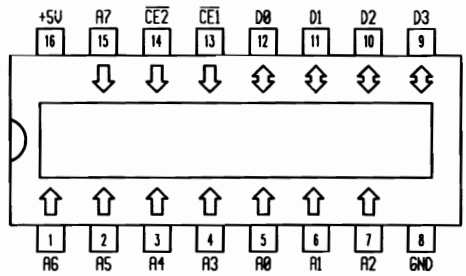
82114 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $	t_{aa} ns	t_{ref} ms	Output
N 82S114 F	Sig	24-DIC	TTL	0...+75	<919	<60		TTL-TS
N 82S114 N	Sig	24-DIP	TTL	0...+75	<919	<60		TTL-TS
S 82S114 F	Sig	24-DIC	TTL	-55...+125	<1017	<90		TTL-TS

82115 — 256x8-Bit PROM



82115 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S115 F	Sig	24-DIC	TTL	0...+75	<919		<60		TTL-TS
N 82S115 N	Val	24-DIP	TTL	0...+75	<919		<60		TTL-TS
S 82S115 F	Sig	24-DIC	TTL	-55...+125	<1017		<90		TTL-TS

82126 — 256x4-Bit PROM

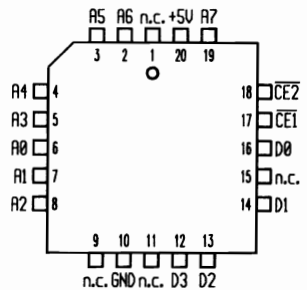


82126 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S10	Amd	16-DIP	TTL	0...+75	<577		<60		TTL-OC
Am 27S11	Amd	16-DIC	TTL	0...+75	<630		<60		TTL-TS
Am 27S20	Amd	16-DIP	TTL	0...+75	<682		<45		TTL-OC
Am 27S20 A	Amd	16-DIP	TTL	0...+75	<682		<30		TTL-OC
Am 27S21	Amd	16-DIP	TTL	0...+75	<682		<45		TTL-TS
Am 27S21 A	Amd	16-DIP	TTL	0...+75	<682		<30		TTL-TS
DM 54S287 AJ	Nsc	16-DIC	TTL	-55...+125	<715		<40		TTL-TS
DM 54S287 J	Nsc	16-DIC	TTL	-55...+125	<715		<60		TTL-TS

82126 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output	82126 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
DM 54S387 AJ	Nsc	16-DIC	TTL	-55...+125	<715	<40		TTL-OC	**TBP 14S10 J**	Tix	16-DIC	TTL	0...+70	<709	<65		TTL-TS
DM 54S387 J	Nsc	16-DIC	TTL	-55...+125	<715	<60		TTL-OC	**TBP 14S10 MJ**	Tix	16-DIC	TTL	-55...+125	<709	<75		TTL-TS
DM 74S287 AJ	Nsc	16-DIC	TTL	0...+70	<715	<30		TTL-TS	**TBP 14S10 N**	Tix	16-DIP	TTL	0...+70	<709	<65		TTL-TS
DM 74S287 AN	Nsc	16-DIP	TTL	0...+70	<715	<30		TTL-TS	**TBP 24SA10 J**	Tix	16-DIC	TTL	0...+75	<525	<65		TTL-OC
DM 74S287 J	Nsc	16-DIC	TTL	0...+70	<715	<50		TTL-TS	**TBP 24SA10 MJ**	Tix	16-DIC	TTL	-55...+125	<550	<75		TTL-OC
DM 74S287 N	Nsc	16-DIP	TTL	0...+70	<715	<50		TTL-TS	**TBP 24SA10 N**	Tix	16-DIP	TTL	0...+75	<525	<65		TTL-OC
DM 74S387 AJ	Nsc	16-DIC	TTL	0...+70	<715	<30		TTL-OC	**TBP 24S10 J**	Tix	16-DIC	TTL	0...+70	<525	<55		TTL-TS
DM 74S387 AN	Nsc	16-DIP	TTL	0...+70	<715	<30		TTL-OC	**TBP 24S10 MJ**	Tix	16-DIC	TTL	-55...+125	<550	<75		TTL-TS
DM 74S387 J	Nsc	16-DIC	TTL	0...+70	<715	<50		TTL-OC	**TBP 24S10 N**	Tix	16-DIP	TTL	0...+70	<525	<55		TTL-TS
DM 74S387 N	Nsc	16-DIP	TTL	0...+70	<715	<50		TTL-OC	**3601**	Int	16-DIP	TTL	0...+75	<682	<70		TTL-OC
IM 5603 A	Isi	16-DIP	TTL	0...+75	<682	<60		TTL-OC	**3601-1**	Int	16-DIP	TTL	0...+75	<682	<50		TTL-OC
IM 56S03	Isi	16-DIP	TTL	0...+75	<682	<50		TTL-OC	**3621**	Int	16-DIP	TTL	0...+75	<682	<70		TTL-TS
IM 5623	Isi	16-DIP	TTL	0...+75	<682	<60		TTL-TS	**3621-1**	Int	16-DIP	TTL	0...+75	<682	<50		TTL-TS
IM 56S23	Isi	16-DIP	TTL	0...+75	<682	<50		TTL-TS	**6300-1**	Mmi	16-DIC	TTL	0...+70	<682	<55		TTL-OC
M 54700	Mit	16-DIP	TTL	0...+75	<656	<60		TTL-OC	**6301-1**	Mmi	16-DIC	TTL	0...+70	<682	<55		TTL-TS
MB 7052	Fui	16-DIP	TTL	0...+75	<682	<70		TTL-TS	**63LS140**	Mmi	16-DIP	TTL	0...+75	<341	<55		TTL-OC
MB 7057	Fui	16-DIP	TTL	0...+75	<682	<70		TTL-OC	**63PS140**	Mmi	16-DIP	TTL	0...+75	409 / <105	27		TTL-OC
MSL 8520 A	Oki	16-DIC	TTL	0...+70	<550	<100		TTL-OC	**63S140**	Mmi	16-DIP	TTL	0...+75	<630	<45		TTL-OC
MSL 8521 A	Oki	16-DIC	TTL	0...+70	<605	<100		TTL-TS	**63LS141**	Mmi	16-DIP	TTL	0...+75	<341	<55		TTL-TS
N 82S27 F	Sig	16-DIC	TTL	0...+75	$0,6	<40		TTL-OC	**63PS141**	Mmi	16-DIP	TTL	0...+75	409 / <131	27		TTL-TS
N 82S126 D	Val	16-FLAT	TTL	0...+75	<630	<50		TTL-OC	**63S141**	Mmi	16-DIP	TTL	0...+75	<630	<45		TTL-TS
N 82S126A D	Val	16-FLAT	TTL	0...+75	<630	<30		TTL-OC	**93417 DC**	Fch	16-DIC	TTL	0...+75	475	<45		TTL-OC
N 82S126 F	Sig	16-DIC	TTL	0...+75	<630	<50		TTL-OC	**93417 DM**	Fch	16-DIC	TTL	-55...+125	475	<60		TTL-OC
N 82S126 N	Val	16-DIP	TTL	0...+75	<630	<50		TTL-OC	**93417 FC**	Fch	16-FLAT	TTL	0...+75	475	<45		TTL-OC
N 82S126A N	Val	16-DIP	TTL	0...+75	<630	<30		TTL-OC	**93417 FM**	Fch	16-FLAT	TTL	-55...+125	475	<60		TTL-OC
N 82S129 D	Val	16-FLAT	TTL	0...+75	<630	<50		TTL-TS	**93417 PC**	Fch	16-DIP	TTL	0...+75	475	<45		TTL-OC
N 82S129A D	Val	16-FLAT	TTL	0...+75	<630	<27		TTL-TS	**93427 DC**	Fch	16-DIC	TTL	0...+75	<814	<45		TTL-TS
N 82S129 F	Sig	16-DIC	TTL	0...+75	<630	<50		TTL-TS	**93427 DM**	Fch	16-DIC	TTL	-55...+125	<935	<60		TTL-TS
N 82S129 N	Val	16-DIP	TTL	0...+75	<630	<50		TTL-TS	**93427 FC**	Fch	16-FLAT	TTL	0...+75	475	<45		TTL-TS
N 82S129A N	Val	16-DIP	TTL	0...+75	<630	<27		TTL-TS	**93427 FM**	Fch	16-FLAT	TTL	-55...+125	475	<60		TTL-TS
SN 74S287 J	Tix	16-DIC	TTL	0...+70	<709	<65		TTL-TS	**93427 PC**	Fch	16-DIP	TTL	0...+75	475	<45		TTL-TS
SN 74S287 N	Tix	16-DIP	TTL	0...+70	<709	<65		TTL-TS	**µPB 403 C**	Nec	16-DIC	TTL	-25...+75	<715	<60		TTL-OC
SN 74S387 J	Tix	16-DIC	TTL	0...+70	<709	<65		TTL-OC	**µPB 403 C-1**	Nec	16-DIC	TTL	-25...+75	<715	<45		TTL-OC
SN 74S387 N	Tix	16-DIP	TTL	0...+70	<709	<65		TTL-OC	**µPB 403 C-2**	Nec	16-DIC	TTL	-25...+75	<715	<35		TTL-OC
TBP 14SA10 J	Tix	16-DIC	TTL	0...+70	<709	<65		TTL-OC	**µPB 403 D**	Nec	16-DIP	TTL	-25...+75	<715	<60		TTL-OC
TBP 14SA10 MJ	Tix	16-DIC	TTL	-55...+125	<709	<75		TTL-OC	**µPB 403 D-1**	Nec	16-DIP	TTL	-25...+75	<715	<45		TTL-OC
TBP 14SA10 N	Tix	16-DIP	TTL	0...+70	<709	<65		TTL-OC	**µPB 403 D-2**	Nec	16-DIP	TTL	-25...+75	<715	<35		TTL-OC

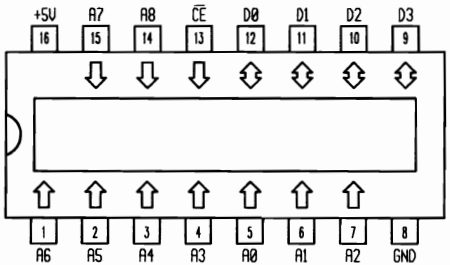
82126 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
µPB 423 C	Nec	16-DIC	TTL	-25...+75	<715	<60		TTL-TS
µPB 423 C-1	Nec	16-DIC	TTL	-25...+75	<715	<45		TTL-TS
µPB 423 C-2	Nec	16-DIC	TTL	-25...+75	<715	<35		TTL-TS
µPB 423 D	Nec	16-DIP	TTL	-25...+75	<715	<60		TTL-TS
µPB 423 D-1	Nec	16-DIP	TTL	-25...+75	<715	<45		TTL-TS
µPB 423 D-2	Nec	16-DIP	TTL	-25...+75	<715	<35		TTL-TS

82126 — **256x4-Bit PROM**



82126 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
DM 74S287 AV	Nsc	20-FLAT	TTL	0...+70	<715	<30		TTL-TS
DM 74S287 V	Nsc	20-FLAT	TTL	0...+70	<715	<50		TTL-TS
DM 74S387 AV	Nsc	20-FLAT	TTL	0...+70	<715	<30		TTL-OC
DM 74S387 V	Nsc	20-FLAT	TTL	0...+70	<715	<50		TTL-OC
N 82S126 A	Val	20-PLCC	TTL	0...+75	<630	<50		TTL-OC
N 82S126A A	Val	20-PLCC	TTL	0...+75	<630	<30		TTL-OC
N 82S129 A	Val	20-PLCC	TTL	0...+75	<630	<50		TTL-TS
N 82S129A A	Val	20-PLCC	TTL	0...+75	<630	<27		TTL-TS

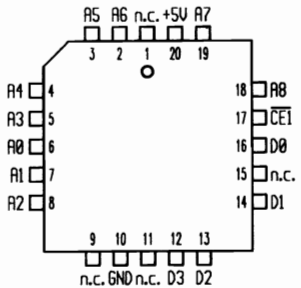
82130 — 512x4-Bit PROM



82130 Type	Man	Case	Techn.	TU°C	Ptyp mW / P standby mW ($mW/bit)	taa ns	tref ms	Output
Am 27S12	Amd	16-DIP	TTL	0...+75	<682	<50		TTL-OC
Am 27S12 A	Amd	16-DIP	TTL	0...+75	<682	<30		TTL-OC
Am 27S13	Amd	16-DIP	TTL	0...+75	<682	<50		TTL-TS
Am 27S13 A	Amd	16-DIP	TTL	0...+75	<682	<30		TTL-TS
DM 54S570 AJ	Nsc	16-DIC	TTL	-55...+125	<715	<60		TTL-OC
DM 54S570 J	Nsc	16-DIC	TTL	-55...+125	<715	<65		TTL-OC
DM 54S571 AJ	Nsc	16-DIC	TTL	-55...+125	<715	<60		TTL-TS
DM 54S571 BJ	Nsc	16-DIC	TTL	-55...+125	<715	<50		TTL-TS
DM 54S571 J	Nsc	16-DIC	TTL	-55...+125	<715	<65		TTL-TS
DM 74S570 AJ	Nsc	16-DIC	TTL	0...+70	<715	<45		TTL-OC
DM 74S570 AN	Nsc	16-DIP	TTL	0...+70	<715	<45		TTL-OC
DM 74S570 J	Nsc	16-DIC	TTL	0...+70	<715	<55		TTL-OC
DM 74S570 N	Nsc	16-DIP	TTL	0...+70	<715	<55		TTL-OC
DM 74S571 AJ	Nsc	16-DIC	TTL	0...+70	<715	<45		TTL-TS
DM 74S571 AN	Nsc	16-DIP	TTL	0...+70	<715	<45		TTL-TS
DM 74S571 BJ	Nsc	16-DIC	TTL	0...+70	<715	<35		TTL-TS
DM 74S571 BN	Nsc	16-DIP	TTL	0...+70	<715	<35		TTL-TS
DM 74S571 J	Nsc	16-DIC	TTL	0...+70	<715	<55		TTL-TS
DM 74S571 N	Nsc	16-DIP	TTL	0...+70	<715	<55		TTL-TS
IM 5604	Isi	16-DIP	TTL	0...+75	<735	<70		TTL-OC
IM 56S04	Isi	16-DIP	TTL	0...+75	<735	<50		TTL-OC
IM 5624	Isi	16-DIP	TTL	0...+75	<735	<70		TTL-TS
IM 56S24	Isi	16-DIP	TTL	0...+75	<735	<50		TTL-TS
MB 7053	Fui	16-DIC	TTL	0...+75	<735	<70		TTL-TS
MB 7058	Fui	16-DIC	TTL	0...+75	<735	<70		TTL-OC
MCM 7620	Mot	16-DIC	TTL	0...+70	<525	<70		TTL-OC
MCM 7621	Mot	16-DIC	TTL	0...+70	<525	<70		TTL-TS
N 82S130 D	Val	16-FLAT	TTL	0...+75	<735	<50		TTL-OC
N 82S130A D	Val	16-FLAT	TTL	0...+75	<735	<33		TTL-OC
N 82S130 F	Sig	16-DIC	TTL	0...+75	<735	<60		TTL-OC
N 82S130 N	Val	16-DIP	TTL	0...+75	<735	<50		TTL-OC
N 82S130A N	Val	16-DIP	TTL	0...+75	<735	<33		TTL-OC
N 82S131 D	Val	16-FLAT	TTL	0...+75	<735	<50		TTL-TS
N 82S131A D	Val	16-FLAT	TTL	0...+75	<735	<30		TTL-TS
N 82S131 F	Sig	16-DIC	TTL	0...+75	<735	<60		TTL-TS
N 82S131 N	Val	16-DIP	TTL	0...+75	<735	<50		TTL-TS
N 82S131A N	Val	16-DIP	TTL	0...+75	<735	<30		TTL-TS
S 82S130 F	Sig	16-DIC	TTL	-55...+125	<770	<70		TTL-OC
S 82S131 F	Sig	16-DIC	TTL	-55...+125	<770	<70		TTL-TS
3602	Int	16-DIP	TTL	0...+75	<735	<70		TTL-OC
3602 A	Int	16-DIP	TTL	0...+75	<735	<70		TTL-OC
3602 A-2	Int	16-DIP	TTL	0...+75	<735	<60		TTL-OC
3622	Int	16-DIP	TTL	0...+75	<735	<70		TTL-TS
3622 A	Int	16-DIP	TTL	0...+75	<735	<70		TTL-TS
3622 A-2	Int	16-DIP	TTL	0...+75	<735	<60		TTL-TS

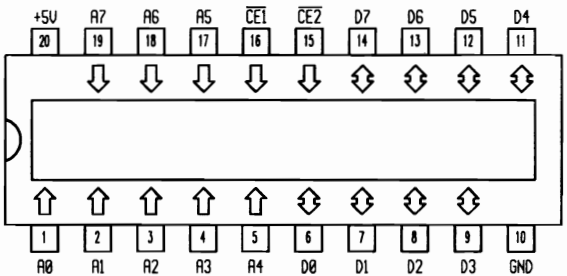
82130 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
6305-1	Mmi	16-DIC	TTL	0...+75	<628		<60		TTL-OC
6306-1	Mmi	16-DIC	TTL	0...+75	<628		<60		TTL-TS
63LS240	Mmi	16-DIP	TTL	0...+75	<367		<60		TTL-OC
63PS240	Mmi	16-DIP	TTL	0...+75	446	<105	30		TTL-OC
63S240	Mmi	16-DIP	TTL	0...+75	<628		<45		TTL-OC
63LS241	Mmi	16-DIP	TTL	0...+75	<367		<60		TTL-TS
63PS241	Mmi	16-DIP	TTL	0...+75	446	<131	30		TTL-TS
63S241	Mmi	16-DIP	TTL	0...+75	<628		<45		TTL-TS
93436 DC	Fch	16-DIC	TTL	0...+75	475		<50		TTL-TS
93436 DM	Fch	16-DIC	TTL	-55...+125	475		<60		TTL-TS
93436 FC	Fch	16-FLAT	TTL	0...+75	475		<50		TTL-TS
93436 FM	Fch	16-FLAT	TTL	-55...+125	475		<60		TTL-TS
93436 PC	Fch	16-DIP	TTL	0...+75	475		<50		TTL-TS
93446 DC	Fch	16-DIC	TTL	0...+75	475		<50		TTL-TS
93446 DM	Fch	16-DIC	TTL	-55...+125	475		<60		TTL-TS
93446 FC	Fch	16-FLAT	TTL	0...+75	475		<50		TTL-TS
93446 FM	Fch	16-FLAT	TTL	-55...+125	475		<60		TTL-TS
93446 PC	Fch	16-DIP	TTL	0...+75	475		<50		TTL-TS
µPB 412 C	Nec	16-DIP	TTL	-25...+75	<715		<45		TTL-TS
µPB 412 C-1	Nec	16-DIP	TTL	-25...+75	<715		<35		TTL-TS
µPB 412 D	Nec	16-DIC	TTL	-25...+75	<715		<45		TTL-TS
µPB 412 D-1	Nec	16-DIC	TTL	-25...+75	<715		<35		TTL-TS

82130 — 512x4-Bit PROM



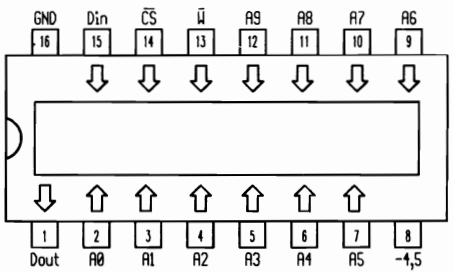
82130 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 74S570 AV	Nsc	20-FLAT	TTL	0...+70	<715		<45		TTL-OC
DM 74S570 V	Nsc	20-FLAT	TTL	0...+70	<715		<55		TTL-OC
DM 74S571 AV	Nsc	20-FLAT	TTL	0...+70	<715		<45		TTL-TS
DM 74S571 BV	Nsc	20-FLAT	TTL	0...+70	<715		<35		TTL-TS
DM 74S571 V	Nsc	20-FLAT	TTL	0...+70	<715		<55		TTL-TS
N 82S130 A	Val	20-PLCC	TTL	0...+75	<735		<50		TTL-OC
N 82S130A A	Val	20-PLCC	TTL	0...+75	<735		<33		TTL-OC
N 82S131 A	Val	20-PLCC	TTL	0...+75	<735		<50		TTL-TS
N 82S131A A	Val	20-PLCC	TTL	0...+75	<735		<30		TTL-TS

82135 — 256x8-Bit PROM



82135 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPB 421 C	Nec	16-DIP	TTL	-25...+75	<770		<50		TTL-TS
µPB 421 C-1	Nec	16-DIP	TTL	-25...+75	<770		<40		TTL-TS
µPB 421 D	Nec	16-DIC	TTL	-25...+75	<770		<50		TTL-TS
µPB 421 D-1	Nec	16-DIC	TTL	-25...+75	<770		<40		TTL-TS

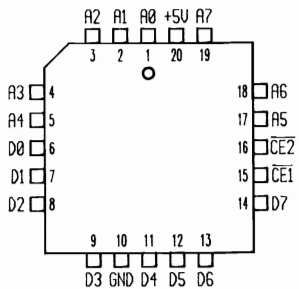
82135 — 256x8-Bit PROM



82135 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 54LS471 J	Nsc	20-DIC	TTL	-55...+125	<550		<70		TTL-TS
DM 74S470	Nsc	20-DIP	TTL	0...+70	<787		<60		TTL-OC
DM 74LS471 J	Nsc	20-DIC	TTL	0...+70	<550		<60		TTL-TS
DM 74LS471 N	Nsc	20-DIP	TTL	0...+70	<550		<60		TTL-TS
DM 74S471 N	Nsc	20-DIP	TTL	0...+70	<787		<60		TTL-TS
N 82LS135 D	Val	20-FLAT	TTL	0...+75	<525		<100		TTL-TS
N 82LS135 N	Val	20-DIP	TTL	0...+75	<525		<100		TTL-TS
N 82S135 D	Val	20-FLAT	TTL	0...+75	<787		<45		TTL-TS

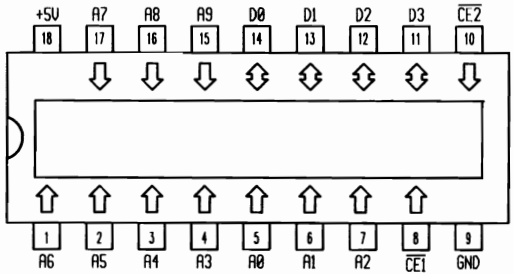
82135 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S135 N	Val	20-DIP	TTL	0...+75	<787		<45		TTL-TS
SN 74S470 J	Tix	20-DIC	TTL	0...+70	<813		<70		TTL-OC
SN 74S470 N	Tix	20-DIP	TTL	0...+70	<813		<70		TTL-OC
SN 74S471 J	Tix	20-DIC	TTL	0...+70	<813		<70		TTL-TS
SN 74S471 N	Tix	20-DIP	TTL	0...+70	<813		<70		TTL-TS
TBP 18SA22 J	Tix	20-DIC	TTL	0...+70	<813		<70		TTL-OC
TBP 18SA22 MJ	Tix	20-DIC	TTL	-55...+125	<813		<80		TTL-OC
TBP 18SA22 N	Tix	20-DIP	TTL	0...+70	<813		<70		TTL-OC
TBP 18S22 J	Tix	20-DIC	TTL	0...+70	<813		<70		TTL-TS
TBP 18S22 MJ	Tix	20-DIC	TTL	-55...+125	<813		<80		TTL-TS
TBP 18S22 N	Tix	20-DIP	TTL	0...+70	<813		<70		TTL-TS
TBP 28LA22 J	Tix	20-DIC	TTL	0...+70	<525		<75		TTL-OC
TBP 28LA22 MJ	Tix	20-DIC	TTL	-55...+125	<550		<80		TTL-OC
TBP 28LA22 N	Tix	20-DIP	TTL	0...+70	<525		<75		TTL-OC
TBP 28L22 J	Tix	20-DIC	TTL	0...+70	<525		<70		TTL-TS
TBP 28L22 MJ	Tix	20-DIC	TTL	-55...+125	<550		<75		TTL-TS
TBP 28L22 N	Tix	20-DIP	TTL	0...+70	<525		<70		TTL-TS
6308-1	Mmi	20-DIC	TTL	0...+70	<814		<70		TTL-OC
6309-1	Mmi	20-DIC	TTL	0...+70	<814		<70		TTL-TS
63LS280	Mmi	20-DIC	TTL	0...+75	289		51		TTL-OC
63PS280	Mmi	20-DIC	TTL	0...+75	551	<131	33		TTL-OC
63S280	Mmi	20-DIC	TTL	0...+75	<551		30		TTL-OC
63LS281	Mmi	20-DIC	TTL	0...+75	289		51		TTL-TS
63PS281	Mmi	20-DIC	TTL	0...+75	551	<157	33		TTL-TS
63S281	Mmi	20-DIC	TTL	0...+75	<551		30		TTL-TS

82135 — 256x8-Bit PROM



82135 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 74LS471 V	Nsc	20-FLAT	TTL	0...+70	<550		<60		TTL-TS
N 82LS135 A	Val	20-PLCC	TTL	0...+75	<525		<100		TTL-TS
N 82S135 A	Val	20-PLCC	TTL	0...+75	<787		<45		TTL-TS

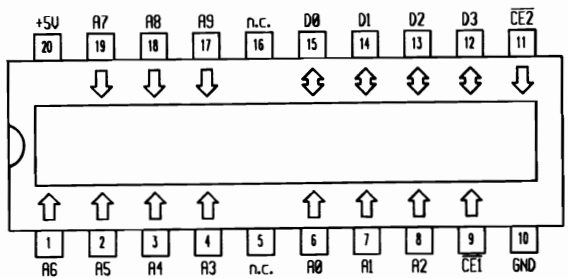
82136 — 1024x4-Bit PROM



82136 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
Am 27S32A	Amd	18-DIP	TTL	0...+75	<735	<35		TTL-OC
Am 27S33A	Amd	18-DIP	TTL	0...+75	<735	<35		TTL-TS
DM 54S572 AJ	Nsc	18-DIC	TTL	-55...+125	<770	<60		TTL-OC
DM 54S572 J	Nsc	18-DIC	TTL	-55...+125	<770	<75		TTL-OC
DM 54S573 AJ	Nsc	18-DIC	TTL	-55...+125	<770	<60		TTL-TS
DM 54S573 BJ	Nsc	18-DIC	TTL	-55...+125	<770	<50		TTL-TS
DM 54S573 J	Nsc	18-DIC	TTL	-55...+125	<770	<75		TTL-TS
DM 74S572 AJ	Nsc	18-DIC	TTL	0...+70	<770	<45		TTL-OC
DM 74S572 AN	Nsc	18-DIP	TTL	0...+70	<770	<45		TTL-OC
DM 74S572 J	Nsc	18-DIC	TTL	0...+70	<770	<60		TTL-OC
DM 74S572 N	Nsc	18-DIP	TTL	0...+70	<770	<60		TTL-OC
DM 74S573 AJ	Nsc	18-DIC	TTL	0...+70	<770	<45		TTL-TS
DM 74S573 AN	Nsc	18-DIP	TTL	0...+70	<770	<45		TTL-TS
DM 74S573 BJ	Nsc	18-DIC	TTL	0...+70	<770	<35		TTL-TS
DM 74S573 BN	Nsc	18-DIP	TTL	0...+70	<770	<35		TTL-TS
DM 74S573 J	Nsc	18-DIC	TTL	0...+70	<770	<60		TTL-TS
DM 74S573 N	Nsc	18-DIP	TTL	0...+70	<770	<60		TTL-TS
HN 25044	Hit	18-DIC	TTL	-20...+75	500	<50		TTL-OC
HN 25045	Hit	18-DIC	TTL	-20...+75	500	<50		TTL-TS
IM 56S06	Isi	18-DIP	TTL	0...+75		<50		TTL-OC
IM 56S26	Isi	18-DIP	TTL	0...+75		<50		TTL-TS
LH 5606	Sha	18-DIP	TTL	0...+75	685	<70		TTL-OC
LH 5626	Sha	18-DIP	TTL	0...+75	685	<70		TTL-TS
M 54740 APS	Mit	18-DIP	TTL	0...+75	<892	<55		TTL-OC
M 54741 APS	Mit	18-DIP	TTL	0...+75	<892	<55		TTL-TS
MB 7054	Fui	18-DIC	TTL	0...+75	<682	<70		TTL-TS
MB 7059	Fui	18-DIC	TTL	0...+75	<682	<70		TTL-OC
MB 7121 E	Fui	18-DIP	TTL	0...+75	<787	<45		TTL-OC
MB 7121 H	Fui	18-DIP	TTL	0...+75	<787	<35		TTL-OC
MB 7121 N	Fui	18-DIP	TTL	0...+75	<787	<60		TTL-OC
MB 7122 E	Fui	18-DIP	TTL	0...+75	<787	<45		TTL-OC
MB 7122 H	Fui	18-DIP	TTL	0...+75	<787	<35		TTL-OC
MB 7122 N	Fui	18-DIP	TTL	0...+75	<787	<60		TTL-OC
MCM 7642	Mot	18-DIP	TTL	0...+70	<735	<70		TTL-OC
MCM 7643	Mot	18-DIP	TTL	0...+70	<735	<70		TTL-TS
N 82S136 F	Sig	18-DIC	TTL	0...+75	<735	<60		TTL-OC
N 82S136 N	Sig	18-DIP	TTL	0...+75	<735	<60		TTL-OC
N 82S137C N	Val	18-DIP	TTL	0...+75	<735	<20		TTL-TS
N 82S137 F	Sig	18-DIC	TTL	0...+75	<735	<60		TTL-TS
N 82S137 N	Val	18-DIP	TTL	0...+75	<735	<60		TTL-TS
N 82S137A N	Val	18-DIP	TTL	0...+75	<735	<45		TTL-TS
N 82S137B N	Val	18-DIP	TTL	0...+75	<735	<35		TTL-TS
S 82S136 F	Sig	18-DIC	TTL	-55...+125	<770	<80		TTL-OC
S 82S137 F	Sig	18-DIC	TTL	-55...+125	<770	<80		TTL-TS
SN 74S476 J	Tix	18-DIC	TTL	0...+70	<735	<60		TTL-TS
SN 74S476 N	Tix	18-DIP	TTL	0...+70	<735	<60		TTL-TS
SN 74S477 J	Tix	18-DIC	TTL	0...+70	<735	<60		TTL-OC
SN 74S477 N	Tix	18-DIP	TTL	0...+70	<735	<60		TTL-OC
TBP 24SA41 J	Tix	18-DIC	TTL	0...+70	<735	<60		TTL-OC
TBP 24SA41 MJ	Tix	18-DIC	TTL	-55...+125	<770	<75		TTL-OC
TBP 24SA41 N	Tix	18-DIP	TTL	0...+70	<735	<60		TTL-OC
TBP 24S41 J	Tix	18-DIC	TTL	0...+70	<735	<60		TTL-TS

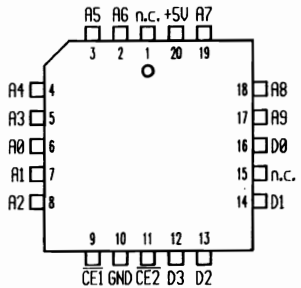
82136 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TBP 24S41 MJ	Tix	18-DIC	TTL	-55...+125	<770		<75		TTL-TS
TBP 24S41 N	Tix	18-DIP	TTL	0...+70	<735		<60		TTL-TS
3605	Int	18-DIP	TTL	0...+75	<787		<70		TTL-OC
3605-2	Int	18-DIP	TTL	0...+75	<787		<60		TTL-OC
3625	Int	18-DIP	TTL	0...+75	<787		<70		TTL-TS
3625-2	Int	18-DIP	TTL	0...+75	<787		<60		TTL-TS
6352-1	Mmi	18-DIC	TTL	0...+70	<919		<60		TTL-OC
6353-1	Mmi	18-DIC	TTL	0...+70	<919		<60		TTL-TS
63LS440	Mmi	18-DIP	TTL	0...+75	<446		<65		TTL-OC
63PS440	Mmi	18-DIP	TTL	0...+75	551	<105	<33		TTL-OC
63S440	Mmi	18-DIP	TTL	0...+75	<892		<50		TTL-OC
63LS441	Mmi	18-DIP	TTL	0...+75	<446		<65		TTL-TS
63PS441	Mmi	18-DIP	TTL	0...+75	551	<131	<33		TTL-TS
63S441	Mmi	18-DIP	TTL	0...+75	<892		<50		TTL-TS
93452 DC	Fch	18-DIC	TTL	0...+75	<892		<55		TTL-OC
93452 DM	Fch	18-DIC	TTL	-55...+125	<935		<70		TTL-OC
93452 PC	Fch	18-DIP	TTL	0...+75	<892		<55		TTL-OC
93453 DC	Fch	18-DIC	TTL	0...+75	<892		<55		TTL-TS
93453 DM	Fch	18-DIC	TTL	-55...+125	<935		<70		TTL-TS
93453 PC	Fch	18-DIP	TTL	0...+75	<892		<55		TTL-TS
µPB 400 C-E	Nip	18-DIP	TTL	0...+75	<787		<100		TTL-OC
µPB 406 C	Nip	18-DIP	TTL	-25...+75	<825		<70		TTL-OC
µPB 406 C-1	Nip	18-DIP	TTL	-25...+75	<825		<60		TTL-OC
µPB 406 C-2	Nip	18-DIP	TTL	-25...+75	<825		<50		TTL-OC
µPB 406 C-3	Nip	18-DIP	TTL	-25...+75	<825		<35		TTL-OC
µPB 406 D	Nip	18-DIC	TTL	-25...+75	<825		<70		TTL-OC
µPB 406 D-1	Nip	18-DIC	TTL	-25...+75	<825		<60		TTL-OC
µPB 406 D-2	Nip	18-DIC	TTL	-25...+75	<825		<50		TTL-OC
µPB 406 D-3	Nip	18-DIC	TTL	-25...+75	<825		<35		TTL-OC
µPB 426 C	Nip	18-DIP	TTL	-25...+75	<825		<70		TTL-TS
µPB 426 C-1	Nip	18-DIP	TTL	-25...+75	<825		<60		TTL-TS
µPB 426 C-2	Nip	18-DIP	TTL	-25...+75	<825		<50		TTL-TS
µPB 426 C-3	Nip	18-DIP	TTL	-25...+75	<825		<35		TTL-TS
µPB 426 D	Nip	18-DIC	TTL	-25...+75	<825		<70		TTL-TS
µPB 426 D-1	Nip	18-DIC	TTL	-25...+75	<825		<60		TTL-TS
µPB 426 D-2	Nip	18-DIC	TTL	-25...+75	<825		<50		TTL-TS
µPB 426 D-3	Nip	18-DIC	TTL	-25...+75	<825		<35		TTL-TS

82136 — 1024x4-Bit PROM



82136 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S137 D	Val	20-FLAT	TTL	0...+75	<735		<60		TTL-TS
N 82S137A D	Val	20-FLAT	TTL	0...+75	<735		<45		TTL-TS
N 82S137B D	Val	20-FLAT	TTL	0...+75	<735		<35		TTL-TS

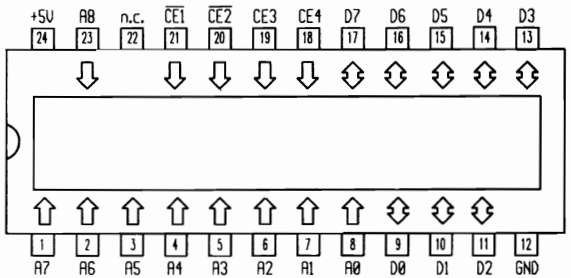
82136 — 1024x4-Bit PROM



82136 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S137C A	Val	20-PLCC	TTL	0...+75	<735		<20		TTL-TS

82136 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 74S572 AV	Nsc	20-FLAT	TTL	0...+70	<770		<45		TTL-OC
DM 74S572 V	Nsc	20-FLAT	TTL	0...+70	<770		<60		TTL-OC
DM 74S573 AV	Nsc	20-FLAT	TTL	0...+70	<770		<45		TTL-TS
DM 74S573 BV	Nsc	20-FLAT	TTL	0...+70	<770		<35		TTL-TS
DM 74S573 V	Nsc	20-FLAT	TTL	0...+70	<770		<60		TTL-TS
N 82S137 A	Val	20-PLCC	TTL	0...+75	<735		<60		TTL-TS
N 82S137A A	Val	20-PLCC	TTL	0...+75	<735		<45		TTL-TS
N 82S137B A	Val	20-PLCC	TTL	0...+75	<735		<35		TTL-TS

82140 — 512x8-Bit PROM



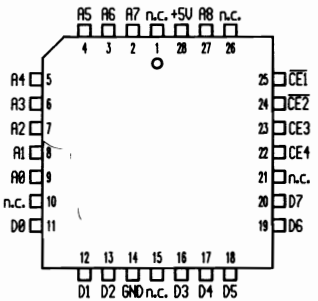
82140 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S30	Amd	24-DIP	TTL	0...+75	<919		<55		TTL-OC
Am 27S30 A	Amd	24-DIP	TTL	0...+75	<919		<35		TTL-OC
Am 27S31	Amd	24-DIP	TTL	0...+75	<919		<55		TTL-TS
Am 27S31 A	Amd	24-DIP	TTL	0...+75	<919		<35		TTL-TS
DM 54S474 AJ	Nsc	24-DIC	TTL	-55...+125	<935		<60		TTL-TS
DM 54S474 BJ	Nsc	24-DIC	TTL	-55...+125	<935		<50		TTL-TS
DM 54S474 J	Nsc	24-DIC	TTL	-55...+125	<935		<75		TTL-TS
DM 54S475 AJ	Nsc	24-DIC	TTL	-55...+125	<935		<60		TTL-OC

82140 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 54S475 J	Nsc	24-DIC	TTL	-55...+125	<935		<75		TTL-OC
DM 74S474 AJ	Nsc	24-DIC	TTL	0...+70	<935		<45		TTL-TS
DM 74S474 AN	Nsc	24-DIP	TTL	0...+70	<935		<45		TTL-TS
DM 74S474 BJ	Nsc	24-DIC	TTL	0...+70	<935		<35		TTL-TS
DM 74S474 BN	Nsc	24-DIP	TTL	0...+70	<935		<35		TTL-TS
DM 74S474 J	Nsc	24-DIC	TTL	0...+70	<935		<65		TTL-TS
DM 74S474 N	Nsc	24-DIP	TTL	0...+70	<935		<65		TTL-TS
DM 74S475 AJ	Nsc	24-DIC	TTL	0...+70	<935		<45		TTL-OC
DM 74S475 AN	Nsc	24-DIP	TTL	0...+70	<935		<45		TTL-OC
DM 74S475 J	Nsc	24-DIC	TTL	0...+70	<935		<65		TTL-OC
DM 74S475 N	Nsc	24-DIP	TTL	0...+70	<935		<65		TTL-OC
DM 87S295 N	Nsc	24-DIP	TTL	0...+70	<892		<65		TTL-OC
DM 87S296 N	Nsc	24-DIP	TTL	0...+70	<892		<65		TTL-TS
IM 5605 C	Isi	24-DIP	TTL	0...+75	<971		<70		TTL-OC
IM 5605 CA	Isi	24-DIP	TTL	0...+75	<971		<55		TTL-OC
IM 5625 C	Isi	24-DIP	TTL	0...+75	<971		<70		TTL-TS
IM 5625 CA	Isi	24-DIP	TTL	0...+75	<971		<55		TTL-TS
MCM 7640	Mot	24-DIC	TTL	0...+70	<735		<70		TTL-OC
MCM 7641	Mot	24-DIC	TTL	0...+70	<735		<70		TTL-TS
N 82S140 F	Sig	24-DIC	TTL	0...+75	<919		<60		TTL-OC
N 82S140 N	Sig	24-DIP	TTL	0...+75	<919		<60		TTL-OC
N 82S141A N	Val	24-DIP	TTL	0...+75	<919		<45		TTL-TS
N 82S141 F	Sig	24-DIC	TTL	0...+75	<919		<60		TTL-TS
N 82S141 N	Sig	24-DIP	TTL	0...+75	<919		<60		TTL-TS
S 82S140 F	Sig	24-DIC	TTL	-55...+125	<1017		<90		TTL-OC
S 82S141 F	Sig	24-DIC	TTL	-55...+125	<1017		<90		TTL-TS
SN 74S474 J	Tix	24-DIC	TTL	0...+70	600		<75		TTL-TS
SN 74S474 N	Tix	24-DIP	TTL	0...+70	600		<75		TTL-TS
SN 74S475 J	Tix	24-DIC	TTL	0...+70	600		<75		TTL-OC
SN 74S475 N	Tix	24-DIP	TTL	0...+70	600		<75		TTL-OC
TBP 18SA46 J	Tix	24-DIC	TTL	0...+70	600		<75		TTL-OC
TBP 18SA46 MJ	Tix	24-DIC	TTL	-55...+125	600		<85		TTL-OC
TBP 18SA46 N	Tix	24-DIP	TTL	0...+70	600		<75		TTL-OC
TBP 18S46 J	Tix	24-DIC	TTL	0...+70	600		<75		TTL-TS
TBP 18S46 MJ	Tix	24-DIC	TTL	-55...+125	600		<85		TTL-TS
TBP 18S46 N	Tix	24-DIP	TTL	0...+70	600		<75		TTL-TS
TBP 28L45 J	Tix	24-TDIC	TTL	0...+70	<262		<95		TTL-TS

82140 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TBP 28L45 MJ	Tix	24-TDIC	TTL	-55...+125	<275		<110		TTL-TS
TBP 28L45 N	Tix	24-TDIP	TTL	0...+70	<262		<95		TTL-TS
TBP 28P45 J	Tix	24-TDIC	TTL	0...+70	<525	<63	35		TTL-TS
TBP 28P45 MJ	Tix	24-TDIC	TTL	-55...+125	<550	<66	35		TTL-TS
TBP 28P45 N	Tix	24-TDIP	TTL	0...+70	<525	<63	35		TTL-TS
TBP 28S45 J	Tix	24-TDIC	TTL	0...+70	<709		<60		TTL-TS
TBP 28S45 MJ	Tix	24-TDIC	TTL	-55...+125	<742		<60		TTL-TS
TBP 28S45 N	Tix	24-TDIP	TTL	0...+70	<709		<60		TTL-TS
TBP 28L46 J	Tix	24-TDIC	TTL	0...+70	<262		<95		TTL-TS
TBP 28L46 MJ	Tix	24-TDIC	TTL	-55...+125	<275		<110		TTL-TS
TBP 28L46 N	Tix	24-TDIP	TTL	0...+70	<262		<95		TTL-TS
TBP 28SA46 J	Tix	24-TDIC	TTL	0...+70	<709		<65		TTL-OC
TBP 28SA46 MJ	Tix	24-TDIC	TTL	-55...+125	<742		<65		TTL-OC
TBP 28SA46 N	Tix	24-TDIP	TTL	0...+70	<709		<65		TTL-OC
TBP 28S46 J	Tix	24-TDIC	TTL	0...+70	<709		<60		TTL-TS
TBP 28S46 MJ	Tix	24-TDIC	TTL	-55...+125	<742		<70		TTL-TS
TBP 28S46 N	Tix	24-TDIP	TTL	0...+70	<709		<60		TTL-TS
3604	Int	24-DIP	TTL	0...+75	<997		<70		TTL-OC
3604-4	Int	24-DIP	TTL	0...+75	<997		<90		TTL-OC
3604 A	Int	24-DIP	TTL	0...+75	<919		<70		TTL-OC
3604 A-2	Int	24-DIP	TTL	0...+75	<919		<60		TTL-OC
3624	Int	24-DIP	TTL	0...+75	<997		<70		TTL-TS
3624-4	Int	24-DIP	TTL	0...+75	<997		<90		TTL-TS
3624 A	Int	24-DIP	TTL	0...+75	<919		<70		TTL-TS
3624 A-4	Int	24-DIP	TTL	0...+75	<919		<60		TTL-TS
6340-1	Mmi	24-DIC	TTL	0...+70	<892		<90		TTL-OC
6340-2	Mmi	24-DIP	TTL	0...+75	<814		<70		TTL-OC
6341-1	Mmi	24-DIC	TTL	0...+70	<892		<90		TTL-TS
6341-2	Mmi	24-DIP	TTL	0...+75	<814		<70		TTL-TS
63LS482	Mmi	24-DIP	TTL	0...+75			51		TTL-OC
63PS482	Mmi	24-DIP	TTL	0...+75			36		TTL-OC
63S482	Mmi	24-DIP	TTL	0...+75			30		TTL-OC
63LS483	Mmi	24-DIP	TTL	0...+75			51		TTL-TS
63PS483	Mmi	24-DIP	TTL	0...+75			36		TTL-TS
63S483	Mmi	24-DIP	TTL	0...+75			30		TTL-TS
93438 DC	Fch	24-DIC	TTL	0...+75	650		<55		TTL-OC
93438 DM	Fch	24-DIC	TTL	-55...+125	650		<70		TTL-OC

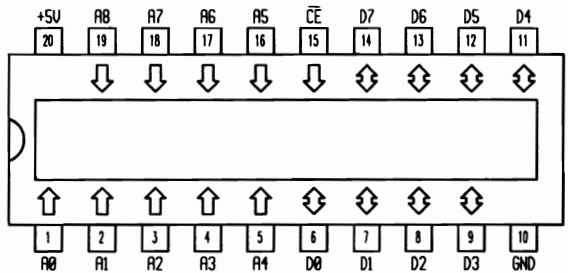
82140 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93438 FC	Fch	24-FLAT	TTL	0...+75	650		<55		TTL-OC
93438 FM	Fch	24-FLAT	TTL	-55...+125	650		<70		TTL-OC
93438 PC	Fch	24-DIP	TTL	0...+75	650		<55		TTL-OC
93448 DC	Fch	24-DIC	TTL	0...+75	650		<55		TTL-TS
93448 DM	Fch	24-DIC	TTL	-55...+125	650		<70		TTL-TS
93448 FC	Fch	24-FLAT	TTL	0...+75	650		<55		TTL-TS
93448 FM	Fch	24-FLAT	TTL	-55...+125	650		<70		TTL-TS
93448 PC	Fch	24-DIP	TTL	0...+75	650		<55		TTL-TS
µPB 405 C	Nip	24-DIP	TTL	-25...+75	<880		<60		TTL-OC
µPB 405 C-1	Nip	24-DIP	TTL	-25...+75	<880		<50		TTL-OC
µPB 405 C-2	Nip	24-DIP	TTL	-25...+75	<880		<40		TTL-OC
µPB 405 D	Nip	24-DIC	TTL	-25...+75	<880		<60		TTL-OC
µPB 405 D-1	Nip	24-DIC	TTL	-25...+75	<880		<50		TTL-OC
µPB 405 D-2	Nip	24-DIC	TTL	-25...+75	<880		<40		TTL-OC
µPB 425 C	Nip	24-DIP	TTL	-25...+75	<880		<60		TTL-TS
µPB 425 C-1	Nip	24-DIP	TTL	-25...+75	<880		<50		TTL-TS
µPB 425 C-2	Nip	24-DIP	TTL	-25...+75	<880		<40		TTL-TS
µPB 425 D	Nip	24-DIC	TTL	-25...+75	<880		<60		TTL-TS
µPB 425 D-1	Nip	24-DIC	TTL	-25...+75	<880		<50		TTL-TS
µPB 425 D-2	Nip	24-DIC	TTL	-25...+75	<880		<40		TTL-TS

82140 — 512x8-Bit PROM



82140 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / $P_{standby}$ mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
DM 74S474 AV	Nsc	28-FLAT	TTL	0...+70	<935	<45		TTL-TS
DM 74S474 BV	Nsc	28-FLAT	TTL	0...+70	<935	<35		TTL-TS
DM 74S474 V	Nsc	28-FLAT	TTL	0...+70	<935	<65		TTL-TS
DM 74S475 AV	Nsc	28-FLAT	TTL	0...+70	<935	<45		TTL-OC
DM 74S475 V	Nsc	28-FLAT	TTL	0...+70	<935	<65		TTL-OC

82147 — 512x8-Bit PROM

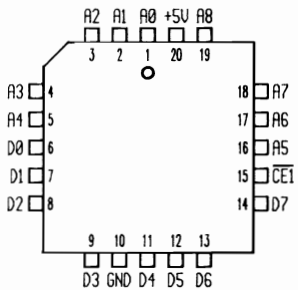


82147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / $P_{standby}$ mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
Am 27S28 A	Amd	20-DIP	TTL	0...+75	<840	<35		TTL-OC
Am 27S29 A	Amd	20-DIP	TTL	0...+75	<840	<35		TTL-TS
DM 54S472 AJ	Nsc	20-DIC	TTL	0...+70	<853	<60		TTL-TS
DM 54S472 BJ	Nsc	20-DIC	TTL	0...+70	<853	<50		TTL-TS
DM 54S472 J	Nsc	20-DIC	TTL	0...+70	<853	<75		TTL-TS
DM 54S473 AJ	Nsc	20-DIC	TTL	0...+70	<853	<60		TTL-OC
DM 54S473 J	Nsc	20-DIC	TTL	0...+70	<853	<75		TTL-OC
DM 74S472 AJ	Nsc	20-DIC	TTL	0...+70	<853	<45		TTL-TS

82147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 74S472 AN	Nsc	20-DIP	TTL	0...+70	<853		<45		TTL-TS
DM 74S472 BJ	Nsc	20-DIC	TTL	0...+70	<853		<35		TTL-TS
DM 74S472 BN	Nsc	20-DIP	TTL	0...+70	<853		<35		TTL-TS
DM 74S472 J	Nsc	20-DIC	TTL	0...+70	<853		<60		TTL-TS
DM 74S472 N	Nsc	20-DIP	TTL	0...+70	<853		<60		TTL-TS
DM 74S473 AJ	Nsc	20-DIC	TTL	0...+70	<853		<45		TTL-OC
DM 74S473 AN	Nsc	20-DIP	TTL	0...+70	<853		<45		TTL-OC
DM 74S473 J	Nsc	20-DIC	TTL	0...+70	<853		<60		TTL-OC
DM 74S473 N	Nsc	20-DIP	TTL	0...+70	<853		<60		TTL-OC
MB 7123 H	Fui	20-DIP	TTL	0...+75	<892		<35		TTL-OC
MB 7123 N	Fui	20-DIP	TTL	0...+75	<892		<60		TTL-OC
MB 7124 H	Fui	20-DIP	TTL	0...+75	<892		<35		TTL-TS
MB 7124 N	Fui	20-DIP	TTL	0...+75	<892		<60		TTL-TS
N 82S147B N	Val	20-DIP	TTL	0...+75	<814		<25		TTL-TS
N 82S147 D	Val	20-FLAT	TTL	0...+75	<814		<60		TTL-TS
N 82S147A D	Val	20-FLAT	TTL	0...+75	<814		<45		TTL-TS
N 82S147 N	Val	20-DIP	TTL	0...+75	<814		<60		TTL-TS
N 82S147A N	Val	20-DIP	TTL	0...+75	<814		<45		TTL-TS
SN 74S472 J	Tix	20-DIC	TTL	0...+70	600		<75		TTL-TS
SN 74S472 N	Tix	20-DIP	TTL	0...+70	600		<75		TTL-TS
SN 74S473 J	Tix	20-DIC	TTL	0...+70	600		<75		TTL-OC
SN 74S473 N	Tix	20-DIP	TTL	0...+70	600		<75		TTL-OC
TBP 18SA42 J	Tix	20-DIC	TTL	0...+70	600		<75		TTL-OC
TBP 18SA42 MJ	Tix	20-DIC	TTL	-55...+125	600		<85		TTL-OC
TBP 18SA42 N	Tix	20-DIP	TTL	0...+70	600		<75		TTL-OC
TBP 18S42 J	Tix	20-DIC	TTL	0...+70	600		<75		TTL-TS
TBP 18S42 MJ	Tix	20-DIC	TTL	-55...+125	600		<85		TTL-TS
TBP 18S42 N	Tix	20-DIP	TTL	0...+70	600		<75		TTL-TS
TBP 28L42 J	Tix	20-DIC	TTL	0...+70	<262		<95		TTL-TS
TBP 28L42 MJ	Tix	20-DIC	TTL	-55...+125	<275		<110		TTL-TS
TBP 28L42 N	Tix	20-DIP	TTL	0...+70	<262		<95		TTL-TS
TBP 28P42 J	Tix	20-DIC	TTL	0...+70	<525	<63	35		TTL-TS
TBP 28P42 MJ	Tix	20-DIC	TTL	-55...+125	<550	<66	35		TTL-TS
TBP 28P42 N	Tix	20-DIP	TTL	0...+70	<525	<63	35		TTL-TS
TBP 28SA42 J	Tix	20-DIC	TTL	0...+75	<709		<65		TTL-OC
TBP 28SA42 MJ	Tix	20-DIC	TTL	-55...+125	<742		<65		TTL-OC
TBP 28SA42 N	Tix	20-DIP	TTL	0...+75	<709		<65		TTL-OC

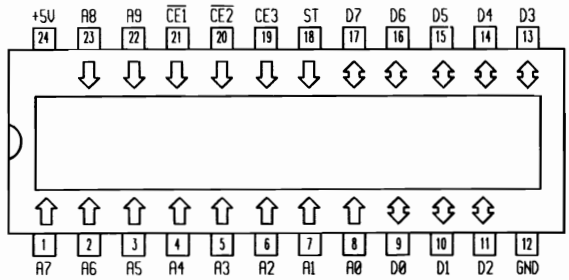
82147 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TBP 28S42 J	Tix	20-DIC	TTL	0...+75	<709		<60		TTL-TS
TBP 28S42 MJ	Tix	20-DIC	TTL	-55...+125	<742		<60		TTL-TS
TBP 28S42 N	Tix	20-DIP	TTL	0...+75	<709		<60		TTL-TS
6348-1	Mmi	20-DIC	TTL	0...+70	<814		<70		TTL-OC
6348-2	Mmi	20-DIC	TTL	0...+75	<814		<70		TTL-OC
6349-1	Mmi	20-DIC	TTL	0...+70	<814		<70		TTL-TS
6349-2	Mmi	20-DIC	TTL	0...+75	<814		<55		TTL-TS
63LS480	Mmi	20-DIC	TTL	0...+75	289		51		TTL-OC
63PS480	Mmi	20-DIC	TTL	0...+75	551	<131	36		TTL-OC
63S480	Mmi	20-DIC	TTL	0...+75	551		30		TTL-OC
63LS481	Mmi	20-DIC	TTL	0...+75	289		51		TTL-TS
63PS481	Mmi	20-DIC	TTL	0...+75	551	<157	36		TTL-TS
63S481	Mmi	20-DIC	TTL	0...+75	551		30		TTL-TS
µPB 424 C	Nec	20-DIP	TTL	-25...+75	<825		<50		TTL-TS
µPB 424 C-1	Nec	20-DIP	TTL	-25...+75	<825		<40		TTL-TS
µPB 424 D	Nec	20-DIC	TTL	-25...+75	<825		<50		TTL-TS
µPB 424 D-1	Nec	20-DIC	TTL	-25...+75	<825		<40		TTL-TS

82147 — 512x8-Bit PROM



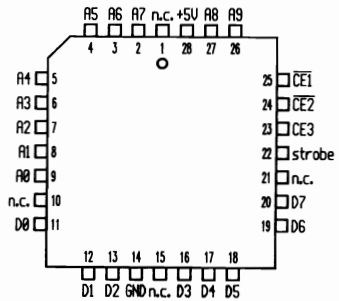
82147 Type	Man	Case	Techn.	T_U °C	P_{typ} mW / P standby mW $ mW/bit	t_{aa} ns	t_{ref} ms	Output
DM 74S472 AV	Nsc	20-FLAT	TTL	0...+70	<853	<45		TTL-TS
DM 74S472 BV	Nsc	20-FLAT	TTL	0...+70	<853	<35		TTL-TS
DM 74S472 V	Nsc	20-FLAT	TTL	0...+70	<853	<60		TTL-TS
DM 74S473 AV	Nsc	20-FLAT	TTL	0...+70	<853	<45		TTL-OC
DM 74S473 V	Nsc	20-FLAT	TTL	0...+70	<853	<60		TTL-OC
N 82S147 A	Val	20-PLCC	TTL	0...+75	<814	<60		TTL-TS
N 82S147A A	Val	20-PLCC	TTL	0...+75	<814	<45		TTL-TS
N 82S147B A	Val	20-PLCC	TTL	0...+75	<814	<25		TTL-TS

82183 — 1024x8-Bit PROM

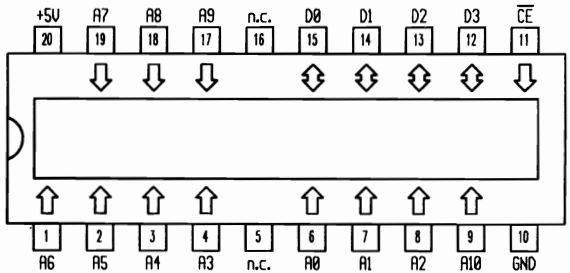


82183 Type	Man	Case	Techn.	T_U °C	P_{typ} mW / P standby mW $ mW/bit	t_{aa} ns	t_{ref} ms	Output
N 82S183 N	Val	24-DIP	TTL	0...+75	<919	<60		TTL-TS

82183 — 1024x8-Bit PROM



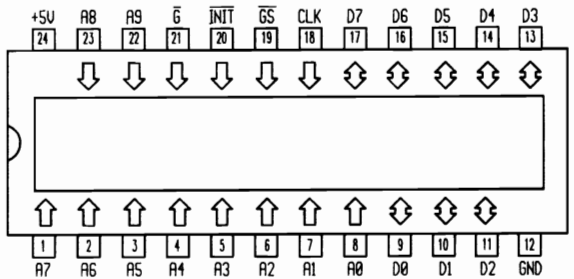
82185 — 2048x4-Bit PROM



82183 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S183 A	Val	28-PLCC	TTL	0...+75	<919		<60		TTL-TS

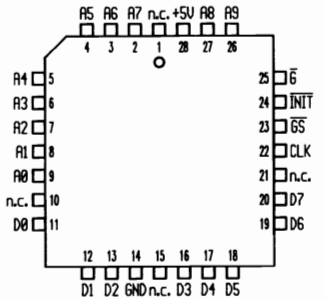
82185 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S185A D	Val	20-FLAT	TTL	0...+75	<814		<50		TTL-TS
N 82S185B D	Val	20-FLAT	TTL	0...+75	<814		<45		TTL-TS
N 82S185 D	Val	20-FLAT	TTL	0...+75	<630		<100		TTL-TS

82187 — 1024x8-Bit PROM



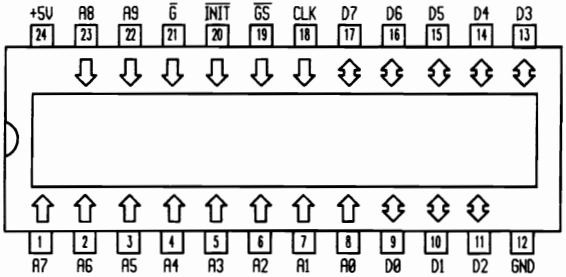
82187 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77SR181 J	Nsc	24-DIC	TTL	-55...+125	<962		<50		TTL-TS
DM 87SR181 J	Nsc	24-TDIC	TTL	0...+75	<962		<40		TTL-TS
DM 87SR181 N	Nsc	24-TDIP	TTL	0...+75	<962		<40		TTL-TS
N 82HS187A N	Val	24-TDIP	TTL	0...+75	<919		<45		TTL-TS
N 82HS187 N	Val	24-TDIP	TTL	0...+75	<919		<55		TTL-TS

82187 — 1024x8-Bit PROM



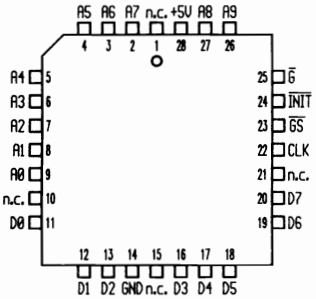
82187 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87SR181 V	Nsc	28-FLAT	TTL	0...+75	<962		<40		TTL-TS
N 82HS187 A	Val	28-PLCC	TTL	0...+75	<919		<55		TTL-TS
N 82HS187A A	Val	28-PLCC	TTL	0...+75	<919		<45		TTL-TS

82189 — 1024x8-Bit Register PROM



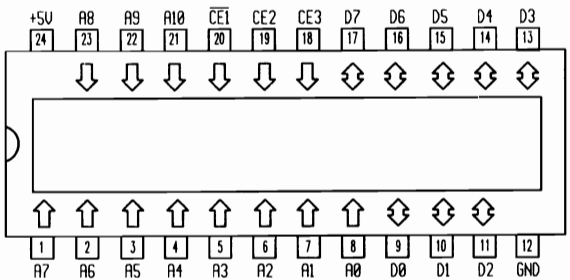
82189 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82HS189A N	Val	24-TDIP	TTL	0...+75	<919		<45		TTL-TS
N 82HS189 N	Val	24-TDIP	TTL	0...+75	<919		<55		TTL-TS

82189 — 1024x8-Bit Register PROM



82189 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82HS189 A	Val	28-PLCC	TTL	0...+75	<919		<55		TTL-TS
N 82HS189A A	Val	28-PLCC	TTL	0...+75	<919		<45		TTL-TS

82190 — 2048x8-Bit PROM



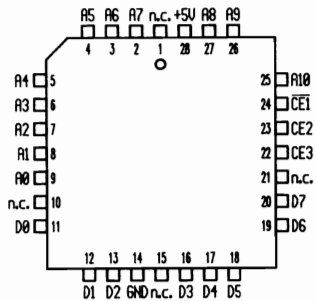
82190 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S190	Amd	24-DIP	TTL	0...+75	<971		<50		TTL-OC
Am 27S190 A	Amd	24-DIP	TTL	0...+75	<971		<35		TTL-OC
Am 27S191	Amd	24-DIP	TTL	0...+75	<971		<50		TTL-TS
Am 27S191 A	Amd	24-DIP	TTL	0...+75	<971		<35		TTL-TS
C 3636 B-1	Int	24-DIC	TTL	0...+75	<971		<35		TTL-TS
C 3636 B-2	Int	24-DIC	TTL	0...+75	<971		<45		TTL-TS
DM 77S190 J	Nsc	24-DIC	TTL	-55...+125	<770		<80		TTL-TS
DM 77S191 J	Nsc	24-DIC	TTL	-55...+125	<770		<80		TTL-OC
DM 77S290 J	Nsc	24-TDIC	TTL	-55...+125	<962		<80		TTL-OC
DM 77S291 AJ	Nsc	24-TDIC	TTL	-55...+125	<962		<60		TTL-TS
DM 77S291 BJ	Nsc	24-TDIC	TTL	-55...+125	<962		<50		TTL-TS
DM 77S291 J	Nsc	24-TDIC	TTL	-55...+125	<962		<80		TTL-TS
DM 87S190 J	Nsc	24-DIC	TTL	0...+70	<962		<65		TTL-OC
DM 87S190 N	Nsc	24-DIP	TTL	0...+70	<962		<65		TTL-OC
DM 87S191 A	Nsc	24-DIP	TTL	0...+70	<919		<45		TTL-TS
DM 87S191 B	Nsc	24-DIP	TTL	0...+70	<919		<35		TTL-TS
DM 87S191 J	Nsc	24-DIC	TTL	0...+70	<962		<65		TTL-TS
DM 87S191 N	Nsc	24-DIP	TTL	0...+70	<962		<65		TTL-TS
DM 87S290 J	Nsc	24-TDIC	TTL	0...+70	<962		<65		TTL-OC
DM 87S290 N	Nsc	24-TDIP	TTL	0...+70	<962		<65		TTL-OC
DM 87S291 AJ	Nsc	24-TDIC	TTL	0...+70	<962		<45		TTL-TS
DM 87S291 AN	Nsc	24-TDIP	TTL	0...+70	<962		<45		TTL-TS
DM 87S291 BJ	Nsc	24-TDIC	TTL	0...+70	<962		<35		TTL-TS
DM 87S291 BN	Nsc	24-TDIP	TTL	0...+70	<962		<35		TTL-TS
DM 87S291 J	Nsc	24-TDIC	TTL	0...+70	<962		<65		TTL-TS
DM 87S291 N	Nsc	24-TDIP	TTL	0...+70	<962		<65		TTL-TS
HN 25168 S	Hit	24-DIP	TTL	0...+75	<892		<60		TTL-OC
HN 25169 S	Hit	24-DIP	TTL	0...+75	<892		<60		TTL-TS
N 82S190 I	Sig	24-DIC	TTL	0...+75	<919		<80		TTL-OC
N 82HS191 N	Val	24-DIP	TTL	0...+75	<919		<20		TTL-TS
N 82HS191 N3	Val	24-TDIP	TTL	0...+75	<919		<20		TTL-TS
N 82S191A N	Val	24-DIP	TTL	0...+75	<919		<55		TTL-TS
N 82S191C N	Val	24-DIP	TTL	0...+75	<919		<35		TTL-TS
N 82S191C N3	Val	24-TDIP	TTL	0...+75	<919		<35		TTL-TS
N 82S191 I	Sig	24-DIC	TTL	0...+75	<919		<80		TTL-TS
N 82S191 N	Val	24-DIP	TTL	0...+75	<919		<80		TTL-TS
S 82S190 I	Sig	24-DIC	TTL	-55...+125	<1017		<100		TTL-OC
S 82S191 I	Sig	24-DIC	TTL	-55...+125	<1017		<100		TTL-TS
TBP 28L166 J	Tix	24-DIC	TTL	0...+70	<367		65		TTL-TS
TBP 28L166 MJ	Tix	24-DIC	TTL	-55...+125	<385		65		TTL-TS
TBP 28L166 N	Tix	24-DIP	TTL	0...+70	<367		65		TTL-TS
TBP 28P166 J	Tix	24-DIC	TTL	0...+70	<682	<131	35		TTL-TS
TBP 28P166 MJ	Tix	24-DIC	TTL	-55...+125	<715	<137	35		TTL-TS
TBP 28P166 N	Tix	24-DIP	TTL	0...+70	<682	<131	35		TTL-TS
TBP 28SA166 J	Tix	24-DIC	TTL	0...+70	<682		<80		TTL-OC

82190 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns.	t_{ref} ms	Output
					$mW/bit				
TBP 28SA166 MJ	Tix	24-DIC	TTL	-55...+125	<715		<80		TTL-OC
TBP 28SA166 N	Tix	24-DIP	TTL	0...+70	<682		<80		TTL-OC
TBP 28S166 J	Tix	24-DIC	TTL	0...+70	<682		<75		TTL-TS
TBP 28S166 MJ	Tix	24-DIC	TTL	-55...+125	<715		<75		TTL-TS
TBP 28S166 N	Tix	24-DIP	TTL	0...+70	<682		<75		TTL-TS
TS 71190A CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<60		TTL-OC
TS 71190A CP	Tho	24-DIP	NMOS	0...+70	<962,5		<60		TTL-OC
TS 71190B CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<45		TTL-OC
TS 71190B CP	Tho	24-DIP	NMOS	0...+70	<962,5		<45		TTL-OC
TS 71190C CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<35		TTL-OC
TS 71190C CP	Tho	24-DIP	NMOS	0...+70	<962,5		<35		TTL-OC
TS 71190 CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<80		TTL-OC
TS 71190 CP	Tho	24-DIP	NMOS	0...+70	<962,5		<80		TTL-OC
TS 71191A CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<60		TTL-TS
TS 71191A CP	Tho	24-DIP	NMOS	0...+70	<962,5		<60		TTL-TS
TS 71191A MC	Tho	24-DIC	NMOS	-55...+125	<1017		<60		TTL-TS
TS 71191A MJ	Tho	24-DIC	NMOS	-55...+125	<1017		<60		TTL-TS
TS 71191B CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<45		TTL-TS
TS 71191B CP	Tho	24-DIP	NMOS	0...+70	<962,5		<45		TTL-TS
TS 71191B MC	Tho	24-DIC	NMOS	-55...+125	<1017		<45		TTL-TS
TS 71191B MJ	Tho	24-DIC	NMOS	-55...+125	<1017		<45		TTL-TS
TS 71191C CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71191C CP	Tho	24-DIP	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71191 CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<80		TTL-TS
TS 71191C MC	Tho	24-DIC	NMOS	-55...+125	<1017		<35		TTL-TS
TS 71191C MJ	Tho	24-DIC	NMOS	-55...+125	<1017		<35		TTL-TS
TS 71191 CP	Tho	24-DIP	NMOS	0...+70	<962,5		<80		TTL-TS
TS 71191 MC	Tho	24-DIC	NMOS	-55...+125	<1017		<80		TTL-TS
TS 71191 MJ	Tho	24-DIC	NMOS	-55...+125	<1017		<80		TTL-TS
TS 71290C CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<35		TTL-0C
TS 71290C CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<35		TTL-0C
TS 71291C CJ	Tho	24-TDIC	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71291C CP	Tho	24-TDIP	NMOS	0...+70	<962,5		<35		TTL-TS
TS 71291C MC	Tho	24-TDIC	NMOS	-55...+125	<1017		<35		TTL-TS
TS 71291C MJ	Tho	24-TDIC	NMOS	-55...+125	<1017		<35		TTL-TS
3636	Int	24-DIC	TTL		<1017		<80		TTL-TS
3636-1	Int	24-DIC	TTL		<1017		<65		TTL-TS

82190 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
82HS191	Int	24-DIC	TTL	0...+75	<919		<50		TTL-TS
82S191	Int	24-DIC	TTL	0...+75	<919		<70		TTL-TS
93Z510 DC	Fch	24-DIC	TTL	0...+75	<919		<45		TTL-OC
93Z510 DM	Fch	24-DIC	TTL	-55...+125	<962		<55		TTL-OC
93Z510 FC	Fch	24-FLAT	TTL	0...+75	<919		<45		TTL-OC
93Z510 FM	Fch	24-FLAT	TTL	-55...+125	<962		<55		TTL-OC
93Z510 PC	Fch	24-DIP	TTL	0...+75	<919		<45		TTL-OC
93Z510 SDC	Fch	24-TDIC	TTL	0...+75	<919		<45		TTL-OC
93Z510 SDM	Fch	24-TDIC	TTL	-55...+125	<962		<55		TTL-OC
93Z511 DC	Fch	24-DIC	TTL	0...+75	<919		<45		TTL-TS
93Z511 DM	Fch	24-DIC	TTL	-55...+125	<962		<55		TTL-TS
93Z511 FC	Fch	24-FLAT	TTL	0...+75	<919		<45		TTL-TS
93Z511 FM	Fch	24-FLAT	TTL	-55...+125	<962		<55		TTL-TS
93Z511 PC	Fch	24-DIP	TTL	0...+70	<919		<45		TTL-TS
93Z511 SDC	Fch	24-TDIC	TTL	0...+75	<919		<45		TTL-TS
93Z511 SDM	Fch	24-TDIC	TTL	-55...+125	<962		<55		TTL-TS
93Z611 DC	Fch	24-DIC	TTL	0...+75			<25		TTL-TS
93Z611 DM	Fch	24-DIC	TTL	-55...+125			<30		TTL-TS
93Z611 FC	Fch	24-FLAT	TTL	0...+75			<25		TTL-TS
93Z611 FM	Fch	24-FLAT	TTL	-55...+125			<30		TTL-TS
93Z611 PC	Fch	24-DIP	TTL	0...+75			<25		TTL-TS
93Z611 SDC	Fch	24-TDIC	TTL	0...+75			<25		TTL-TS
93Z611 SDM	Fch	24-TDIC	TTL	-55...+125			<30		TTL-TS
63LS1680	Mmi	24-DIP	TTL	0...+75	352		66		TTL-OC
63PS1680	Mmi	24-DIP	TTL	0...+75	651	<157	48		TTL-OC
63S1680	Mmi	24-DIP	TTL	0...+75	651		46		TTL-OC
63LS1681	Mmi	24-DIP	TTL	0...+75	352		66		TTL-TS
63PS1681	Mmi	24-DIP	TTL	0...+75	651	<184	48		TTL-TS
63S1681	Mmi	24-DIP	TTL	0...+75	651		46		TTL-TS
µPB 409 C	Nip	24-DIP	TTL	-25...+75	<880		<70		TTL-OC
µPB 409 C-1	Nip	24-DIP	TTL	-25...+75	<880		<60		TTL-OC
µPB 409 C-2	Nip	24-DIP	TTL	-25...+75	<880		<50		TTL-OC
µPB 409 C-3	Nip	24-DIP	TTL	-25...+75	<880		<45		TTL-OC
µPB 409 D	Nip	24-DIC	TTL	-25...+75	<880		<70		TTL-OC
µPB 409 D-1	Nip	24-DIC	TTL	-25...+75	<880		<60		TTL-OC
µPB 409 D-2	Nip	24-DIC	TTL	-25...+75	<880		<50		TTL-OC
µPB 409 D-3	Nip	24-DIC	TTL	-25...+75	<880		<45		TTL-OC

82190 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPB 429 C	Nip	24-DIP	TTL	-25...+75	<880		<70		TTL-TS
µPB 429 C-1	Nip	24-DIP	TTL	-25...+75	<880		<60		TTL-TS
µPB 429 C-2	Nip	24-DIP	TTL	-25...+75	<880		<50		TTL-TS
µPB 429 C-3	Nip	24-DIP	TTL	-25...+75	<880		<45		TTL-TS
µPB 429 D	Nip	24-DIC	TTL	-25...+75	<880		<70		TTL-TS
µPB 429 D-1	Nip	24-DIC	TTL	-25...+75	<880		<60		TTL-TS
µPB 429 D-2	Nip	24-DIC	TTL	-25...+75	<880		<50		TTL-TS
µPB 429 D-3	Nip	24-DIC	TTL	-25...+75	<880		<45		TTL-TS

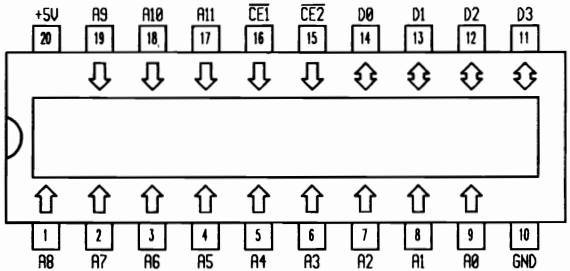
82190 — 2048x8-Bit PROM



82190 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87S190 V	Nsc	28-FLAT	TTL	0...+70	<962		<65		TTL-OC
DM 87S191 V	Nsc	28-FLAT	TTL	0...+70	<962		<65		TTL-TS
DM 87S290 V	Nsc	28-FLAT	TTL	0...+70	<962		<65		TTL-OC
DM 87S291 AV	Nsc	28-FLAT	TTL	0...+70	<962		<45		TTL-TS
DM 87S291 BV	Nsc	28-FLAT	TTL	0...+70	<962		<35		TTL-TS
DM 87S291 V	Nsc	28-FLAT	TTL	0...+70	<962		<65		TTL-TS
N 82HS191 A	Val	28-PLCC	TTL	0...+75	<919		<20		TTL-TS
N 82S191 A	Val	28-PLCC	TTL	0...+75	<919		<80		TTL-TS

82190 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S191A A	Val	28-PLCC	TTL	0...+75	<919		<55		TTL-TS
N 82S191C A	Val	28-PLCC	TTL	0...+75	<919		<35		TTL-TS
TS 71191A ME	Tho	28-LCC	NMOS	-55...+125	<1017		<60		TTL-TS
TS 71191B ME	Tho	28-LCC	NMOS	-55...+125	<1017		<45		TTL-TS
TS 71191C ME	Tho	28-LCC	NMOS	-55...+125	<1017		<35		TTL-TS
TS 71191 ME	Tho	28-LCC	NMOS	-55...+125	<1017		<80		TTL-TS
93Z510 LC	Fch	28-LCC	TTL	0...+75	<919		<45		TTL-OC
93Z510 LM	Fch	28-LCC	TTL	-55...+125	<962		<55		TTL-OC
93Z511 LC	Fch	28-LCC	TTL	0...+75	<919		<45		TTL-TS
93Z511 LM	Fch	28-LCC	TTL	-55...+125	<962		<55		TTL-TS
93Z611 LC	Fch	28-LCC	TTL	0...+75			<25		TTL-TS
93Z611 LM	Fch	28-LCC	TTL	-55...+125			<30		TTL-TS

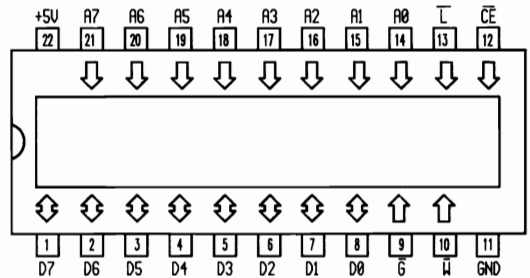
82195 — 4096x4-Bit PROM



82195 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S40	Amd	20-DIP	TTL	0...+75	<866		<50		TTL-OC
Am 27S40 A	Amd	20-DIP	TTL	0...+75	<866		<35		TTL-OC
Am 27S41	Amd	20-DIP	TTL	0...+75	<866		<50		TTL-TS
Am 27S41 A	Amd	20-DIP	TTL	0...+75	<866		<35		TTL-TS
DM 77S195 AJ	Nsc	20-DIC	TTL	-55...+125	<935		<60		TTL-TS
DM 77S195 BJ	Nsc	20-DIC	TTL	-55...+125	<935		<50		TTL-TS
DM 87S195 AJ	Nsc	20-DIC	TTL	0...+70	<935		<45		TTL-TS
DM 87S195 AN	Nsc	20-DIP	TTL	0...+70	<935		<45		TTL-TS

82195 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87S195 BJ	Nsc	20-DIC	TTL	0...+70	<935		<35		TTL-TS
DM 87S195 BN	Nsc	20-DIP	TTL	0...+70	<935		<35		TTL-TS
N 82HS195A D	Val	20-FLAT	TTL	0...+75	<761		<35		TTL-TS
N 82HS195A N	Val	20-DIP	TTL	0...+75	<761		<35		TTL-TS
N 82HS195B D	Val	20-FLAT	TTL	0...+75	<761		<25		TTL-TS
N 82HS195B N	Val	20-DIP	TTL	0...+75	<761		<25		TTL-TS
N 82HS195 D	Val	20-FLAT	TTL	0...+75	<761		<45		TTL-TS
N 82HS195 N	Val	20-DIP	TTL	0...+75	<761		<45		TTL-TS
63LS1640	Mmi	20-DIP	TTL	0...+75	63		66		TTL-OC
63PS1640	Mmi	20-DIP	TTL	0...+75	117	<131	45		TTL-OC
63S1640	Mmi	20-DIP	TTL	0...+75	117		46		TTL-OC
63LS1641	Mmi	20-DIP	TTL	0...+75	63		66		TTL-TS
63PS1641	Mmi	20-DIP	TTL	0...+75	117	<131	45		TTL-TS
63S1641	Mmi	20-DIP	TTL	0...+75	117		46		TTL-TS
63S1641 A	Mmi	20-DIP	TTL	0...+75	<919		<35		TTL-TS

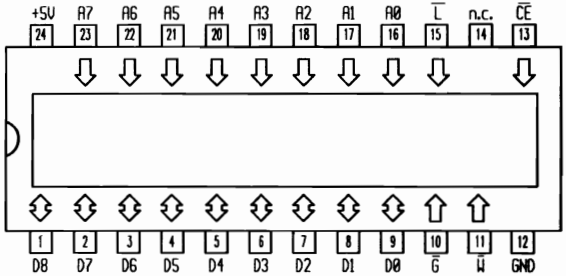
82208 — 258x8-Bit RAM (bipolar)



$\overline{W}$	$\overline{CE}$	$\overline{G}$	$\overline{L}$	D_n	Mode
X	X	H	X	Hi-Z	disable output
X	H	X	X	Hi-Z	disable read/write
L	L	H	X	data in	write
H	L	L	X	data out	read
X	X	X	H	—	transparent address
X	X	X	L	—	hold address

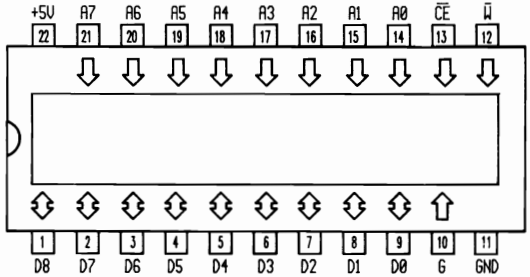
82208 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S208 F	Sig	22-DIC	TTL	0...+75	<971		<60		TTL-TS

82210 — 258x9-Bit RAM (bipolar)



W	CE	G	L	D_n	Mode
X	X	H	X	Hi-Z	disable output
X	H	X	X	Hi-Z	disable read/write
L	L	H	X	data in	write
H	L	L	X	data out	read
X	X	X	H	—	transparent address
X	X	X	L	—	hold address

82212 — 256x9-Bit RAM (bipolar)

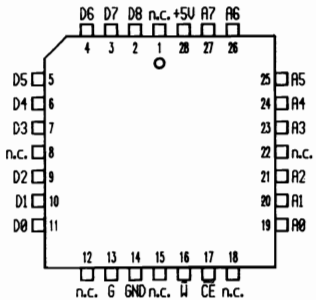


W	CE	G	D_{out}	Mode
X	X	H	Hi-Z	disable output
X	H	X	Hi-Z	disable read/write
L	L	H	data in	write
H	L	L	data out	read

82210 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S210 F	Sig	24-DIC	TTL	0...+75	<971		<60		TTL-TS
N 82S210 N	Sig	24-DIP	TTL	0...+75	<971		<60		TTL-TS

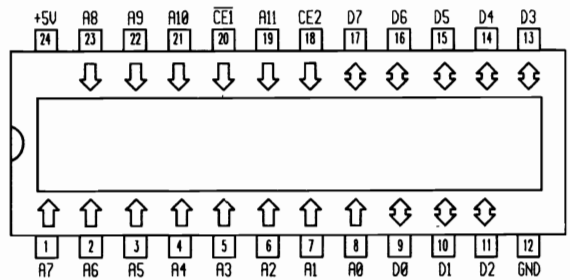
82212 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S212A N	Val	22-DIP	TTL	0...+75	<971		<35		TTL-TS
N 82S212 N	Val	22-DIP	TTL	0...+75	<971		<45		TTL-TS
93479 ADC	Fch	22-DIC	TTL	0...+75	<971		<35		TTL-TS
93479 ADM	Fch	22-DIC	TTL	-55...+125	<1100		<45		TTL-TS
93479 DC	Fch	22-DIC	TTL	0...+75	<971		<45		TTL-TS
93479 DM	Fch	22-DIC	TTL	-55...+125	<1100		<60		TTL-TS

82212 — 256x9-Bit RAM (bipolar)



$\overline{W}$	$\overline{CE}$	G	D_{out}	Mode
X	X	H	Hi-Z	disable output
X	H	X	Hi-Z	disable read/write
L	L	H	data in	write
H	L	L	data out	read

82321 — 4096x8-Bit PROM

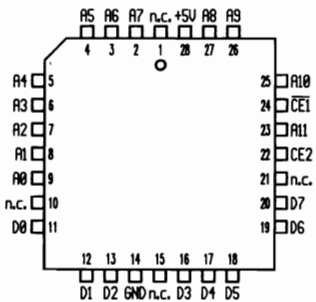


82212 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S212 A	Val	28-PLCC	TTL	0...+75	<971		<45		TTL-TS
N 82S212A A	Val	28-PLCC	TTL	0...+75	<971		<35		TTL-TS

82321 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
Am 27S43	Amd	24-DIP	TTL	0...+75	<971		<55		TTL-TS
Am 27S43 A	Amd	24-DIP	TTL	0...+75	<971		<40		TTL-TS
DM 77S321 J	Nsc	24-DIC	TTL	-55...+125	<1017		<65		TTL-TS
DM 77S421 J	Nsc	24-DIC	TTL	-55...+125	<1017		<65		TTL-TS
DM 87S321 AN	Nsc	24-DIP	TTL	0...+70	<971		<55		TTL-TS
DM 87S321 J	Nsc	24-DIC	TTL	0...+70	<1017		<55		TTL-TS
DM 87S321 N	Nsc	24-DIP	TTL	0...+70	<1017		<55		TTL-TS
DM 87S421 AN	Nsc	24-TDIP	TTL	0...+70	<971		<55		TTL-TS

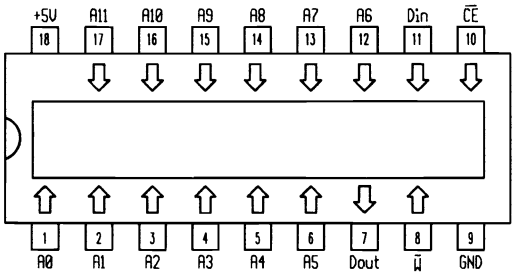
82321 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87S421 J	Nsc	24-TDIC	TTL	0...+70	<1017		<55		TTL-TS
DM 87S421 N	Nsc	24-TDIP	TTL	0...+70	<1017		<55		TTL-TS
MB 7141 E	Fui	24-DIP	TTL	0...+75	<971		<65		TTL-OC
MB 7141 H	Fui	24-DIP	TTL	0...+75	<971		<55		TTL-OC
MB 7141 N	Fui	24-DIP	TTL	0...+75	<971		<80		TTL-OC
MB 7142 E	Fui	24-DIP	TTL	0...+75	<971		<65		TTL-TS
MB 7142 H	Fui	24-DIP	TTL	0...+75	<971		<55		TTL-TS
MB 7142 N	Fui	24-DIP	TTL	0...+75	<971		<80		TTL-TS
N 82S321 N	Val	24-DIP	TTL	0...+75	<919		<70		TTL-TS
N 82HS321 N	Val	24-DIP	TTL	0...+75	<919		<45		TTL-TS
N 82HS321A N	Val	24-DIP	TTL	0...+75	<919		<35		TTL-TS
N 82HS321B N	Val	24-DIP	TTL	0...+75	<919		<30		TTL-TS
TS 71321B CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<55		TTL-TS
TS 71321B CP	Tho	24-DIP	NMOS	0...+70	<962,5		<55		TTL-TS
TS 71321C CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<45		TTL-TS
TS 71321C CP	Tho	24-DIP	NMOS	0...+70	<962,5		<45		TTL-TS
3632	Int	24-DIP	TTL	0...+75	<1017		<50		TTL-TS
3632-1	Int	24-DIP	TTL	0...+75	<1017		<40		TTL-TS
82S321	Int	24-DIP	TTL	0...+75	<919		<50		TTL-TS
82HS321	Int	24-DIP	TTL	0...+75	<919		<40		TTL-TS
63S3281 A	Mmi	24-DIP	TTL	0...+75	<997		<40		TTL-TS
63S3281	Mmi	24-DIP	TTL	0...+75	<997		<50		TTL-TS

82321 — 4096x8-Bit PROM



82321 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82HS321 A	Val	28-PLCC	TTL	0...+75	<919		<45		TTL-TS
N 82HS321A A	Val	28-PLCC	TTL	0...+75	<919		<35		TTL-TS
N 82HS321B A	Val	28-PLCC	TTL	0...+75	<919		<30		TTL-TS

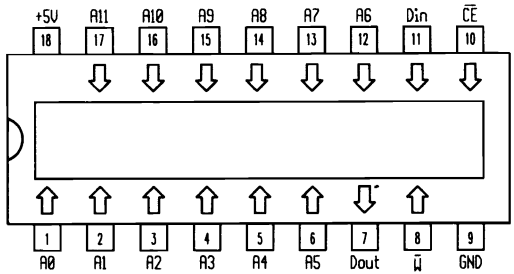
82400 — 4096x1-Bit RAM (bipolar)



CS	W	Din	Dout	Mode
H	X	X	H	not selected
L	L	L	H	write 0
L	L	H	H	write 1
L	H	X	data out	read

82400 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	$mW/bit	taa ns	tref ms	Output
N 82S400A I	Sig	18-DIC	TTL	0...+75	<814			<45		TTL-OC
N 82S400 I	Sig	18-DIC	TTL	0...+75	<814			<70		TTL-OC
SN 74S400 J	Tix	18-DIC	TTL	0...+60	500			75		TTL-OC
SN 74S400 N	Tix	18-DIP	TTL	0...+60	500			75		TTL-OC

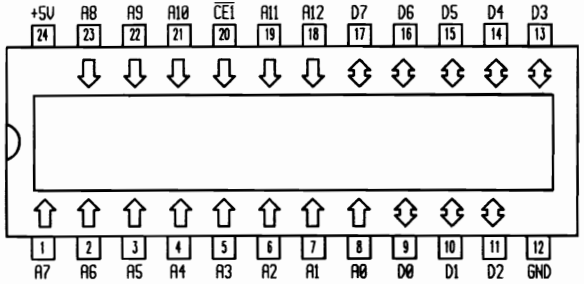
82400 — 4096x1-Bit RAM (bipolar)



CS	W	Din	Dout	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

82400 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	$mW/bit	taa ns	tref ms	Output
N 82S401A I	Sig	18-DIC	TTL	0...+75	<814			<45		TTL-TS
N 82S401 I	Sig	18-DIC	TTL	0...+75	<814			<70		TTL-TS
SN 74S401 J	Tix	18-DIC	TTL	0...+60	500			75		TTL-TS
SN 74S401 N	Tix	18-DIP	TTL	0...+60	500			75		TTL-TS

82641 — 8192x8-Bit PROM

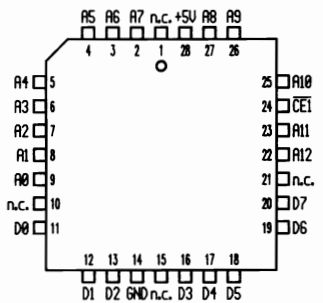


82641 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82HS641 N	Val	24-DIP	TTL	0...+75	<919		<55		TTL-TS
N 82HS641A N	Val	24-DIP	TTL	0...+75	<919		<45		TTL-TS
N 82HS641B N	Val	24-DIP	TTL	0...+75	<919		<35		TTL-TS
TS 71640 CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<55		TTL-OC
TS 71640 CP	Tho	24-DIP	NMOS	0...+70	<962,5		<55		TTL-OC
TS 71641 CJ	Tho	24-DIC	NMOS	0...+70	<962,5		<55		TTL-TS
TS 71641 CP	Tho	24-DIP	NMOS	0...+70	<962,5		<55		TTL-TS
93Z564 ADC	Fch	24-DIC	TTL	0...+75	<945		<45		TTL-OC

82641 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93Z564 ADM	Fch	24-DIC	TTL	-55...+125	<990		<55		TTL-OC
93Z564 DC	Fch	24-DIC	TTL	0...+75	<945		<55		TTL-OC
93Z564 DM	Fch	24-DIC	TTL	-55...+125	<990		<65		TTL-TS
93Z565 ADC	Fch	24-DIC	TTL	0...+75	<945		<45		TTL-TS
93Z565 ADM	Fch	24-DIC	TTL	-55...+125	<990		<55		TTL-TS
93Z565 DC	Fch	24-DIC	TTL	0...+75	<945		<55		TTL-TS
93Z565 DM	Fch	24-DIC	TTL	-55...+125	<990		<65		TTL-TS
93Z667 SDC	Fch	24-TDIC	TTL	0...+75			<40		TTL-TS
93Z667 SDM	Fch	24-TDIC	TTL	-55...+125			<45		TTL-TS

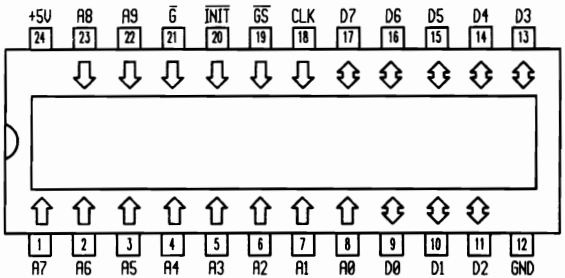
82641

8192x8-Bit PROM

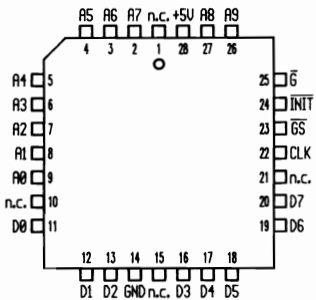


82641 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82HS641 A	Val	28-PLCC	TTL	0...+75	<919		<55		TTL-TS
N 82HS641A A	Val	28-PLCC	TTL	0...+75	<919		<45		TTL-TS
N 82HS641B A	Val	28-PLCC	TTL	0...+75	<919		<35		TTL-TS
93Z564 ALC	Fch	28-LCC	TTL	0...+75	<945		<45		TTL-OC
93Z564 ALM	Fch	28-LCC	TTL	-55...+125	<990		<55		TTL-OC
93Z564 LC	Fch	28-LCC	TTL	0...+75	<945		<55		TTL-OC
93Z564 LM	Fch	28-LCC	TTL	-55...+125	<990		<65		TTL-OC
93Z565 ALC	Fch	28-LCC	TTL	0...+75	<945		<45		TTL-TS
93Z565 ALM	Fch	28-LCC	TTL	-55...+125	<990		<55		TTL-TS
93Z565 LC	Fch	28-LCC	TTL	0...+75	<945		<55		TTL-TS
93Z565 LM	Fch	28-LCC	TTL	-55...+125	<990		<65		TTL-TS

87183	1024x8-Bit Register PROM



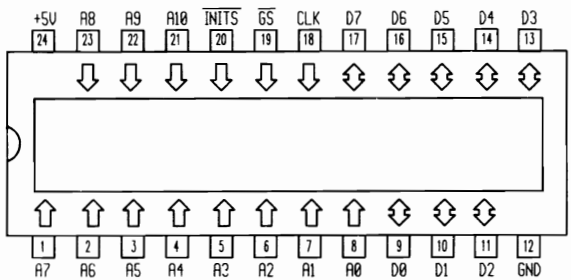
87183	1024x8-Bit Register PROM



87183 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77SR183 BJ	Nsc	24-TDIC	TTL	-55...+125	<1017		<40		TTL-TS
DM 77SR183 J	Nsc	24-DIC	TTL	-55...+125	<1017		<45		TTL-TS
DM 87SR183 BJ	Nsc	24-TDIC	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR183 BN	Nsc	24-TDIP	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR183 J	Nsc	24-TDIC	TTL	0...+70	<1017		<40		TTL-TS
DM 87SR183 N	Nsc	24-TDIP	TTL	0...+70	<1017		<40		TTL-TS

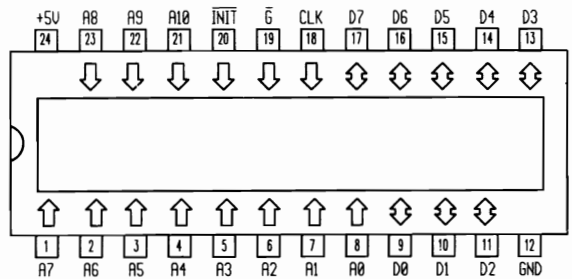
87183 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87SR183 BV	Nsc	28-FLAT	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR183 V	Nsc	28-FLAT	TTL	0...+70	<1017		<40		TTL-TS

87191 — 2048x8-Bit Register PROM



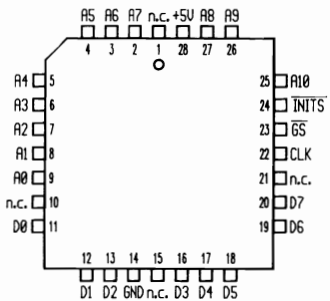
87191 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77SR191 J	Nsc	24-TDIC	TTL	-55...+125	<1045		<35		TTL-TS
DM 87SR191 J	Nsc	24-TDIC	TTL	0...+70	<1045		<25		TTL-TS
DM 87SR191 N	Nsc	24-TDIP	TTL	0...+70	<1045		<25		TTL-TS
TBP 28R165 J	Tix	24-DIC	TTL	0...+70	<735		20		TTL-TS
TBP 28R165 MJ	Tix	24-DIC	TTL	-55...+125	<770		20		TTL-TS
TBP 28R165 N	Tix	24-DIP	TTL	0...+70	<735		20		TTL-TS

87191 — 2048x8-Bit Register PROM



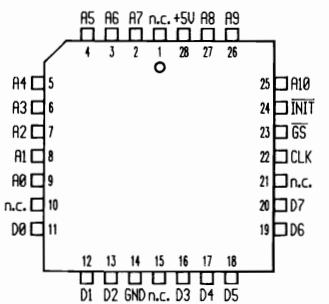
87191 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77SR193 J	Nsc	24-TDIC	TTL	-55...+125	<1045		<35		TTL-TS
DM 87SR193 J	Nsc	24-TDIC	TTL	0...+70	<1045		<25		TTL-TS
DM 87SR193 N	Nsc	24-TDIP	TTL	0...+70	<1045		<25		TTL-TS

87191	2048x8-Bit Register PROM



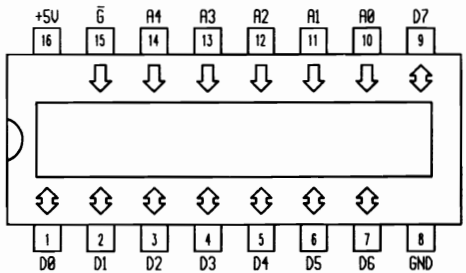
87191 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87SR191 V	Nsc	28-FLAT	TTL	0...+70	<1045		<25		TTL-TS

87191	2048x8-Bit Register PROM



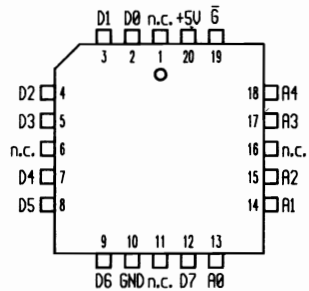
87191 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87SR193 V	Nsc	28-FLAT	TTL	0...+70	<1045		<25		TTL-TS

87288 — 32x8-Bit PROM



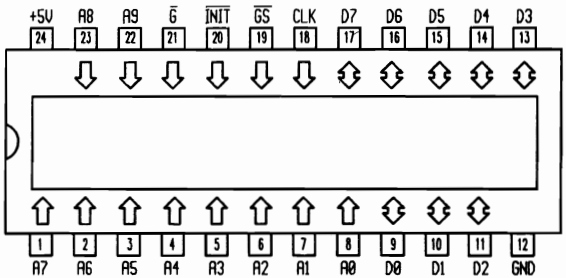
87288 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
PL 77X288 BJ	Nsc	16-DIC	TTL	-55...+125	<770		<20		TTL-TS
PL 87X288 BJ	Nsc	16-DIC	TTL	0...+70	<770		<15		TTL-TS
PL 87X288 BN	Nsc	16-DIP	TTL	0...+70	<770		<15		TTL-TS

87288 — 32x8-Bit PROM



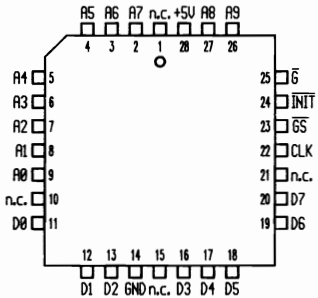
87288 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 74S387 AN	Nsc	20-FLAT	TTL	0...+70	<770		<15		TTL-TS
PL 87X288 BV	Nsc	20-FLAT	TTL	0...+70	<770		<15		TTL-TS

87474	512x8-Bit Register PROM



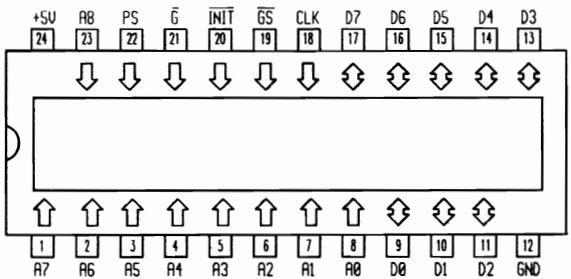
87474	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
Type					$mW/bit				
DM 77SR474 BJ	Nsc	24-TDIC	TTL	-55...+125	<1017		<40		TTL-TS
DM 77SR474 J	Nsc	24-TDIC	TTL	-55...+125	<1017		<55		TTL-TS
DM 87SR474 BJ	Nsc	24-TDIC	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR474 BN	Nsc	24-TDIP	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR474 J	Nsc	24-TDIC	TTL	0...+70	<1017		<50		TTL-TS
DM 87SR474 N	Nsc	24-TDIP	TTL	0...+70	<1017		<50		TTL-TS

87474	512x8-Bit Register PROM



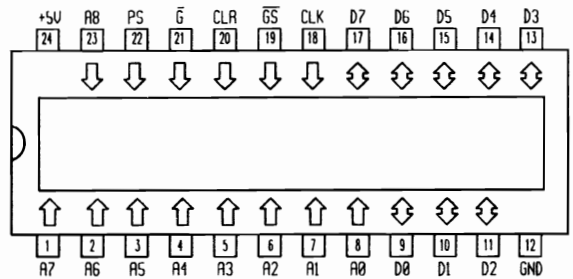
87474	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
Type					$mW/bit				
DM 87SR474 BV	Nsc	28-FLAT	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR474 V	Nsc	28-FLAT	TTL	0...+70	<1017		<50		TTL-TS

87476 — 512x8-Bit Register PROM



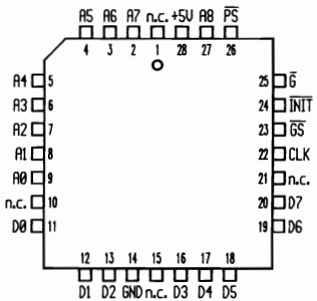
87476 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77SR476 BJ	Nsc	24-TDIC	TTL	-55...+125	<1017		<40		TTL-TS
DM 77SR476 J	Nsc	24-TDIC	TTL	-55...+125	<1017		<55		TTL-TS
DM 87SR476 BJ	Nsc	24-TDIC	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR476 BN	Nsc	24-TDIP	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR476 J	Nsc	24-TDIC	TTL	0...+70	<1017		<50		TTL-TS
DM 87SR476 N	Nsc	24-TDIP	TTL	0...+70	<1017		<50		TTL-TS

87476 — 512x8-Bit Register PROM



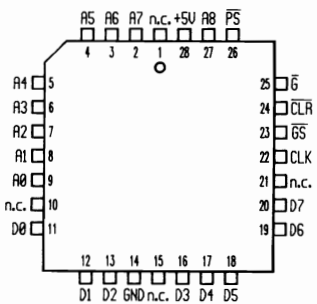
87476 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 77SR25 BJ	Nsc	24-TDIC	TTL	-55...+125	<1017		<40		TTL-TS
DM 77SR25 J	Nsc	24-TDIC	TTL	-55...+125	<1017		<55		TTL-TS
DM 87SR25 BJ	Nsc	24-TDIC	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR25 BN	Nsc	24-TDIP	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR25 J	Nsc	24-TDIC	TTL	0...+70	<1017		<50		TTL-TS
DM 87SR25 N	Nsc	24-TDIP	TTL	0...+70	<1017		<50		TTL-TS

87476 — 512x8-Bit Register PROM



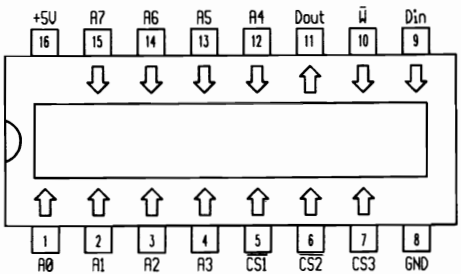
87476 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87SR476 BV	Nsc	28-FLAT	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR476 V	Nsc	28-FLAT	TTL	0...+70	<1017		<50		TTL-TS

87476 — 512x8-Bit Register PROM



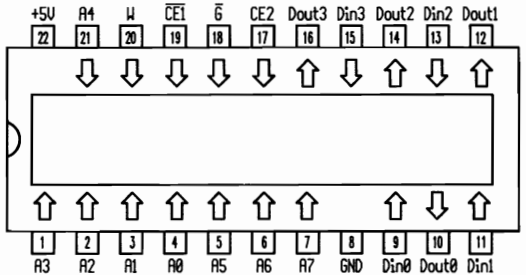
87476 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 87SR25 BV	Nsc	28-FLAT	TTL	0...+70	<1017		<35		TTL-TS
DM 87SR25 V	Nsc	28-FLAT	TTL	0...+70	<1017		<50		TTL-TS

93410 — 256x1-Bit RAM (bipolar)



$\overline{CS}_{1,2}$	CS3	$\overline{W}$	D_{in}	D_{out}	Mode
one H	X	X	X	H	not selected
both L	H	L	L	H	write »0«
both L	H	L	H	H	write »1«
both L	H	H	X	data out	read

93412 — 256x4-Bit RAM (bipolar)

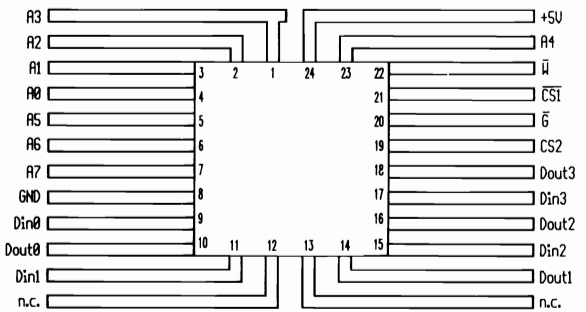


$\overline{CE1}$	CE2	$\overline{G}$	W	D_{out}	Mode
H	X	X	X	Hi-Z	not selected
X	L	X	X	Hi-Z	not selected
X	X	H	H	Hi-Z	output disabled
L	H	H	L	Hi-Z	write
L	H	L	L	data in	write
L	H	L	H	data out	read

93410 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93410A DC	Fch	16-DIC	TTL	0...+75	450		<45		TTL-OC
93410 DC	Fch	16-DIC	TTL	0...+75	450		<60		TTL-OC
93410 DM	Fch	16-DIC	TTL	-55...+125	450		<70		TTL-OC
93410A FC	Fch	16-FLAT	TTL	0...+75	450		<45		TTL-OC
93410 FC	Fch	16-FLAT	TTL	0...+75	450		<60		TTL-OC
93410 FM	Fch	16-FLAT	TTL	-55...+125	450		<70		TTL-OC
93410A PC	Fch	16-DIP	TTL	0...+75	450		<45		TTL-OC
93410 PC	Fch	16-DIP	TTL	0...+75	450		<60		TTL-OC

93412 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MCM 93412	Mot	22-DIP	TTL	0...+75	<892		<45		TTL-OC
MCM 93422	Mot	22-DIP	TTL	0...+75	<892		<45		TTL-TS
93412 DC	Fch	22-DIC	TTL	0...+75	<775		<45		TTL-OC
93L412 DC	Fch	22-DIC	TTL	0...+75	250		<60		TTL-OC
93L412 DM	Fch	22-DIC	TTL	-55...+125	250		<75		TTL-OC
93412 DM	Fch	22-DIC	TTL	-55...+125	<850		<60		TTL-OC
93412 PC	Fch	22-DIP	TTL	0...+75	<775		<45		TTL-OC
93422 ADC	Fch	22-DIC	TTL	0...+75	<600		<35		TTL-TS

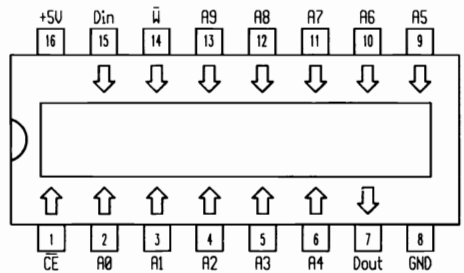
93412 Type	Man	Case	Techn.	Tu°C	P_{typ} mW / P standby mW $ / mW/bit	t_{aa} ns	t_{ref} ms	Output
93422 ADM	Fch	22-DIC	TTL	-55...+125	<715	<45		TTL-TS
93422 APC	Fch	22-DIP	TTL	0...+75	<600	<35		TTL-TS
93422 DC	Fch	22-DIC	TTL	0...+75	<600	<45		TTL-TS
93422 DM	Fch	22-DIC	TTL	-55...+125	<715	<60		TTL-TS
93L422 ADC	Fch	22-DIC	TTL	0...+75	<400	<45		TTL-TS
93L422 ADM	Fch	22-DIC	TTL	-55...+125	<495	<55		TTL-TS
93L422 APC	Fch	22-DIP	TTL	0...+75	<400	<45		TTL-TS
93L422 DC	Fch	22-DIC	TTL	0...+75	<400	<60		TTL-TS
93L422 DM	Fch	22-DIC	TTL	-55...+125	<495	<75		TTL-TS
93L422 PC	Fch	22-DIP	TTL	0...+75	<400	<60		TTL-TS
93422 PC	Fch	22-DIP	TTL	0...+75	<600	<45		TTL-TS



$\overline{CE1}$	CE2	$\overline{G}$	W	D_{out}	Mode
H	X	X	X	Hi-Z	not selected
X	L	X	X	Hi-Z	not selected
X	X	H	H	Hi-Z	output disabled
L	H	H	L	Hi-Z	write
L	H	L	L	data in	write
L	H	L	H	data out	read

93412 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93412 FC	Fch	24-PLCC	TTL	0...+75	<775		<45		TTL-OC
93L412 FC	Fch	24-PLCC	TTL	0...+75	250		<60		TTL-OC
93L412 FM	Fch	24-PLCC	TTL	-55...+125	250		<75		TTL-OC
93412 FM	Fch	24-PLCC	TTL	-55...+125	<850		<60		TTL-OC
93422 AFC	Fch	24-PLCC	TTL	0...+75	<600		<35		TTL-TS
93422 AFM	Fch	24-PLCC	TTL	-55...+125	<715		<45		TTL-TS
93422 ALC	Fch	24-LCC	TTL	0...+75	<600		<35		TTL-TS
93422 ALM	Fch	24-LCC	TTL	-55...+125	<715		<45		TTL-TS
93422 FC	Fch	24-PLCC	TTL	0...+75	<600		<45		TTL-TS
93422 FM	Fch	24-PLCC	TTL	-55...+125	<715		<60		TTL-TS
93L422 AFC	Fch	24-PLCC	TTL	0...+75	<400		<45		TTL-TS
93L422 AFM	Fch	24-PLCC	TTL	-55...+125	<495		<55		TTL-TS
93L422 ALC	Fch	24-LCC	TTL	0...+75	<400		<45		TTL-TS
93L422 ALM	Fch	24-LCC	TTL	-55...+125	<495		<55		TTL-TS
93422 LC	Fch	24-LCC	TTL	0...+75	<600		<45		TTL-TS
93L422 FC	Fch	24-PLCC	TTL	0...+75	<400		<60		TTL-TS
93L422 FM	Fch	24-PLCC	TTL	-55...+125	<495		<75		TTL-TS
93L422 LC	Fch	24-LCC	TTL	0...+75	<400		<60		TTL-TS
93L422 LM	Fch	24-LCC	TTL	-55...+125	<495		<75		TTL-TS
93422 LM	Fch	24-LCC	TTL	-55...+125	<715		<60		TTL-TS

93425 — 1024x1-Bit RAM (bipolar)

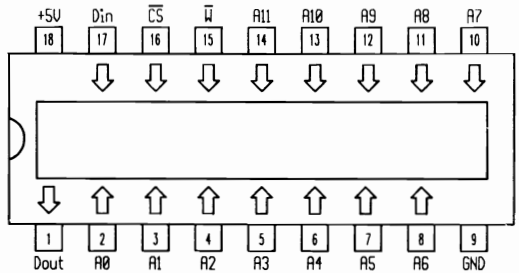


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

93425 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93425 DC-20	Fch	16-DIC	TTL	0...+75	<656		<20		TTL-TS
93425 DC-25	Fch	16-DIC	TTL	0...+75	<656		<25		TTL-TS
93425 DC-30	Fch	16-DIC	TTL	0...+75	<656		<30		TTL-TS
93425 DM-30	Fch	16-DIC	TTL	-55...+125	<742		<30		TTL-TS
93425 DM-40	Fch	16-DIC	TTL	-55...+125	<742		<40		TTL-TS
93425 FC-20	Fch	16-FLAT	TTL	0...+75	<656		<20		TTL-TS
93425 FC-25	Fch	16-FLAT	TTL	0...+75	<656		<25		TTL-TS
93425 FC-30	Fch	16-FLAT	TTL	0...+75	<656		<30		TTL-TS

93425 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93425 FM-30	Fch	16-FLAT	TTL	-55...+125	<742		<30		TTL-TS
93425 FM-40	Fch	16-FLAT	TTL	-55...+125	<742		<40		TTL-TS
93L425 DC-35	Fch	16-DIC	TTL	0...+75	<341		<35		TTL-TS
93L425 DC-45	Fch	16-DIC	TTL	0...+75	<341		<45		TTL-TS
93L425 DM-40	Fch	16-DIC	TTL	-55...+125	<412		<40		TTL-TS
93L425 DM-50	Fch	16-DIC	TTL	-55...+125	<412		<50		TTL-TS
93L425 FC-35	Fch	16-FLAT	TTL	0...+75	<341		<35		TTL-TS
93L425 FC-45	Fch	16-FLAT	TTL	0...+75	<341		<45		TTL-TS
93L425 FM-40	Fch	16-FLAT	TTL	-55...+125	<412		<40		TTL-TS
93L425 FM-50	Fch	16-FLAT	TTL	-55...+125	<412		<50		TTL-TS
93L425 PC-35	Fch	16-DIP	TTL	0...+75	<341		<35		TTL-TS
93L425 PC-45	Fch	16-DIP	TTL	0...+75	<341		<45		TTL-TS
93425 PC-20	Fch	16-DIP	TTL	0...+75	<656		<20		TTL-TS
93425 PC-25	Fch	16-DIP	TTL	0...+75	<656		<25		TTL-TS
93425 PC-30	Fch	16-DIP	TTL	0...+75	<656		<30		TTL-TS

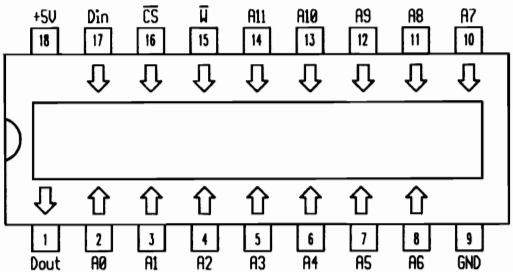
93470 — 4096x1-Bit RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	H	not selected
L	L	L	H	write 0
L	L	H	H	write 1
L	H	X	data out	read

93470 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93470 DC	Fch	18-DIC	TTL	0...+75	<850		<45		TTL-OC
93470 DM	Fch	18-DIC	TTL	-55...+125	<900		<60		TTL-OC
93L470 DC	Fch	18-DIC	TTL	0...+75	400		40		TTL-OC
93L470 DM	Fch	18-DIC	TTL	-55...+125	430		40		TTL-OC
93L470 FC	Fch	18-FLAT	TTL	0...+75	400		40		TTL-OC
93L470 PC	Fch	18-DIP	TTL	0...+75	400		40		TTL-OC
93470 PC	Fch	18-DIP	TTL	0...+75	<850		<45		TTL-OC

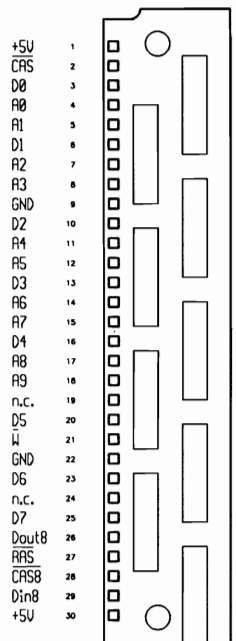
93470 — 4096x1-Bit RAM (bipolar)



CS	W	D_{in}	D_{out}	Mode
H	X	X	Hi-Z	not selected
L	L	L	Hi-Z	write 0
L	L	H	Hi-Z	write 1
L	H	X	data out	read

93470 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
93471 DC	Fch	18-DIC	TTL	0...+75	<850		<45		TTL-TS
93471 DM	Fch	18-DIC	TTL	-55...+125	<900		<60		TTL-TS
93L471 DC	Fch	18-DIC	TTL	0...+75	400		40		TTL-TS
93L471 DM	Fch	18-DIC	TTL	-55...+125	430		40		TTL-TS
93L471 FC	Fch	18-FLAT	TTL	0...+75	400		40		TTL-TS
93L471 PC	Fch	18-DIP	TTL	0...+75	400		40		TTL-TS
93471 PC	Fch	18-DIP	TTL	0...+75	<850		<45		TTL-TS

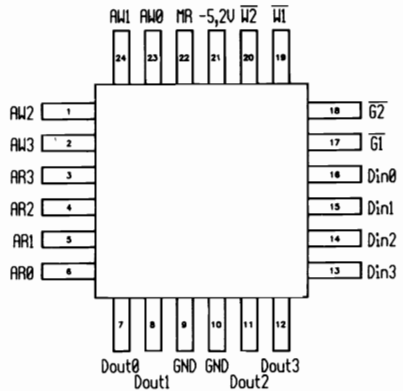
94000 — 4194304x9-Bit dynamic RAM-Modul



94000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYM 94000 S-10	Sie	30-SIC	NMOS	0...+70	<3960	<99	<100	<16	TTL-TS
HYM 94000 S-80	Sie	30-SIC	NMOS	0...+70	<4455	<99	<80	<16	TTL-TS

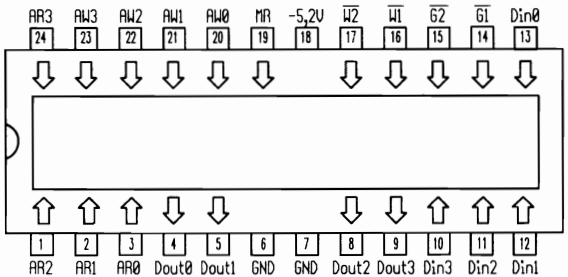
100145

16x4-Bit Register RAM



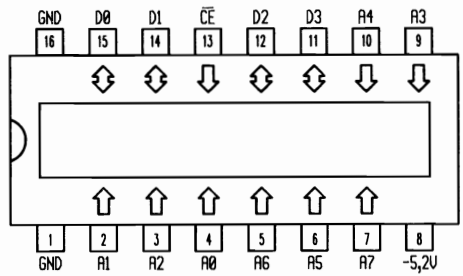
100145 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100145 FC	Fch	24-PLCC	ECL	0...+85	<1284		<7		ECL

100145 — 16x4-Bit Register RAM



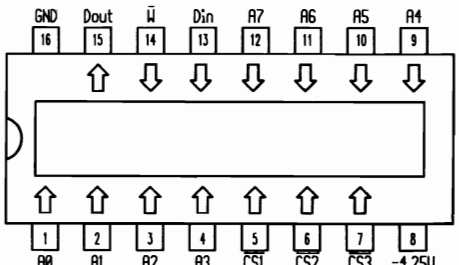
100145 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / $P_{standby}$ mW $/bit	t_{aa} ns	t_{ref} ms	Output
F 100145 DC	Fch	24-TDIC	ECL	0...+85	<1284	<7		ECL

100149 — 256x4-Bit PROM



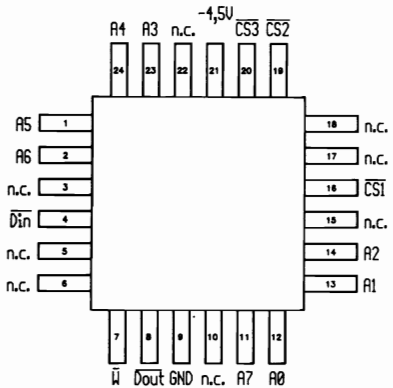
100149 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / $P_{standby}$ mW $/bit	t_{aa} ns	t_{ref} ms	Output
100149A F	Val	16-DIC	ECL	0...+75	<720	<10		ECL
100149 F	Val	16-DIC	ECL	0...+75	<810	<20		ECL

100414 — 256x1-Bit RAM (bipolar)



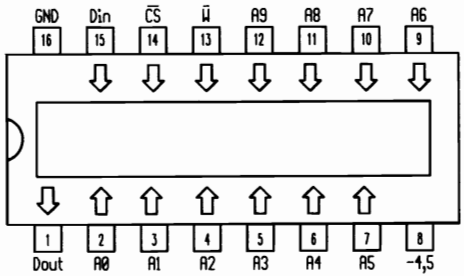
100414 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100414 DC	Fch	16-DIP	ECL	0...+85	<630		<10		ECL

100414 — 256x1-Bit RAM (bipolar)



100414 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100414 FC	Fch	24-PLCC	ECL	0...+85	<630		<10		ECL

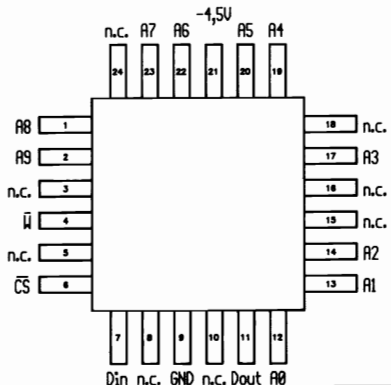
100415 — 1024x1-Bit RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100415 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100415 DC	Fch	16-DIC	ECL	0...+85	<900		<10		ECL
F 100415 FC	Fch	16-FLAT	ECL	0...+85	<900		<10		ECL
HM 100415	Hit	16-DIC	ECL	0...+85	$0,6		<10		ECL
100415 B	Val	16-DIP	ECL	0...+85	520		<10		ECL

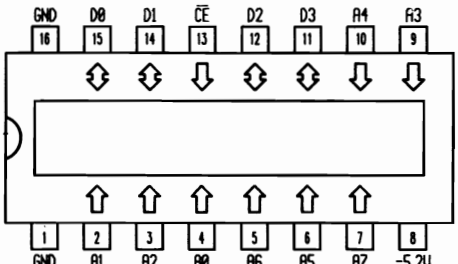
100415 — 1024x1-Bit RAM (bipolar)



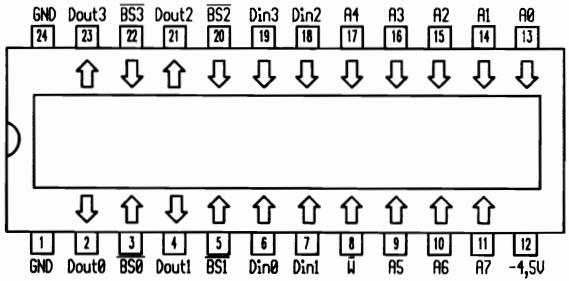
$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100415 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100415 FC	Fch	24-PLCC	ECL	0...+85	<675		<20		ECL

100416 — 256x4-Bit PROM



100422 — 256x4-Bit RAM (bipolar)

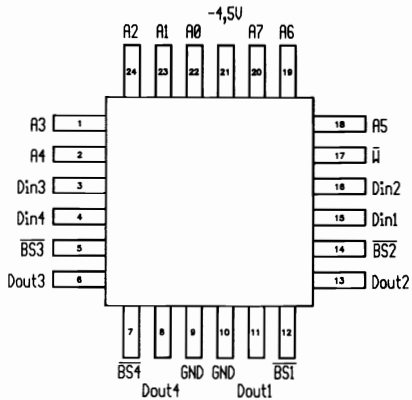


$\overline{BS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100416 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100416 FC	Fch	16-FLAT	ECL	0...+85	<675		<20		ECL

100422 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
DM 100422 AJ	Nsc	24-DIC	ECL	0...+85	<900		<10		ECL
DM 100422 J	Nsc	24-DIC	ECL	0...+85	<900		<12		ECL
HM 100422	Hit	24-DIC	ECL	0...+85	$0,8		<10		ECL

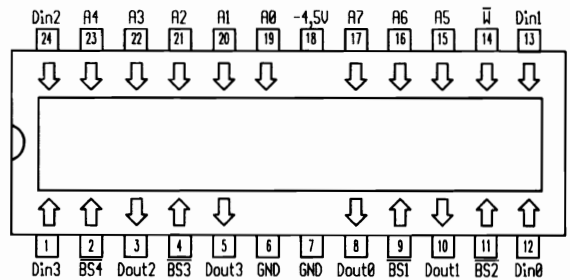
100422 — 256x4-Bit RAM (bipolar)



CS	W	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100422 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 100422 AW	Nsc	24-PLCC	ECL	0...+85	<900		<10		ECL
DM 100422 W	Nsc	24-PLCC	ECL	0...+85	<900		<12		ECL
F 100422 FC	Fch	24-FLAT	ECL	0...+85	<1035		<10		ECL
HM 100422 F	Hit	24-PLCC	ECL	0...+85	$0,8		<10		ECL
µPB 100422 B-10	Nec	24-FLAT	ECL	0...+85	<1000		<10		ECL
µPB 100422 B-7	Nec	24-FLAT	ECL	0...+85	<1000		<7		ECL

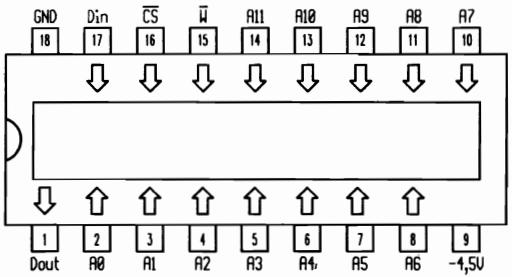
100422 — 256x4-Bit RAM (bipolar)



CS	W	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

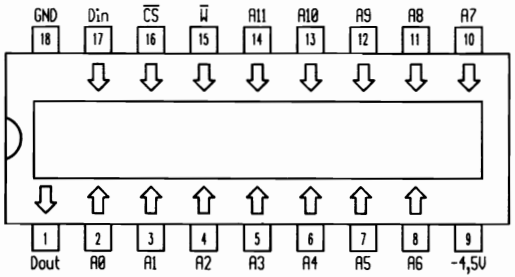
100422 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100422 DC	Fch	24-TDIC	ECL	0...+85	<1035		<10		ECL
100422 B	Val	24-DIC	ECL	0...+85	<945		<10		ECL
100422 C	Val	24-DIC	ECL	0...+85	<945		<7		ECL
µPB 100422 D-10	Nec	24-DIC	ECL	0...+85	<1000		<10		ECL
µPB 100422 D-7	Nec	24-DIC	ECL	0...+85	<1000		<7		ECL

100470 — 4096x1-Bit ECL RAM (bipolar)



100470 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPB 100470 D-10	Nec	18-DIC	ECL	0...+85	<1000		<10		ECL
µPB 100470 D-15	Nec	18-DIC	ECL	0...+85	<1000		<15		ECL

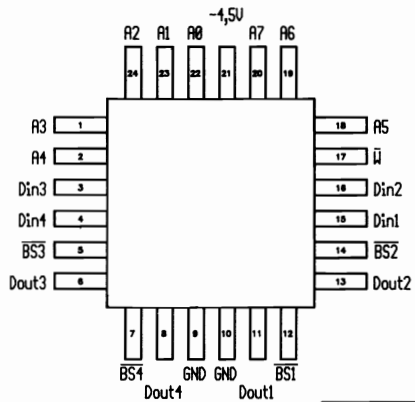
100470 — 4096x1-Bit RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100470 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
DM 100470 AJ	Nsc	18-DIC	ECL	0...+85	<900		<15		ECL
DM 100470 J	Nsc	18-DIC	ECL	0...+85	<900		<25		ECL
F 100470 DC	Fch	18-DIC	ECL	0...+85	<877		<35		ECL
F 100470 FC	Fch	18-FLAT	ECL	0...+85	<877		<35		ECL
HM 100470	Hit	18-DIC	ECL	0...+85	$0,2		<25		ECL
100470 A	Val	18-DIC	ECL	0...+85	<675		<15		ECL

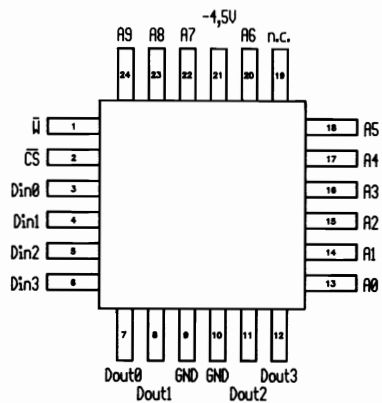
100474 — 1024x4-Bit ECL RAM (bipolar)



CS	W	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100474 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPB 100474 K-45	Nec	24-CLCC	ECL	0...+85	<2000		<4.5		ECL
µPB 100474 K-50	Nec	24-CLCC	ECL	0...+85	<2000		<5		ECL
µPB 100474 K-60	Nec	24-CLCC	ECL	0...+85	<2000		<6		ECL

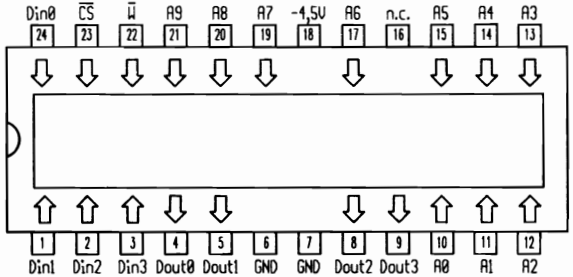
100474 — 1024x4-Bit RAM (bipolar)



CS	W	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100474 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100474 FC	Fch	24-PLCC	ECL	0...+85	$0,25		<10		ECL
HM 100474 F	Hit	24-PLCC	ECL	0...+85	$0,2		<25		ECL
HM 100474 F-10	Hit	24-FLAT	ECL	0...+75	<924		<10		ECL
HM 100474 F-8	Hit	24-FLAT	ECL	0...+75	<924		<8		ECL
µPB 100474 B-10	Nec	24-FLAT	ECL	0...+85	<1000		<10		ECL
µPB 100474 B-15	Nec	24-FLAT	ECL	0...+85	<1000		<15		ECL
µPB 100474 B-45	Nec	24-FLAT	ECL	0...+85	<2000		<4.5		ECL
µPB 100474 B-50	Nec	24-FLAT	ECL	0...+85	<2000		<5		ECL
µPB 100474 B-60	Nec	24-FLAT	ECL	0...+85	<2000		<6		ECL
µPB 100474 B-8	Nec	24-FLAT	ECL	0...+85	<1000		<8		ECL
µPB 100474 B-9	Nec	24-FLAT	ECL	0...+85	<1000		<9		ECL

100474 — 1024x4-Bit RAM (bipolar)

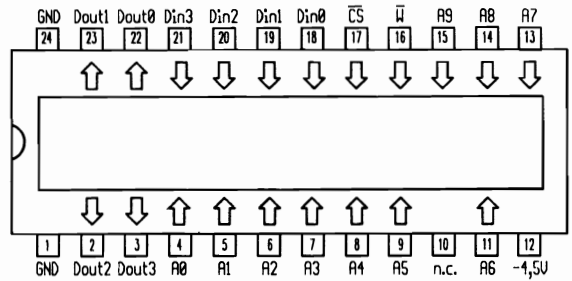


$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100474 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
F 100474 DC	Fch	24-TDIC	ECL	0...+85	$0,25		<10		ECL
HM 100474	Hit	24-DIC	ECL	0...+85	$0,2		<25		ECL
HM 100474-10	Hit	24-DIC	ECL	0...+75	<924		<10		ECL
HM 100474-8	Hit	24-DIC	ECL	0...+75	<924		<8		ECL
100474 A	Val	24-DIC	ECL	0...+85	<945		<15		ECL
µPB 100474 D-10	Nec	24-DIC	ECL	0...+85	<1000		<10		ECL
µPB 100474 D-15	Nec	24-DIC	ECL	0...+85	<1000		<15		ECL
µPB 100474 D-8	Nec	24-DIC	ECL	0...+85	<1000		<8		ECL

100474 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
µPB 100474 D-9	Nec	24-DIC	ECL	0...+85	<1000	<9		ECL

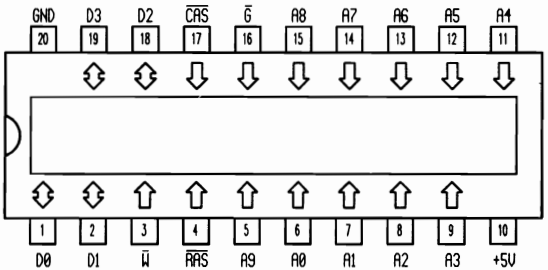
100474 — 1024x4-Bit RAM (bipolar)



$\overline{CS}$	$\overline{W}$	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100474 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
DM 100474 AD	Nsc	24-DIC	ECL	0...+85	<990	<15		ECL
DM 100474 D	Nsc	24-DIC	ECL	0...+85	<900	<25		ECL

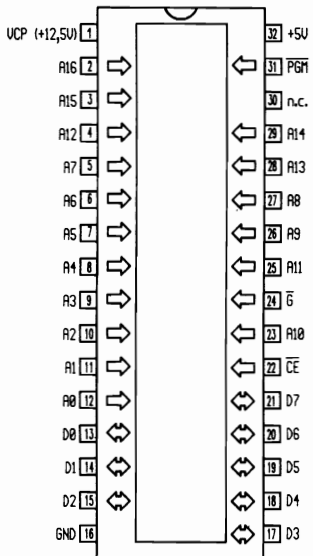
100480 — 16384x1-Bit ECL RAM (bipolar)



CS	W	D_{in}	D_{out}	Mode
H	X	X	L	disable
L	L	L	L	write 0
L	L	H	L	write 1
L	H	X	data out	read

100480 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 100480-15	Hit	20-DIC	ECL	0...+75	<990		<15		ECL
HM 100480 F-15	Hit	20-FLAT	ECL	0...+75	<990		<15		ECL

271023 — 131072x8-Bit EPROM



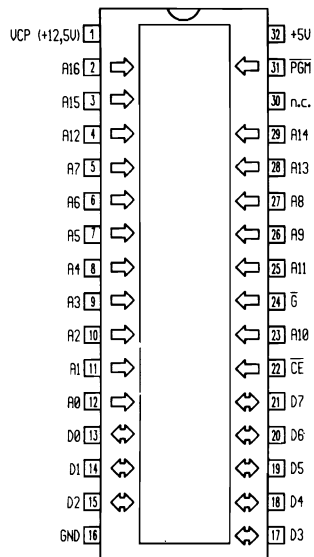
- Pro Adresse ein 10ms-Impuls für Einzelprogrammierung oder für interaktives Programmieren mit 0,5ms-Impulsen bis zu 20 Impulse (10ms!).
- Per address a single 10 ms pulse for single programming or interactive programming with 0.5 ms pulse up to 20 pulses (10 ms!)
- Une impulsion de 10 ms pour chaque adresse et pour une programmation individuelle ou pour une programmation interactive des impulsions de 0,5 ms et pouvant aller jusqu'á 20 impulsions (10 ms!).
- Per ogni indirizzo un impulso 10 ms per programmazione sinola oppure per programmazione interattiva con 0,5 ms-impulsi fino a 20 impulsi (10 ms!).
- Para programación individual un pulso de 10 ms por cada dirección a programar; o para programación interactiva con pulsos e 0,5 ms hasta 20 pulsos (10 ms!).

CE	G	PGM	V_{pp}	V_{cc}	D_n	Mode
L	L	H	+5V	+5V	data out	read
H	X	X	+5V	+5V	Hi-Z	standby
L	H	⊓ *	+12,5V	+6V	data in	program
L	L	H	+12,5V	+6V	data out	program verify
H	X	X	+12,5V	+6V	Hi-Z	program inhibit

271023 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 27C101 G-20	Hit	32-DIC	CMOS	0...+70	<165		<200		TTL-TS
HN 27C101 G-25	Hit	32-DIC	CMOS	0...+70	<165		<250		TTL-TS
NMC 27C1023 Q120	Nsc	32-DIC	CMOS	0...+70	<165	<0,55	<120		TTL-TS
NMC 27C1023 Q150	Nsc	32-DIC	CMOS	0...+70	<165	<0,55	<150		TTL-TS
NMC 27C1023 Q200	Nsc	32-DIC	CMOS	0...+70	<165	<0,55	<200		TTL-TS
NMC 27C1023 Q90	Nsc	32-DIC	CMOS	0...+70	<165	<0,55	<90		TTL-TS
NMC 27C1023 QE120	Nsc	32-DIC	CMOS	-40...+85	<165	<0,55	<120		TTL-TS
NMC 27C1023 QM150	Nsc	32-DIC	CMOS	-55...+125	<165	<0,55	<150		TTL-TS
SMJ 27C010-25 J	Tix	32-DIC	CMOS	-55...+125	<220	<1,5	<250		TTL-TS
SMJ 27C010-30 J	Tix	32-DIC	CMOS	-55...+125	<220	<1,5	<300		TTL-TS
ST 27C1001	Sgs	32-DIC	CMOS	0...+70	<275		<120		TTL-TS
TC 571000 D-17	Tos	32-DIP	CMOS	-40...+85	<157,5	<5,25	<170		TTL-TS
TC 571000 D-20	Tos	32-DIP	CMOS	-40...+85	<157,5	<5,25	<200		TTL-TS
TC 571000 D-200	Tos	32-DIP	CMOS	0...+70	<165	<5,5	<200		TTL-TS
TC 571000 D-25	Tos	32-DIP	CMOS	-40...+85	<157,5	<5,25	<250		TTL-TS
TMS 27C010-170 JL	Tix	32-DIC	CMOS	0...+70	<210	<2,75	<170		TTL-TS
TMS 27C010-200 JL	Tix	32-DIC	CMOS	0...+70	<210	<2,75	<200		TTL-TS
TMS 27C010-20 JL	Tix	32-DIC	CMOS	0...+70	<220	<2,75	<200		TTL-TS
TMS 27C010-250 JL	Tix	32-DIC	CMOS	0...+70	<210	<2,75	<250		TTL-TS
TMS 27C010-25 JL	Tix	32-DIC	CMOS	0...+70	<220	<2,75	<250		TTL-TS
TMS 27C010-300 JL	Tix	32-DIC	CMOS	0...+70	<210	<2,75	<300		TTL-TS
TMS 27C010-30 JL	Tix	32-DIC	CMOS	0...+70	<220	<2,75	<300		TTL-TS
TS 27C1001-12 C	Tho	32-DIC	CMOS	0...+70	<275		<120		TTL-TS
TS 27C1001-12 V	Tho	32-DIC	CMOS	-40...+85	<275		<120		TTL-TS
TS 27C1001-15 C	Tho	32-DIC	CMOS	0...+70	<275		<150		TTL-TS
TS 27C1001-15 V	Tho	32-DIC	CMOS	-40...+85	<275		<150		TTL-TS
TS 27C1001-20 C	Tho	32-DIC	CMOS	0...+70	<275		<200		TTL-TS
TS 27C1001-20 V	Tho	32-DIC	CMOS	-40...+85	<275		<200		TTL-TS
TS 27C1001-25 C	Tho	32-DIC	CMOS	0...+70	<275		<250		TTL-TS
TS 27C1001-25 V	Tho	32-DIC	CMOS	-40...+85	<275		<250		TTL-TS

271023

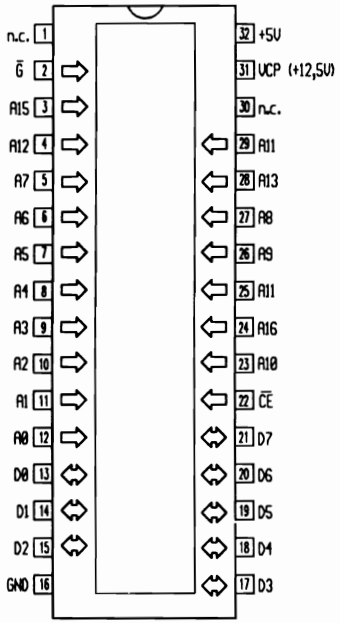
131072x8-Bit PROM



- Pro Adresse ein 10ms-Impuls für Einzelprogrammierung oder für interaktives Programmieren mit 0,5ms-Impulsen bis zu 20 Impulse (10ms!).
- Per address a single 10 ms pulse for single programming or interactive programming with 0.5 ms pulse up to 20 pulses (10 ms!)
- Une impulsion de 10 ms pour chaque adresse et pour une programmation individuelle ou pour une programmation interactive des impulsions de 0,5 ms et pouvant aller jusqu'á 20 impulsions (10 ms!).
- Per ogni indirizzo un impulso 10 ms per programmazione sinola oppure per programmazione interattiva con 0,5 ms-impulsi fino a 20 impulsi (10 ms!).
- Para programación individual un pulso de 10 ms por cada dirección a programar; o para programación interactiva con pulsos e 0,5 ms hasta 20 pulsos (10 ms!).

$\overline{CE}$	$\overline{G}$	$\overline{PGM}$	V_{pp}	V_{cc}	D_n	Mode
L	L	H	+ 5V	+ 5V	data out	read
H	X	X	+ 5V	+ 5V	Hi-Z	standby
L	H	⊓ *	+ 12,5V	+ 6V	data in	program
L	L	H	+ 12,5V	+ 6V	data out	program verify
H	X	X	+ 12,5V	+ 6V	Hi-Z	program inhibit

271023 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 27PC010-200 NL	Tix	32-DIP	CMOS	0...+70	<210	<1,5	<200		TTL-TS
TMX 27PC010-20 NL	Tix	32-DIP	CMOS	0...+70	<220	<1,5	<200		TTL-TS
TMX 27PC010-250 NL	Tix	32-DIP	CMOS	0...+70	<210	<1,5	<250		TTL-TS
TMX 27PC010-25 NL	Tix	32-DIP	CMOS	0...+70	<220	<1,5	<250		TTL-TS
TMX 27PC010-300 NL	Tix	32-DIP	CMOS	0...+70	<210	<1,5	<300		TTL-TS
TMX 27PC010-30 NL	Tix	32-DIP	CMOS	0...+70	<220	<1,5	<300		TTL-TS

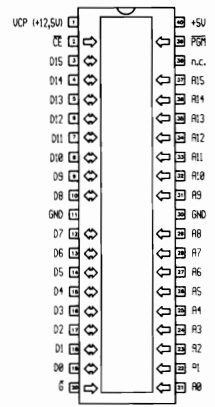


$\overline{CE}$	$\overline{G}$	A9	$\overline{PGM}$	V_{pp}	V_{cc}	D_n	Mode
L	L	X	H	+5V	+5V	data out	read
L	H	X	H	+5V	+5V	Hi-Z	output disable
H	X	X	X	+5V	+5V	Hi-Z	standby
L	H	X	L	+12V	+5V	data in	fast programming
L	L	X	H	+12V	+5V	data out	verify
H	X	X	X	+12V	+5V	Hi-Z	program inhibit
L	L	H	H	+5V	+5V	codes	electronic signature

271023 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 27C301 G-20	Hit	32-DIC	CMOS	0...+70	<165		<200		TTL-TS
HN 27C301 G-25	Hit	32-DIC	CMOS	0...+70	<165		<250		TTL-TS
TC 571001 D-17	Tos	32-DIP	CMOS	0...+70	<157,5	<5,25	<170		TTL-TS
TC 571001 D-20	Tos	32-DIP	CMOS	0...+70	<157,5	<5,25	<200		TTL-TS
TC 571001 D-200	Tos	32-DIP	CMOS	0...+70	<165	<5,5	<200		TTL-TS
TC 571001 D-25	Tos	32-DIP	CMOS	0...+70	<157,5	<5.25	<250		TTL-TS

271024

65536x16-Bit EPROM



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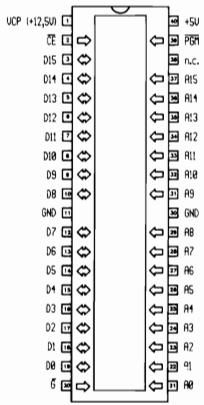
$\overline{CE}$	$\overline{G}$	$\overline{PGM}$	V_{pp}	V_{cc}	D_n	Mode
L	L	H	+ 5V	+ 5V	data out	read
H	X	X	+ 5V	+ 5V	Hi-Z	standby
L	H	⊓ *	+ 12,5V	+ 6V	data in	program
L	L	H	+ 12,5V	+ 6V	data out	program verify
H	X	X	+ 12,5V	+ 6V	Hi-Z	program inhibit

271024 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HN 27C1024 G-15	Hit	40-DIC	CMOS	0...+70			<150		TTL-TS
HN 27C1024 G-20	Hit	40-DIC	CMOS	0...+70			<200		TTL-TS
M 27C1024-12 F1	Sgs	40-DIC	CMOS	0...+70	<275	<5,5	<120		TTL-TS
M 27C1024-12 XF1	Sgs	40-DIC	CMOS	0...+70	<262,5	<5,25	<120		TTL-TS
M 27C1024-15 F1	Sgs	40-DIC	CMOS	0...+70	<275	<5,5	<150		TTL-TS
M 27C1024-15 XF1	Sgs	40-DIC	CMOS	0...+70	<262,5	<5,25	<150		TTL-TS
M 27C1024-15 XF6	Sgs	40-DIC	CMOS	-40...+85	<262,5	<5,25	<150		TTL-TS
M 27C1024-20 F1	Sgs	40-DIC	CMOS	0...+70	<275	<5,5	<200		TTL-TS

271024 Typ · Type · Tipo	Herst. Manuf. Fabr. Prod. Fabr.	Gehäuse Case Boîtier Carcassa Cápsula	Techn. Techn. Techn. Tecn. Tecn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
M 27C1024-20 XF1	Sgs	40-DIC	CMOS	0...+70	<262,5	<5,25	<200		TTL-TS
M 27C1024-20 XF6	Sgs	40-DIC	CMOS	-40...+85	<262,5	<5,25	<200		TTL-TS
M 27C1024-25 F1	Sgs	40-DIC	CMOS	0...+70	<275	<5,5	<250		TTL-TS
M 27C1024-25 XF1	Sgs	40-DIC	CMOS	0...+70	<262,5	<5,25	<250		TTL-TS
M 27C1024-25 XF6	Sgs	40-DIC	CMOS	-40...+85	<262,5	<5,25	<250		TTL-TS
NMC 27C1024 Q120	Nsc	40-DIC	CMOS	0...+70	<275	<0,55	<120		TTL-TS
NMC 27C1024 Q150	Nsc	40-DIC	CMOS	0...+70	<275	<0,55	<150		TTL-TS
NMC 27C1024 Q200	Nsc	40-DIC	CMOS	0...+70	<275	<0,55	<200		TTL-TS
NMC 27C1024 Q90	Nsc	40-DIC	CMOS	0...+70	<275	<0,55	<90		TTL-TS
NMC 27C1024 QE120	Nsc	40-DIC	CMOS	-40...+85	<275	<0,55	<120		TTL-TS
NMC 27C1024 QM150	Nsc	40-DIC	CMOS	-55...+125	<275	<0,55	<150		TTL-TS
SMJ 27C210-25 J	Tix	40-DIC	CMOS	-55...+125	<220	<1,5	<250		TTL-TS
SMJ 27C210-30 J	Tix	40-DIC	CMOS	-55...+125	<220	<1,5	<300		TTL-TS
TC 571024 D-20	Tos	40-DIP	CMOS	-40...+85	<210	<5,25	<200		TTL-TS
TC 571024 D-25	Tos	40-DIP	CMOS	-40...+85	<210	<5,25	<250		TTL-TS
TMS 27C210-170 JL	Tix	40-DIC	CMOS	0...+70	<210	<1,375	<170		TTL-TS
TMS 27C210-200 JL	Tix	40-DIC	CMOS	0...+70	<210	<1,375	<200		TTL-TS
TMS 27C210-20 JL	Tix	40-DIC	CMOS	0...+70	<220	<1,375	<200		TTL-TS
TMS 27C210-250 JL	Tix	40-DIC	CMOS	0...+70	<210	<1,375	<250		TTL-TS
TMS 27C210-25 JL	Tix	40-DIC	CMOS	0...+70	<220	<1,375	<250		TTL-TS
TMS 27C210-300 JL	Tix	40-DIC	CMOS	0...+70	<210	<1,375	<300		TTL-TS
TMS 27C210-30 JL	Tix	40-DIC	CMOS	0...+70	<220	<1,375	<300		TTL-TS
TS 27C1024-12 C	Tho	40-DIC	CMOS	0...+70	<275		<120		TTL-TS
TS 27C1024-12 V	Tho	40-DIC	CMOS	-40...+85	<275		<120		TTL-TS
TS 27C1024-15 C	Tho	40-DIC	CMOS	0...+70	<275		<150		TTL-TS
TS 27C1024-15 V	Tho	40-DIC	CMOS	-40...+85	<275		<150		TTL-TS
TS 27C1024-20 C	Tho	40-DIC	CMOS	0...+70	<275		<200		TTL-TS
TS 27C1024-20 V	Tho	40-DIC	CMOS	-40...+85	<275		<200		TTL-TS
TS 27C1024-25 C	Tho	40-DIC	CMOS	0...+70	<275		<250		TTL-TS
TS 27C1024-25 V	Tho	40-DIC	CMOS	-40...+85	<275		<250		TTL-TS
27C210-15 FA	Phi	40-DIC	CMOS	0...+70	<275	<5,5	<150		TTL-TS
27C210-20 FA	Phi	40-DIC	CMOS	0...+70	<275	<5,5	<200		TTL-TS

271024 — 65536x16-Bit EPROM



* Pro Adresse ein 10ms-Impuls fur Einzel-programmierung oder fur interaktives Programmieren mit 0,5ms-Impulsen bis zu 20 Impulse (10ms!)

* Per address a single 10 ms pulse for single programming or interactive programming with 0.5 ms pulse up to 20 pulses (10 ms!)

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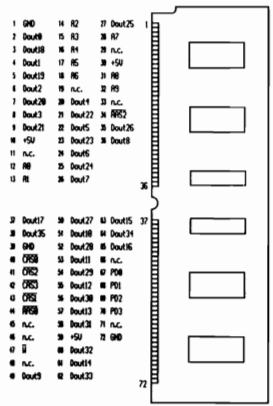
* Per ogni indirizzo un impulso 10 ms per programmazione sinola oppure per programmazione interattiva con 0.5 ms-impulsi fino a 20 impulsi (10 ms!)

* Para programación individual un pulso de 10 ms por cada dirección a programar, o para programación interactiva con pulsos e 0,5 ms hasta 20 pulsos (10 ms!)

$\overline{CE}$	$\overline{G}$	$\overline{PGM}$	V_{pp}	V_{cc}	D_n	Mode
L	L	H	+ 5V	+ 5V	data out	read
H	X	X	+ 5V	+ 5V	Hi-Z	standby
L	H	⌐¬ *	+ 12,5V	+ 6V	data in	program
L	L	H	+ 12,5V	+ 6V	data out	program verify
H	X	X	+ 12,5V	+ 6V	Hi-Z	program inhibit

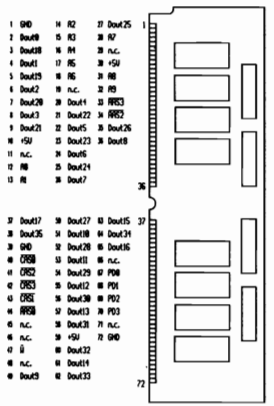
271024 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TMX 27PC210-200 NL	Tix	40-DIP	CMOS	0...+70	<210	<1,5	<200		TTL-TS
TMX 27PC210-20 NL	Tix	40-DIP	CMOS	0...+70	<220	<1,5	<200		TTL-TS
TMX 27PC210-250 NL	Tix	40-DIP	CMOS	0...+70	<210	<1,5	<250		TTL-TS
TMX 27PC210-25 NL	Tix	40-DIP	CMOS	0...+70	<220	<1,5	<250		TTL-TS
TMX 27PC210-300 NL	Tix	40-DIP	CMOS	0...+70	<210	<1,5	<300		TTL-TS
TMX 27PC210-30 NL	Tix	40-DIP	CMOS	0...+70	<220	<1,5	<300		TTL-TS

361020 — 1048576x36-Bit dynamic RAM-Modul



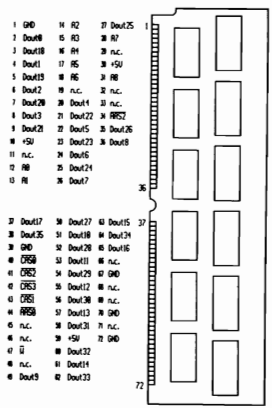
361020 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYM 361020 S-10	Sie	72-SIC	CMOS	0...+70	<5060	<166	<100	<16	TTL-TS
HYM 361020 S-80	Sie	72-SIC	CMOS	0...+70	<5720	<166	<80	<16	TTL-TS

362020 — 2097152x36-Bit dynamic RAM-Modul



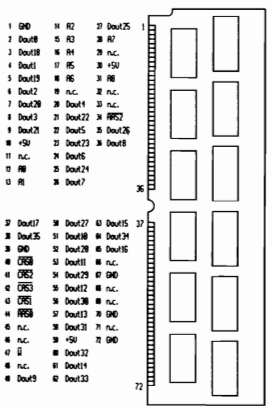
362020 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYM 362020 S-10	Sie	72-SIC	CMOS	0...+70	<5060	<264	<100	<16	TTL-TS
HYM 362020 S-80	Sie	72-SIC	CMOS	0...+70	<5720	<264	<80	<16	TTL-TS

362500 — 262144x36-Bit dynamic RAM-Modul



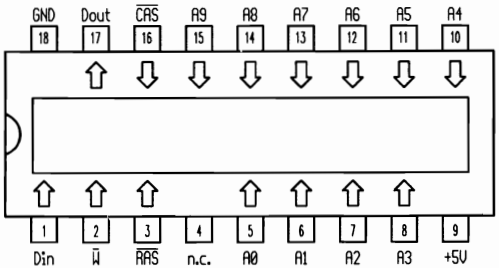
362500 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYM 362500 S-80	Sie	72-SIC	CMOS	0...+70	<4400	<99	<80	<8	TTL-TS

365120 — 524288x36-Bit dynamic RAM-Modul



365120 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYM 365120 S-80	Sie	72-SIC	CMOS	0...+70	<4400	<330	<80	<8	TTL-TS

411000 — 1048576x1-Bit dynamic RAM

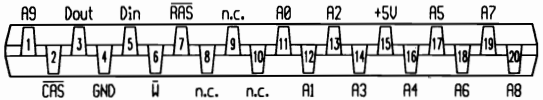


411000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 511000-10	Hit	18-DIC	CMOS	0...+70	<330	<27,5	<100	<8	TTL-TS
HM 511000-12	Hit	18-DIC	CMOS	0...+70	<300	<27,5	<120	<8	TTL-TS
HM 511000-15	Hit	18-DIC	CMOS	0...+70	<220	<27,5	<150	<8	TTL-TS
HM 511000 P-10	Hit	18-DIP	CMOS	0...+70	<330	<27,5	<100	<8	TTL-TS
HM 511000 P-12	Hit	18-DIP	CMOS	0...+70	<275	<27,5	<120	<8	TTL-TS
HM 511000 P-15	Hit	18-DIP	CMOS	0...+70	<220	<27,5	<150	<8	TTL-TS
M5M 41000 AP-10	Mit	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 AP-12	Mit	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS

411000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41000 AP-8	Mit	18-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41000 BP-10	Mit	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 BP-10L	Mit	18-DIP	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 41000 BP-7	Mit	18-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41000 BP-7L	Mit	18-DIP	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 41000 BP-8	Mit	18-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41000 BP-8L	Mit	18-DIP	CMOS	0...+70	<385	<11	<80	<64	TTL-TS
MN 411000-10	Mat	18-DIP	NMOS	0...+70	<522,5	<24,75	<100	<8	TTL-TS
MN 411000-12	Mat	18-DIP	NMOS	0...+70	<467,5	<24,75	<120	<8	TTL-TS
MN 41C1000-08	Mat	18-DIP	CMOS	0...+70	<385	<2,75	<80	<8	TTL-TS
MN 41C1000-10	Mat	18-DIP	CMOS	0...+70	<330	<2,75	<100	<8	TTL-TS
TC 511000 P-10	Tos	18-DIP	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511000 P-12	Tos	18-DIP	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS
TC 511000 P-85	Tos	18-DIP	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS
TC 511000 PL-10	Tos	18-DIP	CMOS	0...+70	<330	<1,7	<100	<8	TTL-TS
TC 511000 PL-12	Tos	18-DIP	CMOS	0...+70	<275	<1,7	<120	<8	TTL-TS
TC 511000 PL-85	Tos	18-DIP	CMOS	0...+70	<385	<1,7	<85	<8	TTL-TS
µPD 411000 C-12	Nec	18-DIP	NMOS	0...+70	<550	28	<120	<8	TTL-TS
µPD 411000 C-15	Nec	18-DIP	NMOS	0...+70	<495	28	<150	<8	TTL-TS
µPD 421000 C-10	Nec	18-DIP	CMOS	0...+70	<330	16.5	<100	<8	TTL-TS
µPD 421000 C-12	Nec	18-DIP	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 421000 C-8	Nec	18-DIP	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

411000

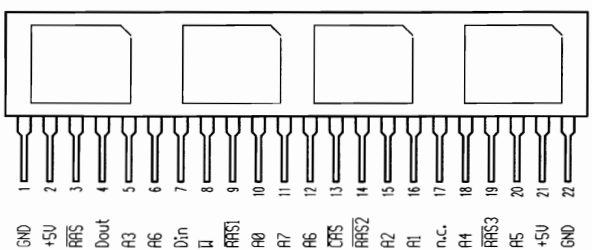
1048576x1-Bit dynamic RAM (page mode)



411000 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41000 AL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 AL-12	Mit	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 41000 AL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41000 BL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 BL-10L	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 41000 BL-7	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41000 BL-7L	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 41000 BL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS

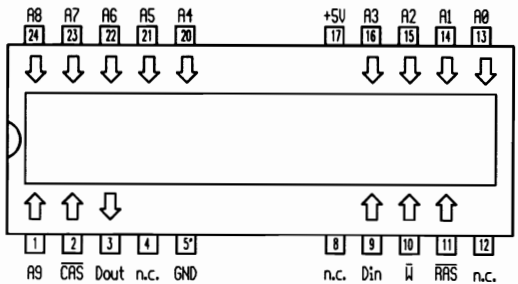
411000 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41000 BL-8L	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<64	TTL-TS
MN 41C1000 L-08	Mat	20-ZIP	CMOS	0...+70	<385	<2,75	<80	<8	TTL-TS
MN 41C1000 L-10	Mat	20-ZIP	CMOS	0...+70	<358	<2,75	<100	<8	TTL-TS
MN 411000 L-10	Mat	20-ZIP	NMOS	0...+70	<522,5	<24,75	<100	<8	TTL-TS
MN 411000 L-12	Mat	20-ZIP	NMOS	0...+70	<467,5	<24,75	<120	<8	TTL-TS
TC 511000 Z-10	Tos	20-ZIP	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511000 Z-12	Tos	20-ZIP	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS
TC 511000 Z-85	Tos	20-ZIP	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS
TC 511000 ZL-10	Tos	20-ZIP	CMOS	0...+70	<330	<1,7	<100	<8	TTL-TS
TC 511000 ZL-12	Tos	20-ZIP	CMOS	0...+70	<275	<1,7	<120	<8	TTL-TS
TC 511000 ZL-85	Tos	20-ZIP	CMOS	0...+70	<385	<1,7	<85	<8	TTL-TS

411000 — 1048576x1-Bit dynamic RAM-Modul



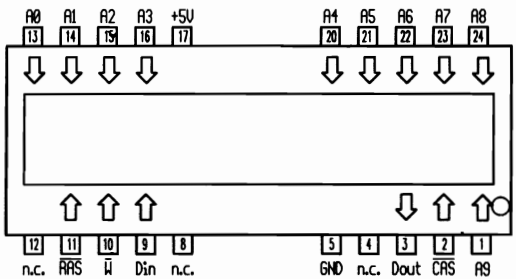
411000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MC 411000 A1 A-12	Nec	22-SIP	NMOS	0...+70	<539	110	<120	4	TTL-TS
MC 411000 A1 A-15	Nec	22-SIP	NMOS	0...+70	<467.5	110	<150	4	TTL-TS

411000 — 1048576x1-Bit dynam. RAM (page mode)



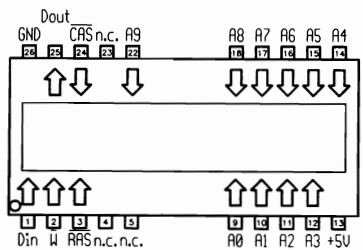
411000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41000 BVP-10	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 BVP-10L	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 41000 BVP-7	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41000 BVP-7L	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 41000 BVP-8	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41000 BVP-8L	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<64	TTL-TS

411000 — 1048576x1-Bit dynam. RAM (page mode)



411000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41000 BRV-10	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 BRV-10L	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 41000 BRV-7	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41000 BRV-7L	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 41000 BRV-8	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41000 BRV-8L	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<64	TTL-TS

411000 — 1048576x1-Bit dynam. RAM (page mode)

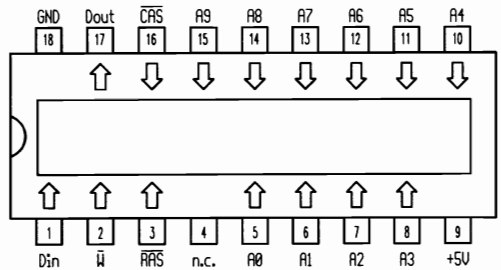


411000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41000 AJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 AJ-12	Mit	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 41000 AJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41000 BJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41000 BJ-10L	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 41000 BJ-7	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41000 BJ-7L	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 41000 BJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS

411000 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41000 BJ-8L	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<64	TTL-TS
MN 41C1000 SJ-08	Mat	26-FLAT	CMOS	0...+70	<385	<2,75	<80	<8	TTL-TS
MN 41C1000 SJ-10	Mat	26-FLAT	CMOS	0...+70	<330	<2,75	<100	<8	TTL-TS
MN 411000 SJ-10	Mat	26-FLAT	NMOS	0...+70	<522,5	<24,75	<100	<8	TTL-TS
MN 411000 SJ-12	Mat	26-FLAT	NMOS	0...+70	<467,5	<24,75	<120	<8	TTL-TS
TC 511000 J-10	Tos	26-FLAT	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511000 J-12	Tos	26-FLAT	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS
TC 511000 J-85	Tos	26-FLAT	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS
TC 511000 JL-10	Tos	26-FLAT	CMOS	0...+70	<330	<1,7	<100	<8	TTL-TS
TC 511000 JL-12	Tos	26-FLAT	CMOS	0...+70	<385	<1,7	<120	<8	TTL-TS
TC 511000 JL-85	Tos	26-FLAT	CMOS	0...+70	<385	<1,7	<85	<8	TTL-TS
µPD 411000 LA-12	Nec	26-FLAT	NMOS	0...+70	<550	28	<120	<8	TTL-TS
µPD 411000 LA-15	Nec	26-FLAT	NMOS	0...+70	<495	28	<150	<8	TTL-TS
µPD 421000 LA-10	Nec	26-FLAT	CMOS	0...+70	<330	16.5	<100	<8	TTL-TS
µPD 421000 LA-12	Nec	26-FLAT	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 421000 LA-8	Nec	26-FLAT	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

411001

1048576x1-Bit dynam. RAM (nibble mode)

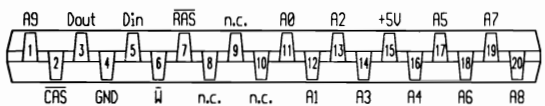


411001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 511001-10	Hit	18-DIC	CMOS	0...+70	<330	<27,5	<100	<8	TTL-TS
HM 511001-12	Hit	18-DIC	CMOS	0...+70	<275	<27,5	<120	<8	TTL-TS
HM 511001-15	Hit	18-DIC	CMOS	0...+70	<220	<27,5	<150	<8	TTL-TS
HM 511001 P-10	Hit	18-DIP	CMOS	0...+70	<330	<27,5	<100	<8	TTL-TS
HM 511001 P-12	Hit	18-DIP	CMOS	0...+70	<275	<27,5	<120	<8	TTL-TS
HM 511001 P-15	Hit	18-DIP	CMOS	0...+70	<220	<27,5	<150	<8	TTL-TS
M5M 41001 AP-10	Mit	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41001 AP-12	Mit	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS

411001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
M5M 41001 AP-8	Mit	18-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41001 BP-10	Mit	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41001 BP-7	Mit	18-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41001 BP-8	Mit	18-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
TC 511001 P-10	Tos	18-DIP	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511001 P-12	Tos	18-DIP	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS
TC 511001 P-85	Tos	18-DIP	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS
µPD 411001 C-12	Nec	18-DIP	NMOS	0...+70	<550	28	<120	<8	TTL-TS
µPD 411001 C-15	Nec	18-DIP	NMOS	0...+70	<495	28	<150	<8	TTL-TS
µPD 421001 C-10	Nec	18-DIP	CMOS	0...+70	<330	16.5	<100	<8	TTL-TS
µPD 421001 C-12	Nec	18-DIP	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 421001 C-8	Nec	18-DIP	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

411001

1048576x1-Bit dynam. RAM (nibble mode)

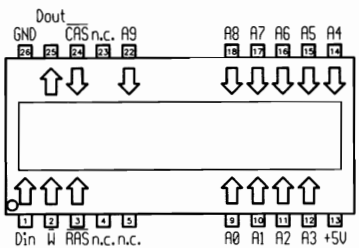


411001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
M5M 41001 AL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41001 AL-12	Mit	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 41001 AL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41001 BL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41001 BL-7	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41001 BL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
TC 511001 Z-10	Tos	20-ZIP	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511001 Z-12	Tos	20-ZIP	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS

411001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 511001 Z-85	Tos	20-ZIP	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS

411001

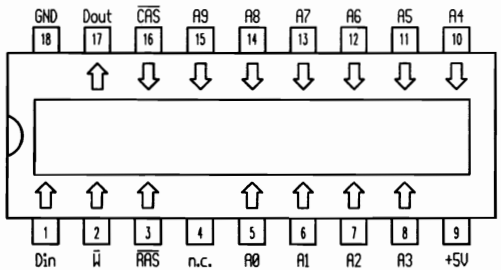
1048576x1-Bit dynam. RAM (nibble mode)



411001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41001 AJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41001 AJ-12	Mit	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 41001 AJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41001 BJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41001 BJ-7	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41001 BJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
TC 511001 J-10	Tos	26-FLAT	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511001 J-12	Tos	26-FLAT	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS

411001 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 511001 J-85	Tos	26-FLAT	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS
µPD 411001 LA-12	Nec	26-FLAT	NMOS	0...+70	<550	28	<120	<8	TTL-TS
µPD 411001 LA-15	Nec	26-FLAT	NMOS	0...+70	<495	28	<150	<8	TTL-TS
µPD 421001 LA-10	Nec	26-FLAT	CMOS	0...+70	<330	16.5	<100	<8	TTL-TS
µPD 421001 LA-12	Nec	26-FLAT	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 421001 LA-8	Nec	26-FLAT	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

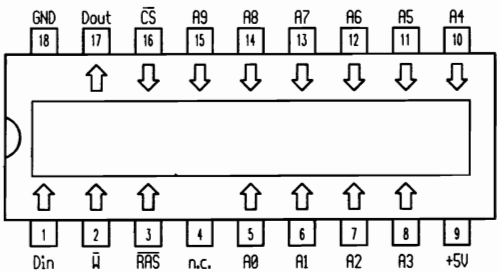
411002 — 1048576x1-Bit dynam. RAM (static column)



411002 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 421002 C-10	Nec	18-DIP	CMOS	0...+70	<330	16.5	<100	<8	TTL-TS
µPD 421002 C-12	Nec	18-DIP	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 421002 C-8	Nec	18-DIP	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

411002

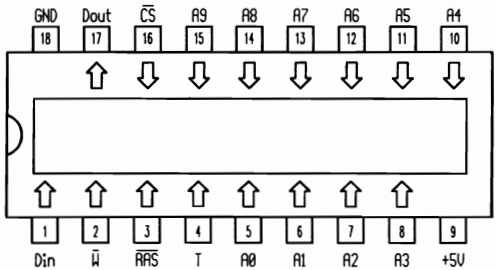
1048576x1-Bit dynam. RAM (static column)



411002 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HM 511002-10	Hit	18-DIC	CMOS	0...+70	<330	<27,5	<100	<8	TTL-TS
HM 511002-12	Hit	18-DIC	CMOS	0...+70	<275	<27,5	<120	<8	TTL-TS
HM 511002-15	Hit	18-DIC	CMOS	0...+70	<220	<27,5	<150	<8	TTL-TS
HM 511002 P-10	Hit	18-DIP	CMOS	0...+70	<330	<27,5	<100	<8	TTL-TS
HM 511002 P-12	Hit	18-DIP	CMOS	0...+70	<275	<27,5	<120	<8	TTL-TS
HM 511002 P-15	Hit	18-DIP	CMOS	0...+70	<220	<27,5	<150	<8	TTL-TS
M5M 41002 AP-10	Mit	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41002 AP-12	Mit	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS

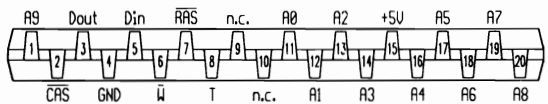
411002 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41002 AP-8	Mit	18-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41002 BP-10	Mit	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41002 BP-7	Mit	18-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41002 BP-8	Mit	18-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MN 41C1002-08	Mat	18-DIP	CMOS	0...+70	<385	<2,75	<80	<8	TTL-TS
MN 41C1002-10	Mat	18-DIP	CMOS	0...+70	<330	<2,75	<100	<8	TTL-TS

411002 — 1048576x1-Bit dynam. RAM (static column)



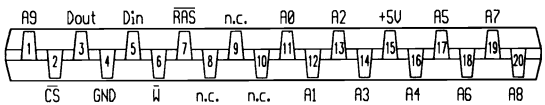
411002 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41C1002 P-10	Sam	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1002 P-12	Sam	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511002 P-10	Mot	18-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
MCM 511002 P-12	Mot	18-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511002 P-85	Mot	18-DIP	CMOS	0...+70	<385	<11	<85	<8	TTL-TS
TC 511002 P-10	Tos	18-DIP	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511002 P-12	Tos	18-DIP	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS
TC 511002 P-85	Tos	18-DIP	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS

411002 — 1048576x1-Bit dynam. RAM (static column)



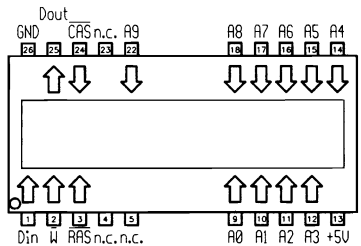
411002 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41C1002 Z-10	Sam	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1002 Z-12	Sam	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
TC 511002 Z-10	Tos	20-ZIP	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511002 Z-12	Tos	20-ZIP	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS
TC 511002 Z-85	Tos	20-ZIP	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS

411002 — 1048576x1-Bit dynam. RAM (static column)



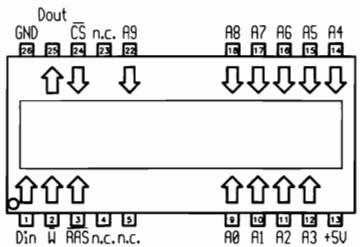
411002 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41002 AL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41002 AL-12	Mit	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 41002 AL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41002 BL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41002 BL-7	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41002 BL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MN 41C1002 L-08	Mat	20-ZIP	CMOS	0...+70	<385	<2,75	<80	<8	TTL-TS
MN 41C1002 L-10	Mat	20-ZIP	CMOS	0...+70	<330	<2,75	<100	<8	TTL-TS

411002 — 1048576x1-Bit dynam. RAM (static column)



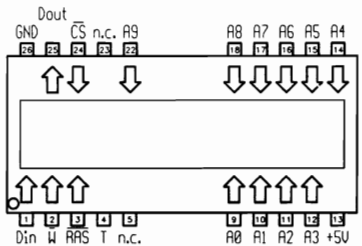
411002 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
µPD 421002 LA-10	Nec	26-FLAT	CMOS	0...+70	<330	16.5	<100	<8	TTL-TS
µPD 421002 LA-12	Nec	26-FLAT	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 421002 LA-8	Nec	26-FLAT	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

411002 — 1048576x1-Bit dynam. RAM (static column)



411002 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 41002 AJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41002 AJ-12	Mit	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 41002 AJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 41002 BJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 41002 BJ-7	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 41002 BJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MN 41C1002 SJ-08	Mat	26-FLAT	CMOS	0...+70	<385	<2,75	<80	<8	TTL-TS
MN 41C1002 SJ-10	Mat	26-FLAT	CMOS	0...+70	<330	<2,75	<100	<8	TTL-TS

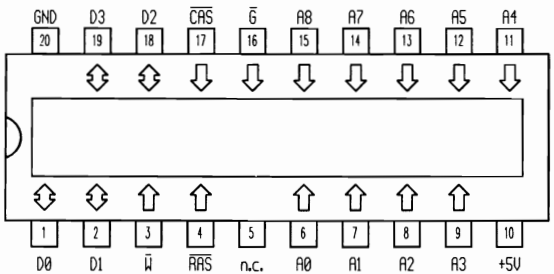
411002 — 1048576x1-Bit dynam. RAM (static column)



411002 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 41C1002 J-10	Sam	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
KM 41C1002 J-12	Sam	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511002 J-10	Mot	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
MCM 511002 J-12	Mot	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
MCM 511002 J-85	Mot	26-FLAT	CMOS	0...+70	<385	<11	<85	<8	TTL-TS
TC 511002 J-10	Tos	26-FLAT	CMOS	0...+70	<330	<5,5	<100	<8	TTL-TS
TC 511002 J-12	Tos	26-FLAT	CMOS	0...+70	<275	<5,5	<120	<8	TTL-TS
TC 511002 J-85	Tos	26-FLAT	CMOS	0...+70	<385	<5,5	<85	<8	TTL-TS

424256

262144x4-Bit dynam. RAM (page mode)

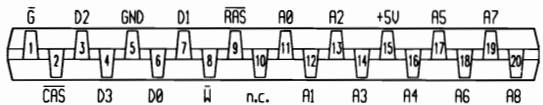


424256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 514256-10	Sie	20-DIP	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
HYB 514256-12	Sie	20-DIP	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
HYB 514256-85	Sie	20-DIP	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS
HYB 514256 B-60	Sie	20-DIP	CMOS	0...+70	<495	<11	<60	<8	TTL-TS
HYB 514256 B-70	Sie	20-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
HYB 514256 B-80	Sie	20-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
HYB 514256 BL-60	Sie	20-DIP	CMOS	0...+70	<495	<5,5	<60	<64	TTL-TS
HYB 514256 BL-70	Sie	20-DIP	CMOS	0...+70	<440	<5,5	<70	<64	TTL-TS

424256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 44C256 P-10	Sam	20-DIP	CMOS	0...+70			<100	<8	TTL-TS
KM 44C256 P-12	Sam	20-DIP	CMOS	0...+70			<120	<8	TTL-TS
M5M 44256 AP-10	Mit	20-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44256 AP-12	Mit	20-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 44256 AP-8	Mit	20-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BP-10	Mit	20-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44256 BP-10L	Mit	20-DIP	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 44256 BP-7	Mit	20-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44256 BP-7L	Mit	20-DIP	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 44256 BP-8	Mit	20-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BP-8L	Mit	20-DIP	CMOS	0...+70	<385	<11	<80	<64	TTL-TS
M5M 44266 BP-10	Mit	20-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44266 BP-7	Mit	20-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44266 BP-8	Mit	20-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MCM 514256 P-10	Mot	20-DIP	CMOS	0...+70	<358	<11	<100	<8	TTL-TS
MCM 514256 P-12	Mot	20-DIP	CMOS	0...+70	<303	<11	<120	<8	TTL-TS
MCM 514256 P-85	Mot	20-DIP	CMOS	0...+70	<413	<11	<85	<8	TTL-TS
MN 414256-10	Mat	20-DIP	NMOS	0...+70	<522,5	<24,75	<100	<8	TTL-TS
MN 414256-12	Mat	20-DIP	NMOS	0...+70	<467,5	<24,75	<120	<8	TTL-TS
MN 41C4256-08	Mat	20-DIP	CMOS	0...+70	<413	<2,75	<80	<8	TTL-TS
MN 41C4256-10	Mat	20-DIP	CMOS	0...+70	<358	<2,75	<100	<8	TTL-TS
MN 42C4256 SJ-08	Mat	20-FLAT	CMOS	0...+70	<413	<2,75	<80	<64	TTL-TS
MN 42C4256 SJ-10	Mat	20-FLAT	CMOS	0...+70	<358	<2,75	<100	<64	TTL-TS
TC 514256 P-10	Tos	20-DIP	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
TC 514256 P-12	Tos	20-DIP	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
TC 514256 P-85	Tos	20-DIP	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS
TC 514256 PL-10	Tos	20-DIP	CMOS	0...+70	<358	<1,7	<100	<8	TTL-TS
TC 514256 PL-12	Tos	20-DIP	CMOS	0...+70	<303	<1,7	<120	<8	TTL-TS
TC 514256 PL-85	Tos	20-DIP	CMOS	0...+70	<413	<1,7	<85	<8	TTL-TS
µPD 424256 C-10	Nec	20-DIP	CMOS	0...+70	<330	16,5	<100	<8	TTL-TS
µPD 424256 C-12	Nec	20-DIP	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 424256 C-8	Nec	20-DIP	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

424256

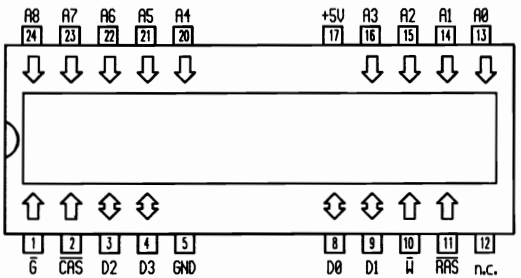
262144x4-Bit dynam. RAM (page mode)



424256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 514256 BZ-60	Sie	20-ZIP	CMOS	0...+70	<495	<11	<60	<8	TTL-TS
HYB 514256 BZ-70	Sie	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
HYB 514256 BZ-80	Sie	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
HYB 514256 BZL-60	Sie	20-ZIP	CMOS	0...+70	<495	<5,5	<60	<64	TTL-TS
HYB 514256 BZL-70	Sie	20-ZIP	CMOS	0...+70	<440	<5,5	<70	<64	TTL-TS
KM 44C256 Z-10	Sam	20-ZIP	CMOS	0...+70			<100	<8	TTL-TS
KM 44C256 Z-12	Sam	20-ZIP	CMOS	0...+70			<120	<8	TTL-TS
M5M 44256 AL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS

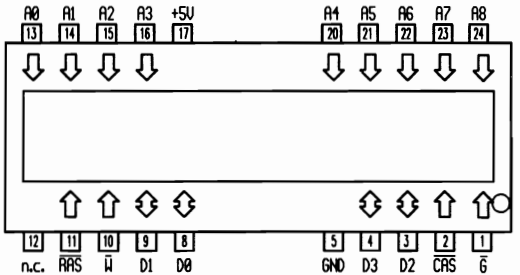
424256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44256 AL-12	Mit	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 44256 AL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44256 BL-10L	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 44256 BL-7	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44256 BL-7L	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 44256 BL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BL-8L	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<64	TTL-TS
M5M 44266 BL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44266 BL-7	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44266 BL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MN 41C4256 L-08	Mat	20-ZIP	CMOS	0...+70	<413	<2,75	<80	<8	TTL-TS
MN 41C4256 L-10	Mat	20-ZIP	CMOS	0...+70	<358	<2,75	<100	<8	TTL-TS
MN 414256 L-10	Mat	20-ZIP	NMOS	0...+70	<522,5	<24,75	<100	<8	TTL-TS
MN 414256 L-12	Mat	20-ZIP	NMOS	0...+70	<467,5	<24,75	<120	<8	TTL-TS
TC 514256 Z-10	Tos	20-ZIP	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
TC 514256 Z-12	Tos	20-ZIP	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
TC 514256 Z-85	Tos	20-ZIP	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS
TC 514256 ZL-10	Tos	20-ZIP	CMOS	0...+70	<358	<1,7	<100	<8	TTL-TS
TC 514256 ZL-12	Tos	20-ZIP	CMOS	0...+70	<303	<1,7	<120	<8	TTL-TS
TC 514256 ZL-85	Tos	20-ZIP	CMOS	0...+70	<413	<1,7	<85	<8	TTL-TS

424256 — 262144x4-Bit dynam. RAM (page mode)



424256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44256 BVP-10	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44256 BVP-10L	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 44256 BVP-7	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44256 BVP-7L	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 44256 BVP-8	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BVP-8L	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<64	TTL-TS

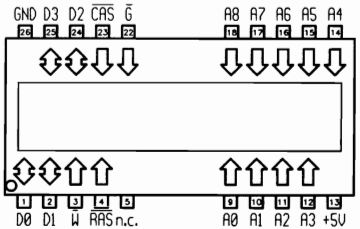
424256 — 262144x4-Bit dynam. RAM (page mode)



424256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44256 BRV-10	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44256 BRV-10L	Mit	24-FLAT	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 44256 BRV-7	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44256 BRV-7L	Mit	24-FLAT	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 44256 BRV-8	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BRV-8L	Mit	24-FLAT	CMOS	0...+70	<385	<11	<80	<64	TTL-TS

424256

262144x4-Bit dynamic RAM



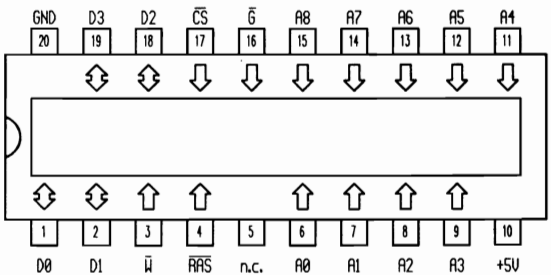
424256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
HYB 514256 BJ-60	Sie	26-FLAT	CMOS	0...+70	<495	<11	<60	<8	TTL-TS
HYB 514256 BJ-70	Sie	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
HYB 514256 BJ-80	Sie	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
HYB 514256 BJL-60	Sie	26-FLAT	CMOS	0...+70	<495	<5,5	<60	<64	TTL-TS
HYB 514256 BJL-70	Sie	26-FLAT	CMOS	0...+70	<440	<5,5	<70	<64	TTL-TS
HYB 514256 J-10	Sie	26-FLAT	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
HYB 514256 J-12	Sie	26-FLAT	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
HYB 514256 J-85	Sie	26-FLAT	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS

424256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Ausgang Output Sortie Uscita Salida
					$mW/bit				
KM 44C256 J-10	Sam	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
KM 44C256 J-12	Sam	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
M5M 44256 AJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44256 AJ-12	Mit	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 44256 AJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44256 BJ-10L	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<64	TTL-TS
M5M 44256 BJ-7	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44256 BJ-7L	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<64	TTL-TS
M5M 44256 BJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44256 BJ-8L	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<64	TTL-TS
M5M 44266 BJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44266 BJ-7	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44266 BJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MCM 514256 J-10	Mot	26-FLAT	CMOS	0...+70	<358	<11	<100	<8	TTL-TS
MCM 514256 J-12	Mot	26-FLAT	CMOS	0...+70	<303	<11	<120	<8	TTL-TS
MCM 514256 J-85	Mot	26-FLAT	CMOS	0...+70	<413	<11	<85	<8	TTL-TS
MN 41C4256 SJ-08	Mat	26-FLAT	CMOS	0...+70	<413	<2,75	<80	<8	TTL-TS
MN 41C4256 SJ-10	Mat	26-FLAT	CMOS	0...+70	<358	<2,75	<100	<8	TTL-TS
MN 414256 SJ-10	Mat	26-FLAT	NMOS	0...+70	<522,5	<24,75	<100	<8	TTL-TS
MN 414256 SJ-12	Mat	26-FLAT	NMOS	0...+70	<467,5	<24,75	<120	<8	TTL-TS
TC 514256 J-10	Tos	26-FLAT	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
TC 514256 J-12	Tos	26-FLAT	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
TC 514256 J-85	Tos	26-FLAT	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS
TC 514256 JL-10	Tos	26-FLAT	CMOS	0...+70	<358	<1,7	<100	<8	TTL-TS
TC 514256 JL-12	Tos	26-FLAT	CMOS	0...+70	<303	<1,7	<120	<8	TTL-TS
TC 514256 JL-85	Tos	26-FLAT	CMOS	0...+70	<413	<1,7	<85	<8	TTL-TS
µPD 424256 LA-10	Nec	26-FLAT	CMOS	0...+70	<330	16.5	<100	<8	TTL-TS
µPD 424256 LA-12	Nec	26-FLAT	CMOS	0...+70	<275	16.5	<120	<8	TTL-TS
µPD 424256 LA-8	Nec	26-FLAT	CMOS	0...+70	<385	16.5	<80	<8	TTL-TS

424258

2

262144x4-Bit dynam. RAM (static column)

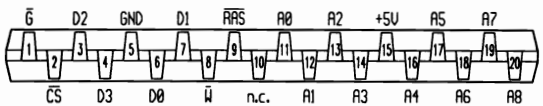


424258 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
KM 44C258 P-10	Sam	20-DIP	CMOS	0...+70			<100	<8	TTL-TS
KM 44C258 P-12	Sam	20-DIP	CMOS	0...+70			<120	<8	TTL-TS
M5M 44258 AP-10	Mit	20-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44258 AP-12	Mit	20-DIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 44258 AP-8	Mit	20-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44258 BP-10	Mit	20-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44258 BP-7	Mit	20-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44258 BP-8	Mit	20-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS

424258 Type	Man	Case	Techn.	TU°C	Ptyp mW	P standby mW	taa ns	tref ms	Output
					$mW/bit				
M5M 44268 BP-10	Mit	20-DIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44268 BP-7	Mit	20-DIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44268 BP-8	Mit	20-DIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MCM 514258 P-10	Mot	20-DIP	CMOS	0...+70	<358	<11	<100	<8	TTL-TS
MCM 514258 P-12	Mot	20-DIP	CMOS	0...+70	<303	<11	<120	<8	TTL-TS
MCM 514258 P-85	Mot	20-DIP	CMOS	0...+70	<413	<11	<85	<8	TTL-TS
MN 41C4258-08	Mat	20-DIP	CMOS	0...+70	<413	<2,75	<80	<8	TTL-TS
MN 41C4258-10	Mat	20-DIP	CMOS	0...+70	<358	<2,75	<100	<8	TTL-TS
MN 41C4258 SJ-08	Mat	20-FLAT	CMOS	0...+70	<413	<2,75	<80	<8	TTL-TS
MN 41C4258 SJ-10	Mat	20-FLAT	CMOS	0...+70	<358	<2,75	<100	<8	TTL-TS
TC 514258 P-10	Tos	20-DIP	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
TC 514258 P-12	Tos	20-DIP	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
TC 514258 P-85	Tos	20-DIP	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS

424258

262144x4-Bit dynam. RAM (static column)

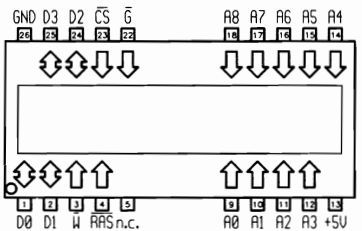


424258 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 44C258 Z-10	Sam	20-ZIP	CMOS	0...+70			<100	<8	TTL-TS
KM 44C258 Z-12	Sam	20-ZIP	CMOS	0...+70			<120	<8	TTL-TS
M5M 44258 AL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44258 AL-12	Mit	20-ZIP	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 44258 AL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44258 BL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44258 BL-7	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44258 BL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS

424258 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44268 BL-10	Mit	20-ZIP	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44268 BL-7	Mit	20-ZIP	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44268 BL-8	Mit	20-ZIP	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MN 41C4258 L-08	Mat	20-ZIP	CMOS	0...+70	<413	<2,75	<80	<8	TTL-TS
MN 41C4258 L-10	Mat	20-ZIP	CMOS	0...+70	<358	<2,75	<100	<8	TTL-TS
TC 514258 Z-10	Tos	20-ZIP	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
TC 514258 Z-12	Tos	20-ZIP	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
TC 514258 Z-85	Tos	20-ZIP	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS

424258

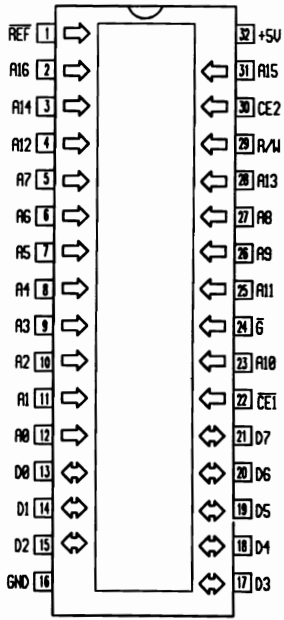
262144x4-Bit dynam. RAM (static column)



424258 Type	Herst. Manuf. Fabr. Prod. Fabr.	Gehäuse Case Boîtier Carcassa Cápsula	Techn. Techn. Techn. Tecn. Tecn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
KM 44C258 J-10	Sam	26-FLAT	CMOS	0...+70			<100	<8	TTL-TS
KM 44C258 J-12	Sam	26-FLAT	CMOS	0...+70			<120	<8	TTL-TS
M5M 44258 AJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44258 AJ-12	Mit	26-FLAT	CMOS	0...+70	<275	<11	<120	<8	TTL-TS
M5M 44258 AJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
M5M 44258 BJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44258 BJ-7	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44258 BJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS

424258 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
M5M 44268 BJ-10	Mit	26-FLAT	CMOS	0...+70	<330	<11	<100	<8	TTL-TS
M5M 44268 BJ-7	Mit	26-FLAT	CMOS	0...+70	<440	<11	<70	<8	TTL-TS
M5M 44268 BJ-8	Mit	26-FLAT	CMOS	0...+70	<385	<11	<80	<8	TTL-TS
MCM 514258 J-10	Mot	26-FLAT	CMOS	0...+70	<358	<11	<100	<8	TTL-TS
MCM 514258 J-12	Mot	26-FLAT	CMOS	0...+70	<303	<11	<120	<8	TTL-TS
MCM 514258 J-85	Mot	26-FLAT	CMOS	0...+70	<413	<11	<85	<8	TTL-TS
TC 514258 J-10	Tos	26-FLAT	CMOS	0...+70	<358	<5,5	<100	<8	TTL-TS
TC 514258 J-12	Tos	26-FLAT	CMOS	0...+70	<303	<5,5	<120	<8	TTL-TS
TC 514258 J-85	Tos	26-FLAT	CMOS	0...+70	<413	<5,5	<85	<8	TTL-TS
µPD 424258 C-10	Nec	26-FLAT	CMOS	0...+70	<330		<100	<8	TTL-TS
µPD 424258 C-12	Nec	26-FLAT	CMOS	0...+70	<275		<120	<8	TTL-TS
µPD 424258 C-8	Nec	26-FLAT	CMOS	0...+70	<385		<80	<8	TTL-TS
µPD 424258 LA-10	Nec	26-FLAT	CMOS	0...+70	<330		<100	<8	TTL-TS
µPD 424258 LA-12	Nec	26-FLAT	CMOS	0...+70	<275		<120	<8	TTL-TS
µPD 424258 LA-8	Nec	26-FLAT	CMOS	0...+70	<385		<80	<8	TTL-TS

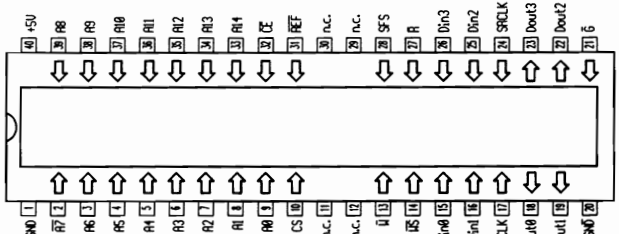
518128 — 131072x8-Bit pseudo-static RAM



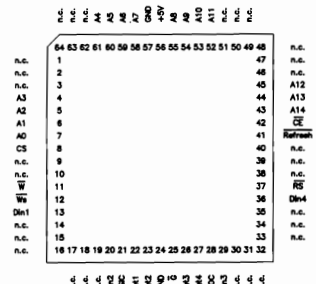
* Bei fallender Flanke (CE2= H) oder steigender Flanke (CE1= L) sind alle Adreß-eingänge «in», sonst sind sie «X».
* At CE1 falling edge (CE2= H) or CE2 rising edge (CE1= L) all address inputs are "in" and at other condition the address input are "X".
* Pour un flanc descendant (CE2= H) ou ascendant (CE1= L), toutes les entrées d'adresses sont "in", autrement, elles sont "X".
* A fianco in riduzione (CE2= H) o fianco in aumento (CE1= L) tutti gli ingressi di indirizzo sono "in", altrimenti sono "X".
* Para flancos de caída (CE2= H) o flancos de subida (CE1= L) todas las entradas de dirección son "in"; en todos los demás casos, son "X".

518128 Type	Man	Case	Techn.	T_{tj}/C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 518128 P-10	Tos	32-DIP	CMOS	0...+70	<330	<5,5	<100	<16	TTL-TS
TC 518128 P-12	Tos	32-DIP	CMOS	0...+70	<275	<5,5	<120	<16	TTL-TS
TC 518128 PL-10	Tos	32-DIP	CMOS	0...+70	<330	<0,55	<100	<16	TTL-TS
TC 518128 PL-12	Tos	32-DIP	CMOS	0...+70	<275	<0,55	<120	<16	TTL-TS

521000 — 262144x4-Bit dynamic Video-RAM



521000 — 262144x4-Bit dynamic Video-RAM

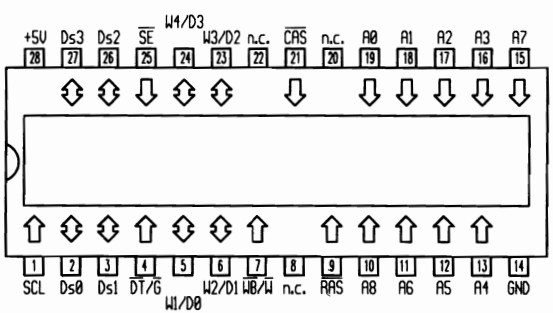


521000 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 4700	Mat	40-DIP	NMOS	0...+70	<825	<110	<200	<2	TTL
MN 4700 K	Mat	40-TDIP	NMOS	0...+70	<825	<110	<200	<2	TTL
TC 521000 P	Tos	40-DIP	CMOS	0...+70	<550	<110	<190	<8	TTL

521000 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
MN 4700 F	Mat	64-PLCC	NMOS	0...+70	<825	<110	<200	<2	TTL

524256 — 262144x4-Bit Multiport Video RAM

Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 524256 P-10	Tos	28-DIP	CMOS	0...+70	<60	<3	<100	<8	TTL
TC 524256 P-12	Tos	28-DIP	CMOS	0...+70	<55	<3	<120	<8	TTL

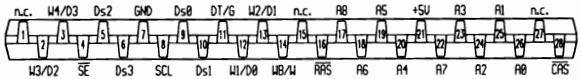


* **Der Level von DT/G in CAS ist vor dem RAS nicht definiert. Es wird aber empfohlen, daß das DT/G den H-Level hat, da dieser Eingan für zukünftige Erweiterungen verwendet wird.**
* **The input level of DT/G in the CAS before RAS timing is not restricted. However it is recommended that DT/G be held H because this input will be used for future expansion of the operation mode.**
* **Le niveau de DT/G dans CAS n'est pas défini avant le RAS. Il est cependant recommandé que le DT/G ait le niveau haut H, étant donné que cette entrée est utilisée pour des élargissements ultérieurs.**
* **Il livello di DT/G in CAS non è definito precedentemente a RAS. Si raccomanda comunque che T/G abbia il livello H, dato che questo ingresso viene utilizzato per futuri ampliamenti.**
* **El nivel de entrada de DT/G en el CAS antes des RAS no está definido. Sin embargo, se recomienda que DT/G se mantenga en nivel H, pues esta entrada está prevista para futuras ampliaciones de los tipos de operación.**

524256

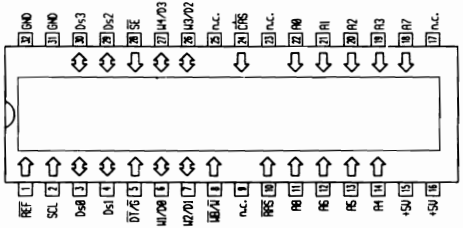
262144x4-Bit Multiport Video RAM

524256 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 524256 Z-10	Tos	28-ZIP	CMOS	0...+70	<60	<3	<100	<8	TTL
TC 524256 Z-12	Tos	28-ZIP	CMOS	0...+70	<55	<3	<120	<8	TTL



* Der Level von DT/G in CAS ist vor dem RAS nicht definiert. Es wird aber empfohlen, daß das DT/G den H-Level hat, da dieser Eingan für zukünftige Erweiterungen verwendet wird.
* The input level of DT/G in the CAS before RAS timing is not restricted. However it is recommended that DT/G be held H because this input will be used for future expansion of the operation mode.
* Le niveau de DT/G dans CAS n'est pas défini avant le RAS. Il est cependant recommandé que le DT/G ait le niveau haut H, étant donné que cette entrée est utilisée pour des élargissements ultérieurs.
* Il livello di DT/G in CAS non è definito precedentemente a RAS. Si raccomanda comunque che T/G abbia il livello H, dato che questo ingresso viene utilizzato per futuri ampliamenti.
* El nivel de entrada de DT/G en el CAS antes des RAS no está definido. Sin embargo, se recomienda que DT/G se mantenga en nivel H, pues esta entrada está prevista para futuras ampliaciones de los tipos de operación.

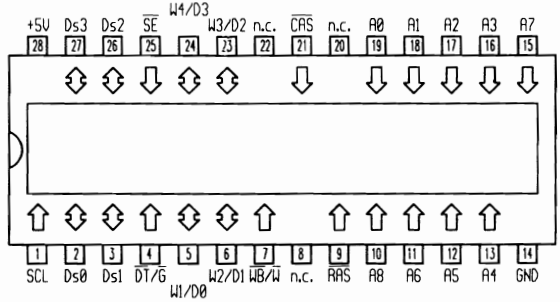
524256 — 262144x4-Bit Multiport Video RAM



* **Der Level von DT/G in CAS ist vor dem RAS nicht definiert. Es wird aber empfohlen, daß das DT/G den H-Level hat, da dieser Eingan für zukünftige Erweiterungen verwendet wird.**
* **The input level of DT/G in the CAS before RAS timing is not restricted. However it is recommended that DT/G be held H because this input will be used for future expansion of the operation mode.**
* **Le niveau de DT/G dans CAS n'est pas défini avant le RAS. Il est cependant recommandé que le DT/G ait le niveau haut H, étant donné que cette entrée est utilisée pour des élargissements ultérieurs.**
* **Il livello di DT/G in CAS non è definito precedentemente a RAS. Si raccomanda comunque che T/G abbia il livello H, dato che questo ingresso viene utilizzato per futuri ampliamenti.**
* **El nivel de entrada de DT/G en el CAS antes des RAS no está definido. Sin embargo, se recomienda que DT/G se mantenga en nivel H, pues esta entrada está prevista para futuras ampliaciones de los tipos de operación.**

524256 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 524256 J-10	Tos	32-FLAT	CMOS	0...+70	<330	<16,5	<100		TTL-TS
TC 524256 J-12	Tos	32-FLAT	CMOS	0...+70	<302,5	<16,5	<120		TTL-TS

524257 — 262144x4-Bit Multiport Video RAM



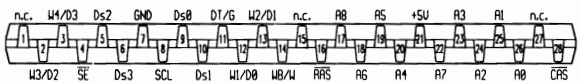
RAS	CAS	DT/G	WB/W	SE	A_n	Mode
H	H	X	X	X	X	standby
	H	H→L	H	X	valid	read
	H	H	H→L	X	valid	write
	H	H	X	X	valid (row addr.)	RAS only refresh
	L	H*	X	X	X	CAS before RAS refresh
	H	H	L	X	valid	write per bit
	L	H*	L	X	valid (A0...A3)	raster operation set up
	H	L	H	X	valid	read transfer
	H	L	L	L	valid	write transfer
	H	L	L	H	valid	pseudo write transfer

Der Level von DT/G in CAS ist vor dem RAS nicht definiert. Es wird aber empfohlen, daß das DT/G den H-Level hat, da dieser Eingang für zukünftige Erweiterungen verwendet wird.

The input level of DT/G in the CAS before RAS timing is not restricted. However it is recommended that DT/G be held H because this input will be used for future expansion of the operation mode.

524257 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 524257 P-10	Tos	28-DIP	CMOS	0...+70	<60	<3	<100	<8	TTL
TC 524257 P-12	Tos	28-DIP	CMOS	0...+70	<55	<3	<120	<8	TTL

524257 — 262144x4-Bit Multiport Video RAM



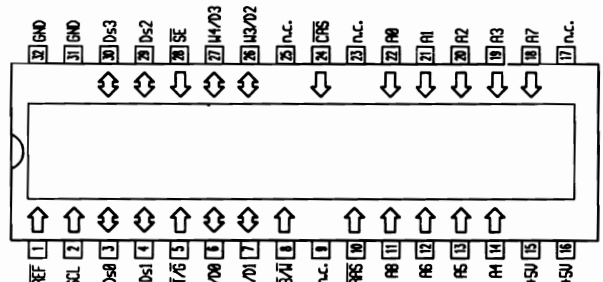
RAS	CAS	DT/G	WB/W	SE	A_n	Mode
H	H	X	X	X	X	standby
↓	H	H→L	H	X	valid	read
	H	H	H→L	X	valid	write
	H	H	X	X	valid (row addr.)	RAS only refresh
	L	H*	X	X	X	CAS before RAS refresh
	H	H	L	X	valid	write per bit
	L	H*	L	X	valid (A0...A3)	raster operation set up
	H	L	H	X	valid	read transfer
	H	L	L	L	valid	write transfer
	H	L	L	H	valid	pseudo write transfer

Der Level von DT/G in CAS ist vor dem RAS nicht definiert. Es wird aber empfohlen, daß das DT/G den H-Level hat, da dieser Eingang für zukünftige Erweiterungen verwendet wird.

The input level of DT/G in the CAS before RAS timing is not restricted. However it is recommended that DT/G be held H because this input will be used for future expansion of the operation mode.

524257 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 524257 Z-10	Tos	28-ZIP	CMOS	0...+70	<60	<3	<100	<8	TTL
TC 524257 Z-12	Tos	28-ZIP	CMOS	0...+70	<55	<3	<120	<8	TTL

524257 — 144x4-Bi 262144x4-Bit Multiport Video RAM -Bit vide



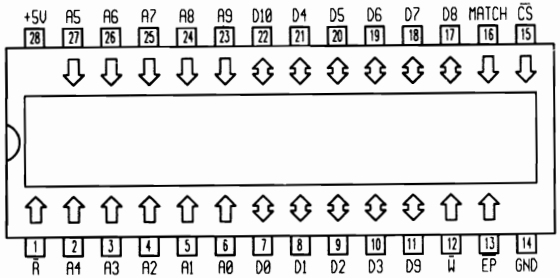
RAS	CAS	DT/G	WB/W	SE	A_n	Mode
H	H	X	X	X	X	standby
↓	H	H→L	H	X	valid	read
	H	H	H→L	X	valid	write
	H	H	X	X	valid (row addr.)	RAS only refresh
	L	H*	X	X	X	CAS before RAS refresh
	H	H	L	X	valid	write per bit
	L	H*	L	X	valid (A0...A3)	raster operation set up
	H	L	H	X	valid	read transfer
	H	L	L	L	valid	write transfer
	H	L	L	H	valid	pseudo write transfer

Der Level von DT/G in CAS ist vor dem RAS nicht definiert. Es wird aber empfohlen, daß das DT/G den H-Level hat, da dieser Eingang für zukünftige Erweiterungen verwendet wird.

The input level of DT/G in the CAS before RAS timing is not restricted. However it is recommended that DT/G be held H because this input will be used for future expansion of the operation mode.

524257 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
TC 524257 J-10	Tos	32-FLAT	CMOS	0...+70	<330	<16,5	<100		TTL-TS
TC 524257 J-12	Tos	32-FLAT	CMOS	0...+70	<302,5	<16,5	<120		TTL-TS

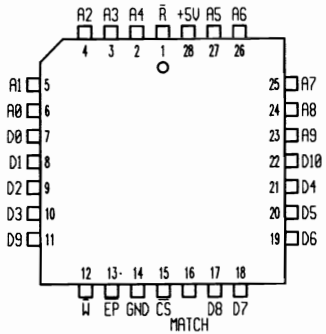
742151 — 1024x12-Bit cache address comparator



W	CS	R	Match	EP	Mode
H	L	H	L	L	parity error
H	L	H	L	H	not equal
H	L	H	H	L	undefined error
H	L	H	H	H	equal
L	L	H	H	in	write
x	H	H	H	H	device disabled
x	x	L	H	x	memory reset

742151 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ACT2151 JD	Tix	28-DIC	CMOS	0...+70	<825		25		MATCH
SN 74ACT2151 N	Tix	28-DIP	CMOS	0...+70	<825		25		MATCH

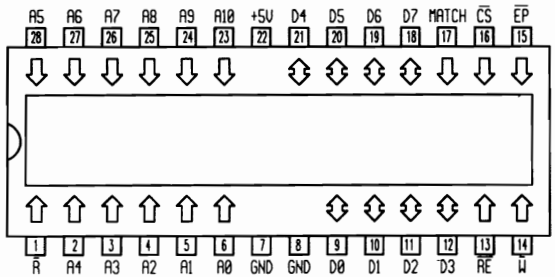
742151 — 1024x12-Bit cache address comparator



W	CS	R	Match	EP	Mode
H	L	H	L	L	parity error
H	L	H	L	H	not equal
H	L	H	H	L	undefined error
H	L	H	H	H	equal
L	L	H	H	in	write
x	H	H	H	H	device disabled
x	x	L	H	x	memory reset

742151 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / $P_{standby}$ mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
SN 74ACT2151 FN	Tix	28-PLCC	CMOS	0...+70	<825	25		MATCH

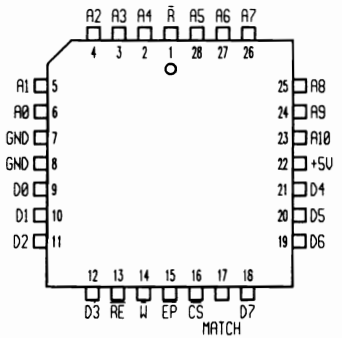
742152 — 2048x8-Bit cache address comparator



W	RE	CS	R	Match	EP	Dn	Mode
H	L	L	H	L	H	data out	read
H	H	L	H	L	L	data in	parity error
H	H	L	H	L	H	data in	not equal
H	H	L	H	H	L	data in	undefined error
H	H	L	H	H	H	data in	equal
L	x	L	H	H	in	data in	write
x	x	H	H	H	H	Hi-Z	device disabled
x	x	x	L	H	x	x	memory reset

742152 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ACT2152-25 JD	Tix	28-DIC	CMOS	0...+70	<688		<25		MATCH
SN 74ACT2152-25 N	Tix	28-DIP	CMOS	0...+70	<688		<25		MATCH
SN 74ACT2152-35 JD	Tix	28-DIC	CMOS	0...+70	<688		<35		MATCH
SN 74ACT2152-35 N	Tix	28-DIP	CMOS	0...+70	<688		<35		MATCH

742152 — 2048x8-Bit cache address comparator

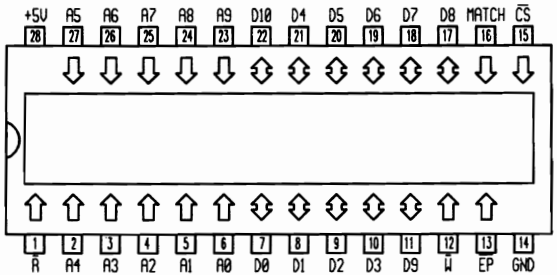


W̄	RE̅	CS̅	R̄	Match	EP̄	Dn	Mode
H	L	L	H	L	H	data out	read
H	H	L	H	L	L	data in	parity error
H	H	L	H	L	H	data in	not equal
H	H	L	H	H	L	data in	undefined error
H	H	L	H	H	H	data in	equal
L	x	L	H	H	in	data in	write
x	x	H	H	H	H	Hi-Z	device disabled
x	x	x	L	H	x	x	memory reset

742152 Type	Man	Case	Techn.	T_{U}°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ACT2152-25 FN	Tix	28-PLCC	CMOS	0...+70	<688		<25		MATCH
SN 74ACT2152-35 FN	Tix	28-PLCC	CMOS	0...+70	<688		<35		MATCH

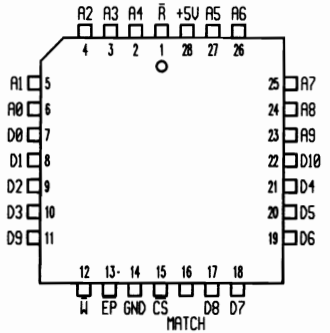
742153 — 1024x12-Bit cache address comparator

742153 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ACT2153 JD	Tix	28-DIC	CMOS	0...+70	<825		25		TTL-OD
SN 74ACT2153 N	Tix	28-DIP	CMOS	0...+70	<825		25		TTL-OD



W	CS	R	Match	EP	Mode
H	L	H	L	L	parity error
H	L	H	L	H	not equal
H	L	H	H	L	undefined error
H	L	H	H	H	equal
L	L	H	H	in	write
x	H	H	H	H	device disabled
x	x	L	H	x	memory reset

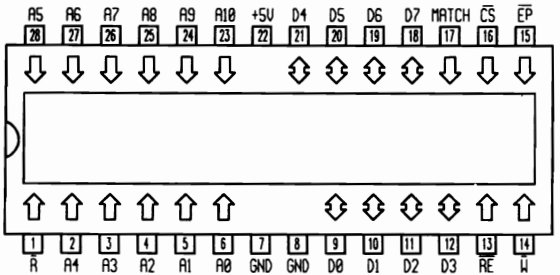
742153 — 1024x12-Bit cache address comparator



W	CS	R	Match	EP	Mode
H	L	H	L	L	parity error
H	L	H	L	H	not equal
H	L	H	H	L	undefined error
H	L	H	H	H	equal
L	L	H	H	in	write
x	H	H	H	H	device disabled
x	x	L	H	x	memory reset

742153 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW $mW/bit	P standby mW	t_{aa} ns	t_{ref} ms	Output
SN 74ACT2153 FN	Tix	28-PLCC	CMOS	0...+70	<825		25		TTL-OD

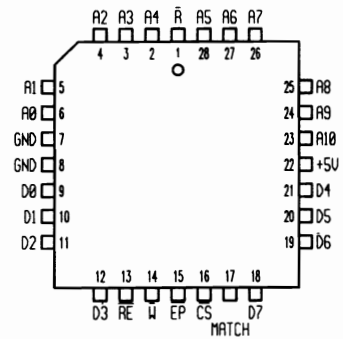
742154 — 2048x8-Bit cache address comparator



W	RE	CS	R	Match	EP	Dn	Mode
H	L	L	H	L	H	data out	read
H	H	L	H	L	L	data in	parity error
H	H	L	H	L	H	data in	not equal
H	H	L	H	H	L	data in	undefined error
H	H	L	H	H	H	data in	equal
L	x	L	H	H	in	data in	write
x	x	H	H	H	H	Hi-Z	device disabled
x	x	x	L	H	x	x	memory reset

742154 Type	Man	Case	Techn.	T_U°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ACT2154-25 JD	Tix	28-DIC	CMOS	0...+70	<688		<25		TTL-OD
SN 74ACT2154-25 N	Tix	28-DIP	CMOS	0...+70	<688		<25		TTL-OD
SN 74ACT2154-35 JD	Tix	28-DIC	CMOS	0...+70	<688		<35		TTL-OD
SN 74ACT2154-35 N	Tix	28-DIP	CMOS	0...+70	<688		<35		TTL-OD

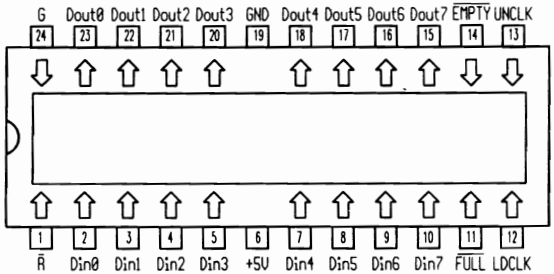
742154 — 2048x8-Bit cache address comparator



$\overline{W}$	$\overline{RE}$	$\overline{CS}$	$\overline{R}$	Match	$\overline{EP}$	Dn	Mode
H	L	L	H	L	H	data out	read
H	H	L	H	L	L	data in	parity error
H	H	L	H	L	H	data in	not equal
H	H	L	H	H	L	data in	undefined error
H	H	L	H	H	H	data in	equal
L	x	L	H	H	in	data in	write
x	x	H	H	H	H	Hi-Z	device disabled
x	x	x	L	H	x	x	memory reset

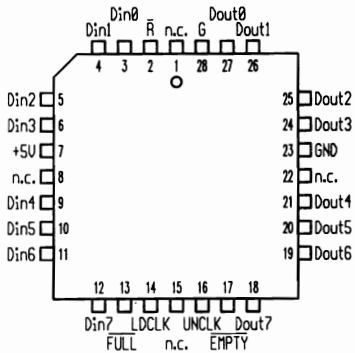
742154 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
SN 74ACT2154-25 FN	Tix	28-PLCC	CMOS	0...+70	<688	<25		TTL-OD
SN 74ACT2154-35 FN	Tix	28-PLCC	CMOS	0...+70	<688	<35		TTL-OD

742232 — 64 words x 8-Bit asynchronous FIFO

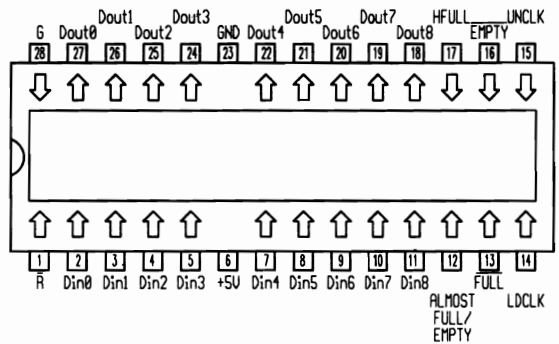


742232 Type	Man	Case	Techn.	T_U°C	P_{typ} mW / P standby mW $mW/bit	t_{aa} ns	t_{ref} ms	Output
SN 74ALS2232 DW	Tix	24-FLAT	TTL	0...+70	<1485	<30		TTL-TS
SN 74ALS2232 NT	Tix	24-TDIP	TTL	0...+70	<1485	<30		TTL-TS

742232 — 64 words x 8-Bit asynchronous FIFO



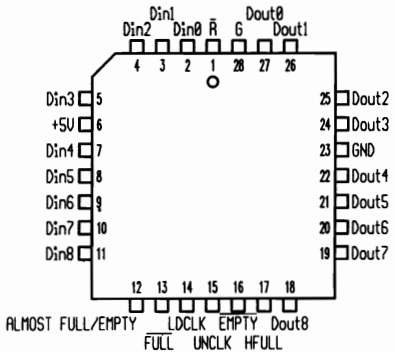
742233 — 64 words x 9-Bit asynchronous FIFO



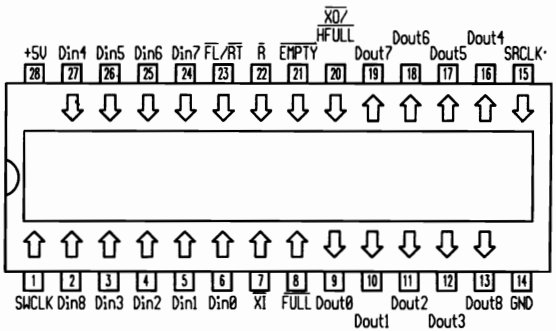
742232 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ALS2232 FN	Tix	28-PLCC	TTL	0...+70	<1485		<30		TTL-TS

742233 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ALS2233 N	Tix	28-DIP	TTL	0...+70	<1595		<30		TTL-TS

742233 — 64 words x 9-Bit asynchronous FIFO



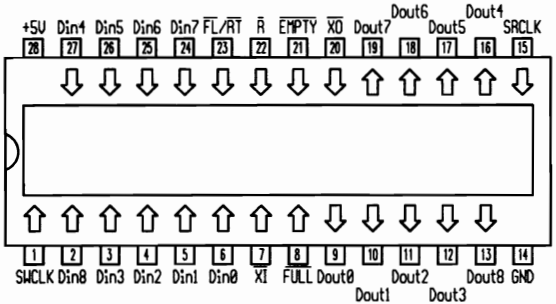
747201 — 512 words x 9-Bit asynchronous FIFO

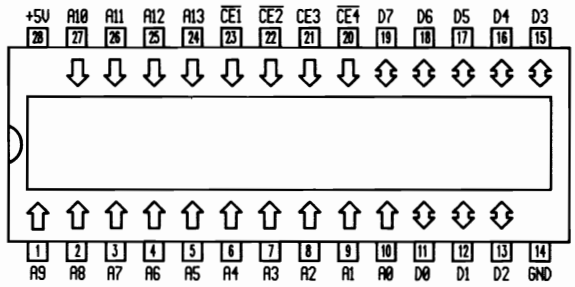


742233 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ALS2233 FN	Tix	28-PLCC	TTL	0...+70	<1595		<30		TTL-TS

747201 Type	Man	Case	Techn.	T_U/°C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ACT7201 A-25N	Tix	28-DIP	CMOS	0...+70	<440	<44	<25		TTL-TS
SN 74ACT7201 A-35N	Tix	28-DIP	CMOS	0...+70	<440	<44	<35		TTL-TS
SN 74ACT7201 A-50N	Tix	28-DIP	CMOS	0...+70	<440	<44	<50		TTL-TS

747202	1024 words x 9-Bit asynchronous FIFO	821281	16384x8-Bit PROM



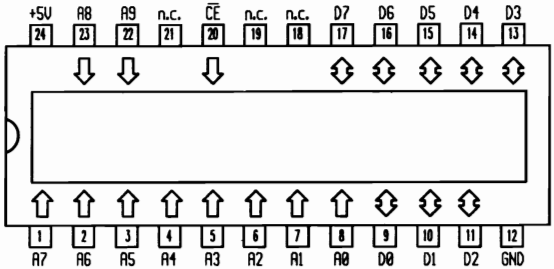


747202 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
SN 74ACT7202-35 N	Tix	28-DIP	CMOS	0...+70	<440	<44	<35		TTL-TS
SN 74ACT7202-50 N	Tix	28-DIP	CMOS	0...+70	<440	<44	<50		TTL-TS

821281 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82HS1281 N	Val	28-DIP	TTL	0...+75	<971		<45		TTL-TS

822708

1204x8-Bit PROM



822708 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
6384-1	Mmi	24-DIC	TTL	0...+70	<945		<90		TTL-OC
6385-1	Mmi	24-DIC	TTL	0...+70	<945		<90		TTL-TS
µPB 417 C	Nip	24-DIP	TTL	-25...+75	<770		<60		TTL-TS
µPB 417 C-1	Nip	24-DIP	TTL	-25...+75	<770		<50		TTL-TS
µPB 417 D	Nip	24-DIC	TTL	-25...+75	<770		<60		TTL-TS
µPB 417 D-1	Nip	24-DIC	TTL	-25...+75	<770		<50		TTL-TS

822708 Type	Man	Case	Techn.	T_U °C	P_{typ} mW	P standby mW	t_{aa} ns	t_{ref} ms	Output
					$mW/bit				
N 82S2708 F	Sig	24-DIC	TTL	0...+75	<919		<70		TTL-TS
N 82S2708 N	Sig	24-DIP	TTL	0...+75	<919		<70		TTL-TS
S 82S2708 F	Sig	24-DIC	TTL	-55...+125	<1017		<90		TTL-TS
S 82S2708 N	Sig	24-DIP	TTL	-55...+125	<1017		<90		TTL-TS
SN 74S2708 J	Tix	24-DIC	TTL	0...+70	<919		<70		TTL-TS
SN 74S2708 N	Tix	24-DIP	TTL	0...+70	<919		<70		TTL-TS
TBP 28S2708 J	Tix	24-DIC	TTL	0...+70	<919		<70		TTL-TS
TBP 28S2708 N	Tix	24-DIP	TTL	0...+70	<919		<70		TTL-TS

NOTES

OTHER TITLES OF INTEREST

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